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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	149
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b60l7c6e0x

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Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
Port C											
PC[0] ⁽¹⁰⁾	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	87	126	154	A8
PC[1] ⁽¹⁰⁾	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F ⁽¹¹⁾	Tristate	82	121	149	C9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX DEBUG[0] EIRQ[5]	SIUL DSPI_1 FlexCAN_4 SSCM SIUL	I/O I/O O O I	M	Tristate	78	117	145	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] DEBUG[1] EIRQ[6] CAN1RX CAN4RX	SIUL DSPI_1 ADC_0 SSCM SIUL FlexCAN_1 FlexCAN_4	I/O I/O O O I I I	S	Tristate	77	116	144	B11



Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PD[0]	PCR[48]	AF0	GPIO[48]	SIUL	I	I	Tristate	41	63	77	P12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	WKPU[27] ⁽⁵⁾	WKPU	I						
		—	ADC0_P[4]	ADC_0	I						
		—	ADC1_P[4]	ADC_1	I						
PD[1]	PCR[49]	AF0	GPIO[49]	SIUL	I	I	Tristate	42	64	78	T12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	WKPU[28] ⁽⁵⁾	WKPU	I						
		—	ADC0_P[5]	ADC_0	I						
		—	ADC1_P[5]	ADC_1	I						
PD[2]	PCR[50]	AF0	GPIO[50]	SIUL	I	I	Tristate	43	65	79	R12
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[6]	ADC_0	I						
		—	ADC1_P[6]	ADC_1	I						
PD[3]	PCR[51]	AF0	GPIO[51]	SIUL	I	I	Tristate	44	66	80	P13
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[7]	ADC_0	I						
		—	ADC1_P[7]	ADC_1	I						

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PD[4]	PCR[52]	AF0	GPIO[52]	SIUL	I	I	Tristate	45	67	81	R13
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[8]	ADC_0	I						
		—	ADC1_P[8]	ADC_1	I						
PD[5]	PCR[53]	AF0	GPIO[53]	SIUL	I	I	Tristate	46	68	82	T13
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[9]	ADC_0	I						
		—	ADC1_P[9]	ADC_1	I						
PD[6]	PCR[54]	AF0	GPIO[54]	SIUL	I	I	Tristate	47	69	83	T14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[10]	ADC_0	I						
		—	ADC1_P[10]	ADC_1	I						
PD[7]	PCR[55]	AF0	GPIO[55]	SIUL	I	I	Tristate	48	70	84	R14
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_P[11]	ADC_0	I						
		—	ADC1_P[11]	ADC_1	I						

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC_0	I/O I/O I/O O	M	Tristate	94	133	161	C6
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	95	139	167	B5
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	96	140	168	C4
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	13	21	G2
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] ⁽⁵⁾ CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	10	14	22	G1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlex_8 —	I/O I/O O —	S	Tristate	—	—	172	A9
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] ⁽⁵⁾ LIN8RX	SIUL eMIOS_0 — — WKPU LINFlex_8	I/O I/O — — I I	S	Tristate	—	—	171	A10
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlex_9 —	I/O I/O O —	S	Tristate	—	—	170	B10
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] ⁽⁵⁾ LIN9RX	SIUL eMIOS_0 — — WKPU LINFlex_9	I/O I/O — — I I	S	Tristate	—	—	169	C10
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	143	A12

4.4 Recommended operating conditions

Table 13. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD}^{(1)}$	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
$V_{SS_LV}^{(2)}$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
$V_{DD_BV}^{(3)}$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	$V_{DD} - 0.1$	$V_{DD} + 0.1$	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V
$V_{DD_ADC}^{(4)}$	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0 ⁽⁵⁾	3.6	V
			Relative to V_{DD}	$V_{DD} - 0.1$	$V_{DD} + 0.1$	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	$V_{SS} - 0.1$	—	V
			Relative to V_{DD}	—	$V_{DD} + 0.1$	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up ⁽⁶⁾	—	3.0 ⁽⁷⁾	250×10^3 (0.25 [V/ μ s])	V/s

- 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
- 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
- 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). Supply ramp slope on V_{DD_BV} should always be faster or equal to slope of V_{DD_HV} . Otherwise, device may enter regulator bypass mode if slope on V_{DD_BV} is slower.
- 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
- Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL} , device is reset.
- Guaranteed by device validation.
- Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

Table 24. I/O weight⁽¹⁾ (continued)

Supply segment			Pad	LQFP176				LQFP144/100			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 176	LQFP 144	LQFP 100		SRC ⁽²⁾ = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	—	—	PB[11]	1%	—	1%	—	—	—	—	—
	—	—	PD[12]	11%	—	13%	—	—	—	—	—
	2	2	PB[12]	11%	—	13%	—	15%	—	17%	—
			PD[13]	11%	—	13%	—	14%	—	17%	—
			PB[13]	11%	—	13%	—	14%	—	17%	—
			PD[14]	11%	—	13%	—	14%	—	17%	—
			PB[14]	11%	—	13%	—	14%	—	16%	—
			PD[15]	11%	—	13%	—	13%	—	16%	—
			PB[15]	11%	—	13%	—	13%	—	15%	—
	—	—	PI[8]	10%	—	12%	—	—	—	—	—
	—	—	PI[9]	10%	—	12%	—	—	—	—	—
	—	—	PI[10]	10%	—	12%	—	—	—	—	—
	—	—	PI[11]	10%	—	12%	—	—	—	—	—
	—	—	PI[12]	10%	—	12%	—	—	—	—	—
	—	—	PI[13]	10%	—	11%	—	—	—	—	—
	2	2	PA[3]	9%	—	11%	—	11%	—	13%	—
		—	PG[13]	9%	13%	11%	11%	10%	14%	12%	13%
		—	PG[12]	9%	13%	10%	11%	10%	14%	12%	12%
		—	PH[0]	6%	8%	7%	7%	6%	9%	7%	8%
		—	PH[1]	6%	8%	7%	7%	6%	8%	7%	7%
		—	PH[2]	5%	7%	6%	6%	5%	7%	6%	7%
		—	PH[3]	5%	7%	5%	6%	5%	7%	6%	6%
		—	PG[1]	4%	—	5%	—	4%	—	5%	—
		—	PG[0]	4%	5%	4%	5%	4%	5%	4%	5%

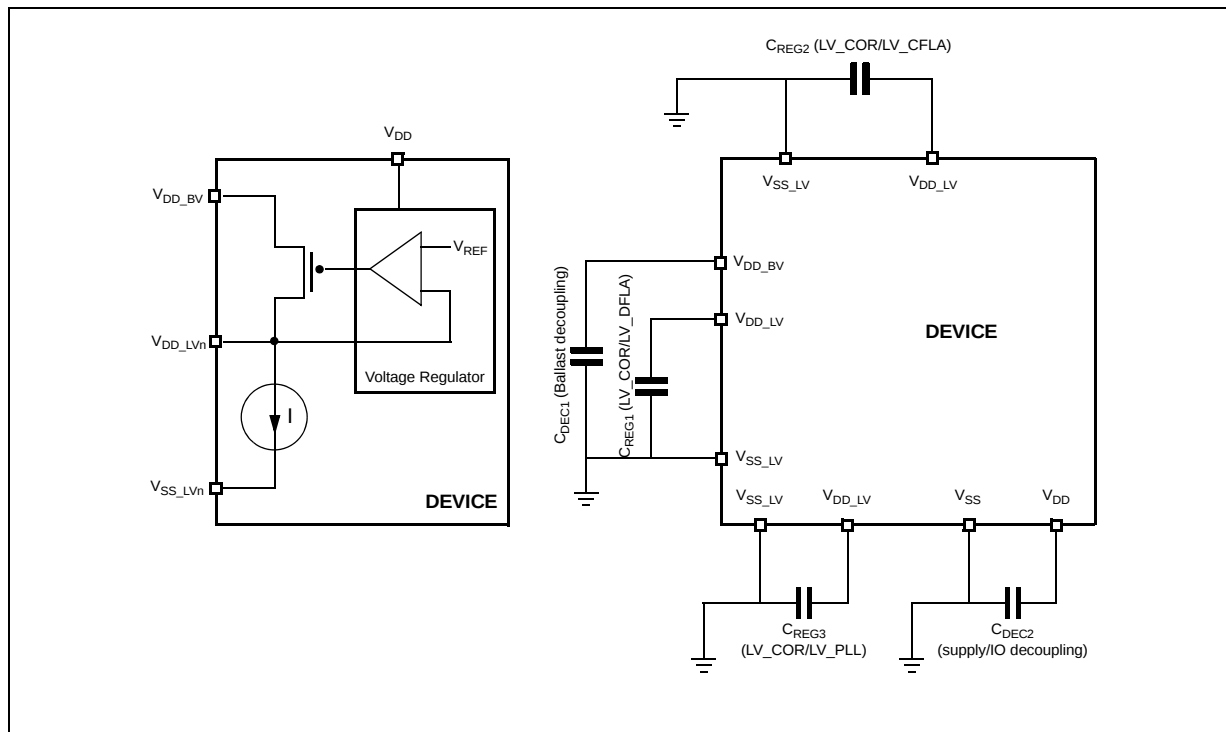
4.8 Power management electrical characteristics

4.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV} . The regulator itself is supplied by the common I/O supply V_{DD} . The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD} .
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
 - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
 - LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
 - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 9. Voltage regulator capacitance connection



1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified.
2. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
3. This value is acceptable to guarantee operation from 4.5 V to 5.5 V.
4. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.
5. In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 μs , depending on external capacitances to be loaded).
6. The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

4.8.2 Low voltage detector electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as five low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27_VREG in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the $5.0\text{ V} \pm 10\%$ range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

Note: When enabled, power domain No. 2 is monitored through LVDLVBKP.

Table 32. Flash power supply DC electrical characteristics

Symbol		Parameter	Conditions ⁽¹⁾		Value			Unit
					Min	Typ	Max	
I _{CFREAD}	CC	Sum of the current consumption on V _{DD_HV} and V _{DD_BV} on read access	Flash module read f _{CPU} = 64 MHz	Code Flash	—	—	33	mA
I _{DFREAD}				Data Flash	—	—	33	
I _{CFMOD}	CC	Sum of the current consumption on V _{DD_HV} and V _{DD_BV} on matrix modification (program/erase)	Program/Erase on-going while reading Flash registers f _{CPU} = 64 MHz	Code Flash	—	—	52	mA
I _{DFMOD}				Data Flash	—	—	33	
I _{CFLPW}	CC	Sum of the current consumption on V _{DD_HV} and V _{DD_BV} during Flash low power mode	—	Code Flash	—	—	1.1	mA
I _{DFLPW}				Data Flash	—	—	900	
I _{CFPWD}	CC	Sum of the current consumption on V _{DD_HV} and V _{DD_BV} during Flash power down mode	—	Code Flash	—	—	150	μA
I _{DFPWD}				Data Flash	—	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

4.10.3 Start-up/Switch-off timings

Table 33. Start-up time/Switch-off time

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
t _{FLARSTEXIT}	CC	T	Delay for Flash module to exit reset mode	—	—	125	μs
t _{FLALPEXIT}	CC	T	Delay for Flash module to exit low-power mode	—	—	0.5	
t _{FLAPDEXIT}	CC	T	Delay for Flash module to exit power-down mode	—	—	30	
t _{FLALPENTRY}	CC	T	Delay for Flash module to enter low-power mode	—	—	0.5	
t _{FLAPDENTRY}	CC	T	Delay for Flash module to enter power-down mode	—	—	1.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

4.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
 - Corrupted program counter
 - Unexpected reset
 - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

4.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 34. EMI radiated emission measurement⁽¹⁾⁽²⁾

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.15 0		1000	MHz
f _{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V _{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S _{EMI}	CC	T	Peak level	V _{DD} = 5 V, T _A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f _{OSC} = 8 MHz/f _{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBμ V
					± 2% PLL frequency modulation	—	—	14	dBμ V

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.

2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Figure 11. Crystal oscillator and resonator connection scheme

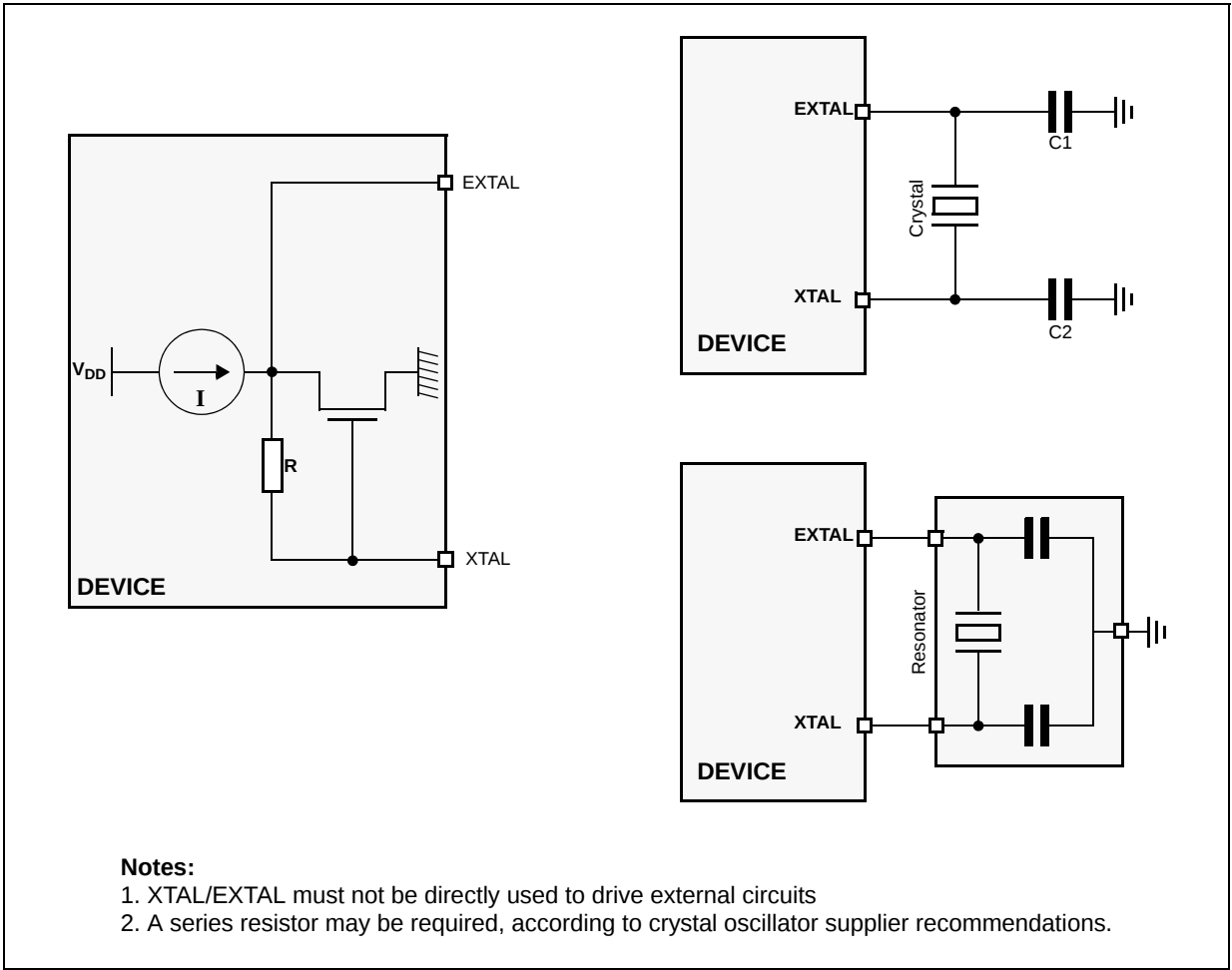


Table 37. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout $C1 = C2$ (pF) ⁽¹⁾	Shunt capacitance between xtalout and xtal in $C0$ ⁽²⁾ (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Figure 12. Fast external crystal oscillator (4 to 16 MHz) timing diagram

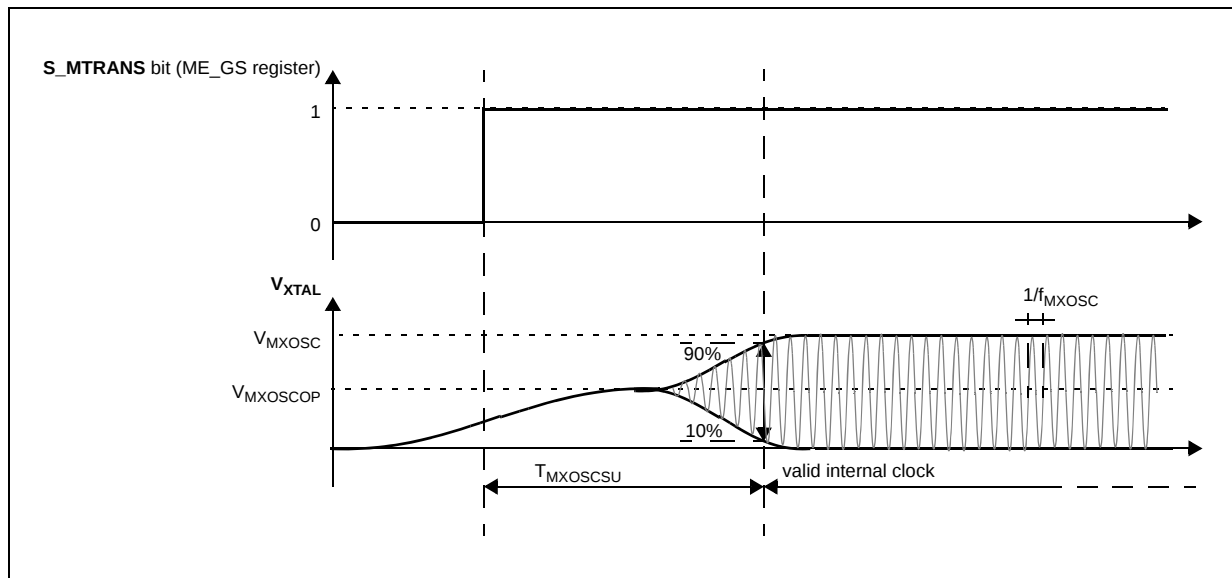


Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
f _{FXOSC}	S R	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g _{mFXOSC}	C C	Fast external crystal oscillator transconductance	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/ V
	C C		V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	C C		V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	C C		V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V _{FXOSC}	C C	Oscillation amplitude at EXTAL	f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
			f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
V _{FXOSCO}	C C	Oscillation operating point	—	—	0.95	—	V

Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾	Value			Unit
					Min	Typ	Max	
I _{FXOSC} ⁽²⁾	C C	T	Fast external crystal oscillator consumption	—	—	2	3	mA
t _{FXOSCSU}	C C	T	Fast external crystal oscillator start-up time	f _{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f _{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V _{IH}	S R	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	0.65V _{DD}	—	V _{DD} + 0.4	V
V _{IL}	S R	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	−0.4	—	0.35V _{DD}	V

1. $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified.

2. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 13. Crystal oscillator and resonator connection scheme

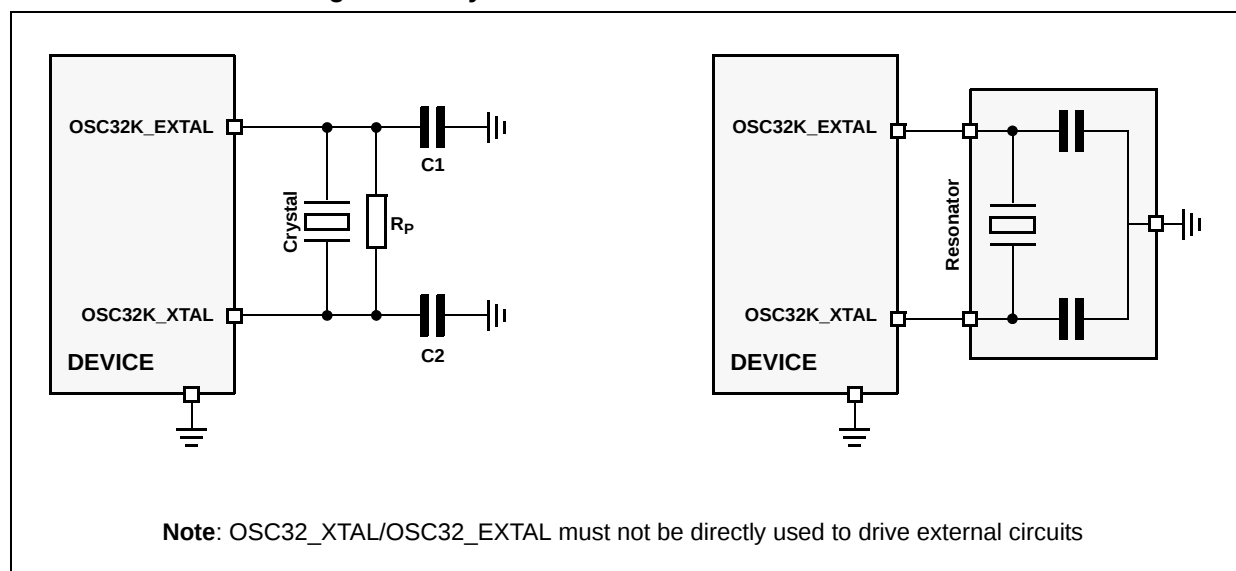
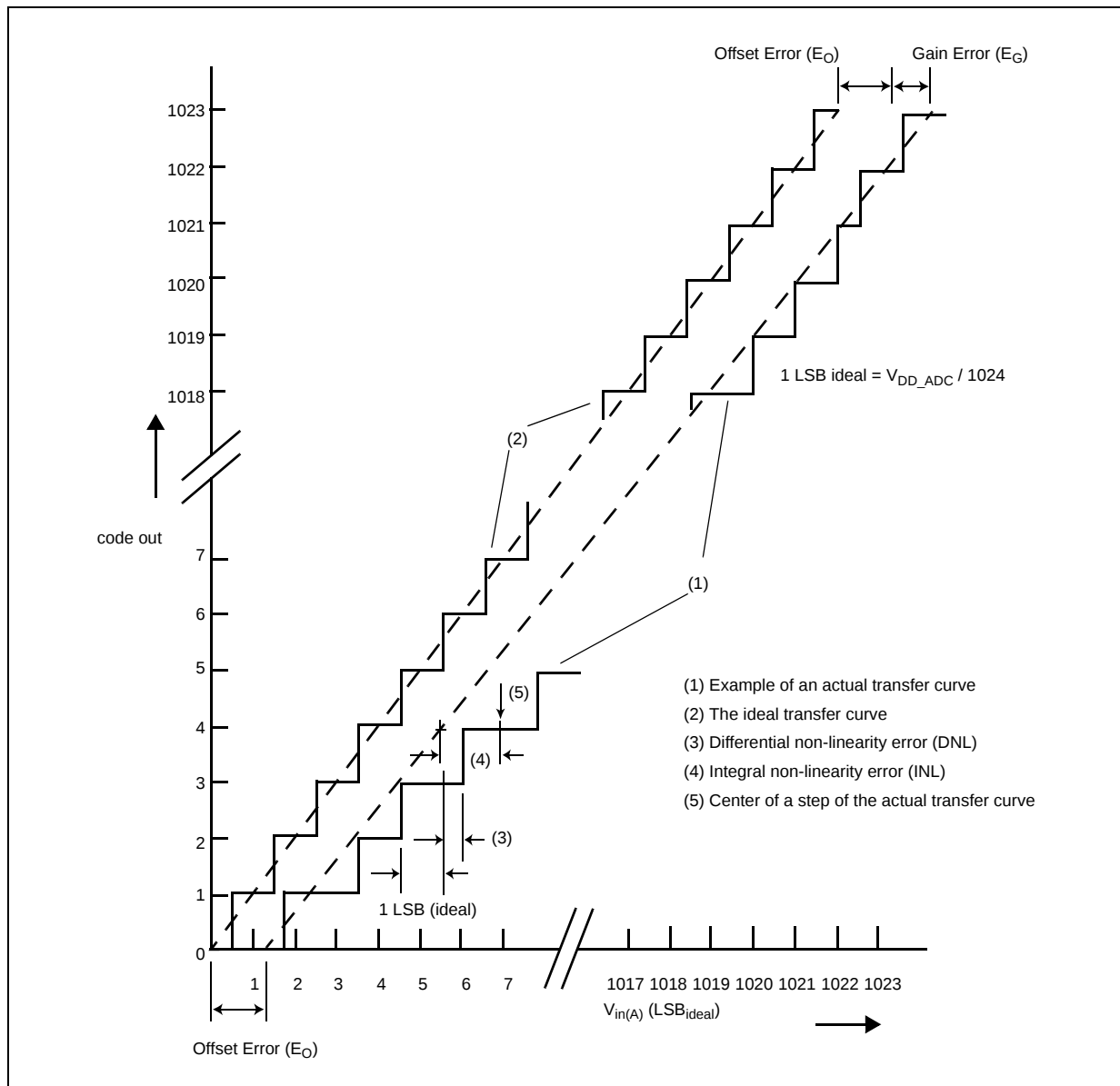


Figure 16. ADC_0 characteristic and error definitions



4.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source

Table 46. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions ⁽¹⁾	Value			Unit
					Min	Typ	Max	
I _{ADC1pwd}	SR	—	ADC_1 consumption in power down mode	—	—	—	50	μA
I _{ADC1run}	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f _{ADC1}	SR	—	ADC_1 analog frequency	V _{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V _{DD} = 5 V	3.33	—	32 + 4%	
t _{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	μs
t _{ADC1_S}	CC	T	Sampling time ⁽⁴⁾ V _{DD} = 3.3 V	f _{ADC1} = 20 MHz, INPSAMP = 12	600	—	—	ns
			Sampling time ⁽⁴⁾ V _{DD} = 5.0 V	f _{ADC1} = 32 MHz, INPSAMP = 17	500	—	—	
			Sampling time ⁽⁴⁾ V _{DD} = 3.3 V	f _{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	μs
			Sampling time ⁽⁴⁾ V _{DD} = 5.0 V	f _{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	
t _{ADC1_C}	CC	P	Conversion time ⁽⁵⁾ V _{DD} = 3.3 V	f _{ADC1} = 20 MHz, INPCMP = 0	2.4	—	—	μs
			Conversion time ⁽⁵⁾ V _{DD} = 5.0 V	f _{ADC1} = 32 MHz, INPCMP = 0	1.5	—	—	μs
			Conversion time ⁽⁵⁾ V _{DD} = 3.3 V	f _{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	μs
			Conversion time ⁽⁵⁾ V _{DD} = 5.0 V	f _{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	μs
Δ _{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1 ⁽⁶⁾	45	—	55	%
C _S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C _{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C _{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C _{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R _{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R _{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R _{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Figure 25. DSPI classic SPI timing — slave, CPHA = 1

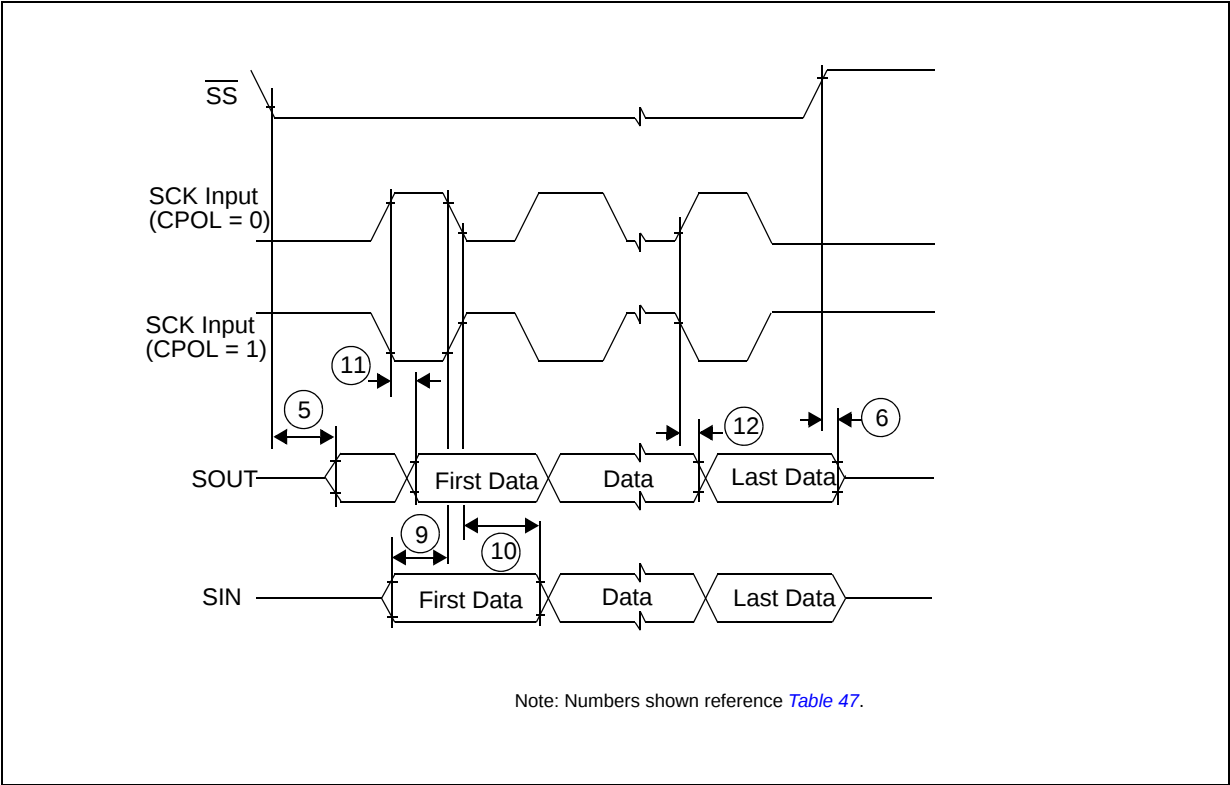


Figure 26. DSPI modified transfer format timing — master, CPHA = 0

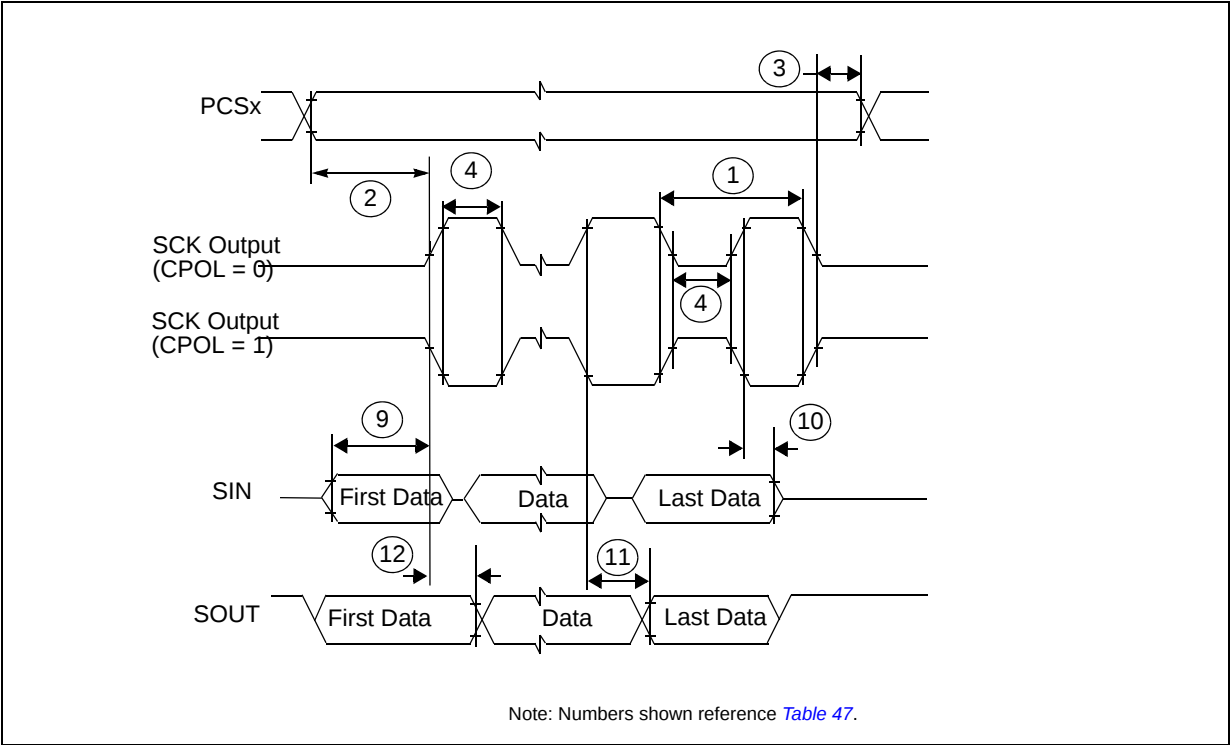


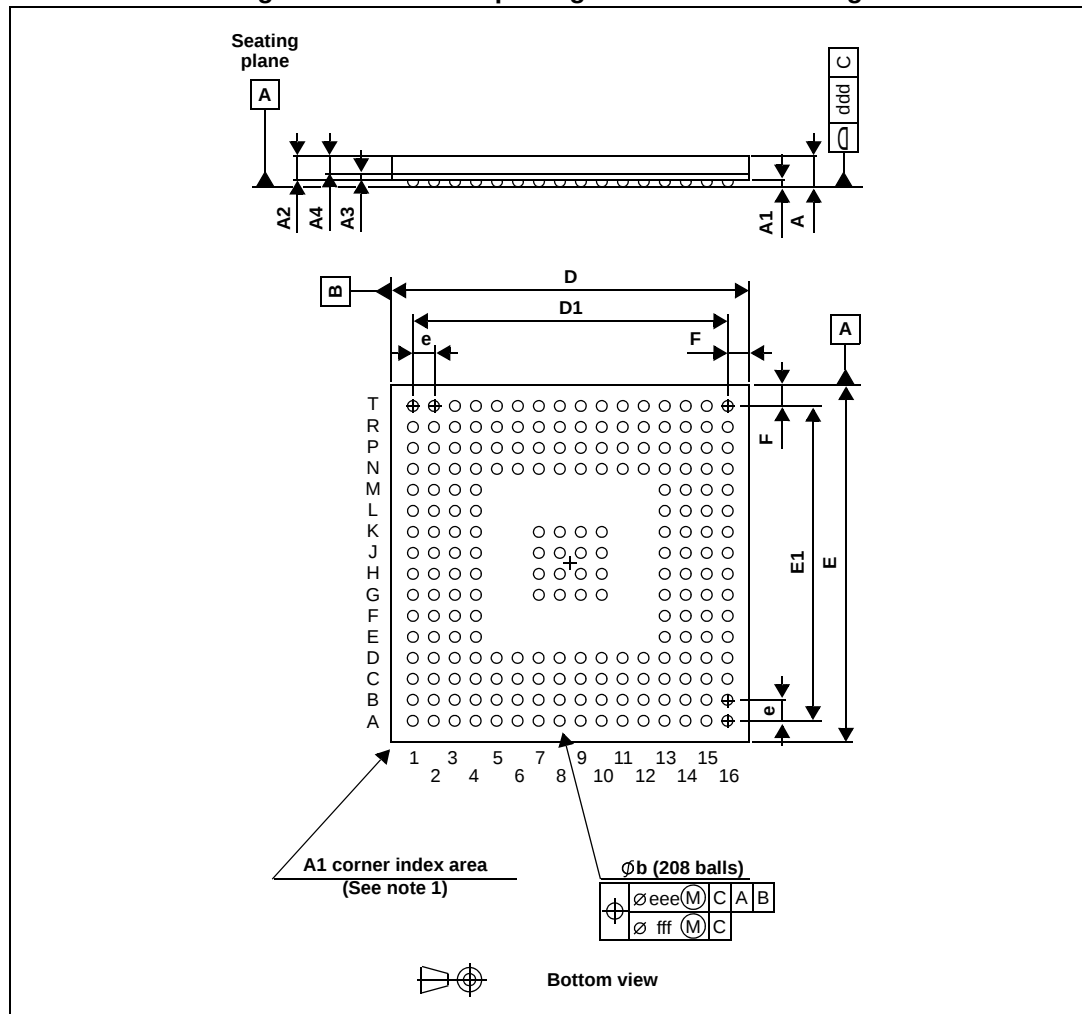
Table 52. LQFP144 mechanical data (continued)

Symbol	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2.4 LBGA208

Figure 36. LBGA208 package mechanical drawing



1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 54. LBGA208 mechanical data

Symbol	mm			inches ⁽¹⁾			Notes
	Min	Typ	Max	Min	Typ	Max	
A	—	—	1.70	—	—	0.0669	(2)
A1	0.30	—	—	0.0118	—	—	—
A2	—	1.085	—	—	0.0427	—	—
A3	—	0.30	—	—	0.0118	—	—
A4	—	—	0.80	—	—	0.0315	—
b	0.50	0.60	0.70	0.0197	0.0236	0.0276	(3)