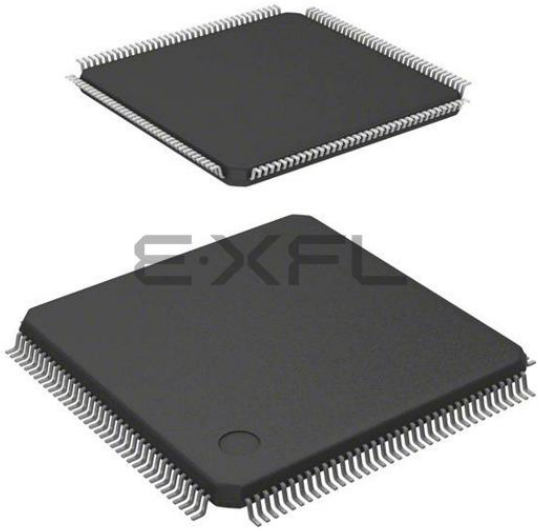

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b64l5c6e0y

List of tables

Table 3 summarizes the functions of the blocks present on the SPC560B54/6x.

Table 3. SPC560B54/6x series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Inter-integrated circuit (I^2C) bus	Two-wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device

Figure 3 shows the SPC560B54/6x in the LQFP144 package.

Figure 3. LQFP144 pin configuration

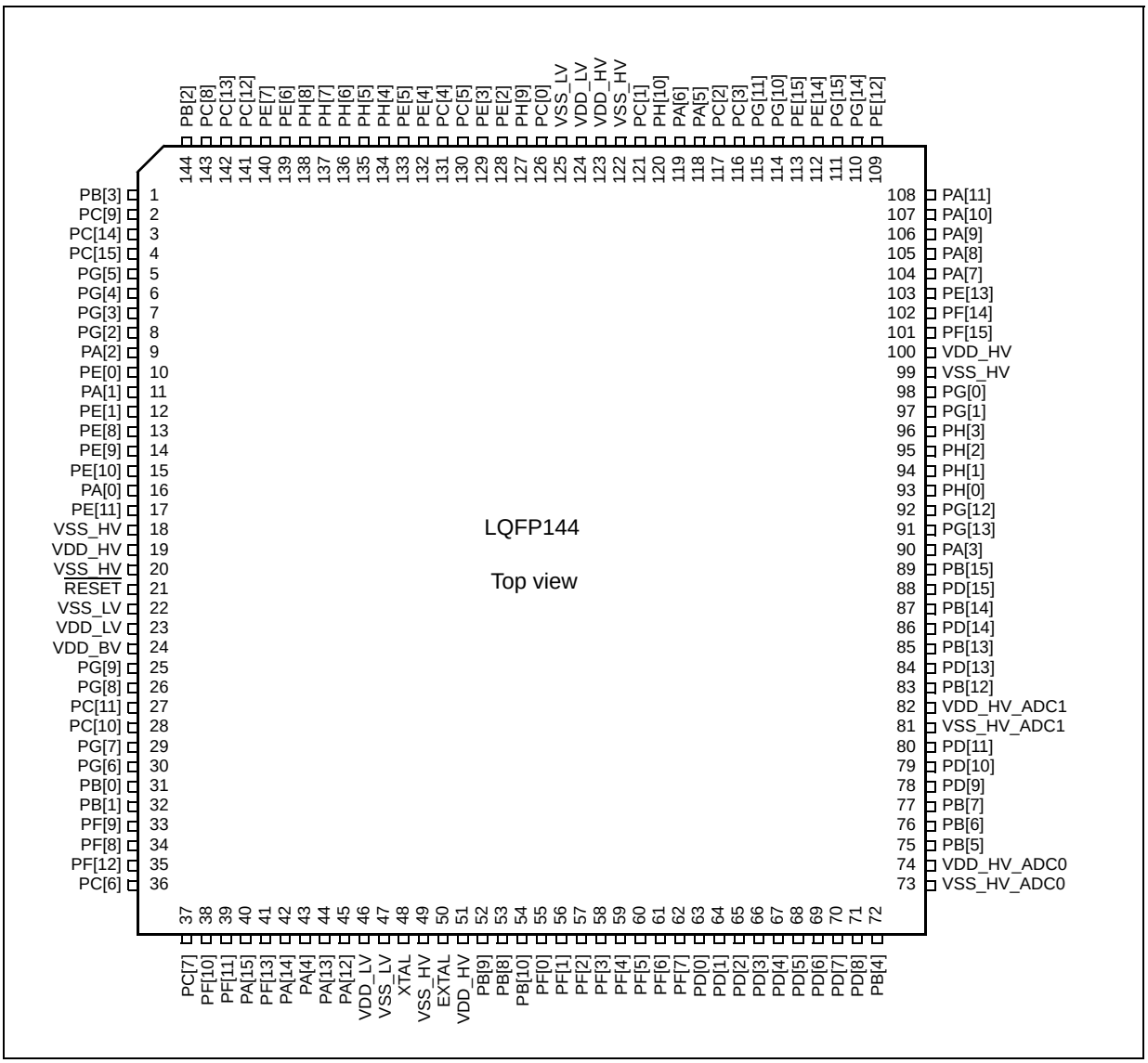


Figure 4 shows the SPC560B54/6x in the LQFP100 package.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[7] —	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3	I/O I/O I/O — I I I	S	Input, weak pull-up	72	105	129	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[7]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	106	130	C15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2]	SIUL eMIOS_0 I^2C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	107	131	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C_0 — SIUL LINFlex_2 ADC_1	I/O I/O I/O — I I I	J	Tristate	75	108	132	B15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	J	Tristate	—	—	97	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	61	83	101	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	63	85	103	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	65	87	105	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	67	89	107	L13

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — WKPU[16][5] LIN5RX	SIUL eMIOS_1 — — WKPU LINFlex_5	I/O I/O — — I I	S	Tristate	—	41	49	T6
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1	I/O O I/O O	M	Tristate	—	102	126	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] E1UC[4] — — EIRQ[13] CAN1RX CAN4RX	SIUL eMIOS_1 — — SIUL FlexCAN_1 FlexCAN_4	I/O I/O — — I I I	S	Tristate	—	101	125	E15
Port G											
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	98	122	E14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PI[5]	PCR[133]	AF0 AF1 AF2 AF3	GPIO[133] E1UC[29] SCK_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O I/O —	S	Tristate	—	—	142	C12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3	GPIO[134] E1UC[30] CS0_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O I/O —	S	Tristate	—	—	11	D2
PI[7]	PCR[135]	AF0 AF1 AF2 AF3	GPIO[135] E1UC[31] CS1_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	12	D3
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	108	J13
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	109	J14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	J	Tristate	—	—	76	R8
PI[15]	PCR[143]	AF0 AF1 AF2 AF3 —	GPIO[143] CS0_4 — — ADC0_S[23]	SIUL DSPI_4 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	75	T8
Port J											
PJ[0]	PCR[144]	AF0 AF1 AF2 AF3 —	GPIO[144] CS1_4 — — ADC0_S[24]	SIUL DSPI_4 — — ADC_0	I/O O — — I	J	Tristate	—	—	74	N5
PJ[1]	PCR[145]	AF0 AF1 AF2 AF3 — —	GPIO[145] — — — ADC0_S[25] SIN_5	SIUL — — —— ADC_0 DSPI_5	I/O — — — I I	J	Tristate	—	—	73	P5

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	S R	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	S R	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
V_{SS_LV}(3)	S R	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}(4)	S R	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to V_{DD}	3.0	V_{DD} + 0.1	
V_{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}(5)	S R	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	S R	V_{DD} slope to ensure correct power up(6)	—	3.0(7)	250×10^3 (0.25 [V/µs])	V/s

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.
3. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
4. 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD\_HV}$ in order to ensure the device does not enter regulator bypass mode.
5. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
6. Guaranteed by device validation.
7. Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

Note: RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 20. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		C			I_{OH} = –7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C			I_{OH} = –11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
		C			I_{OL} = 7 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	0.1V_{DD}	
		C			I_{OL} = 11 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 21. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	

Table 23. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 24 provides the weight of concurrent switching I/Os.

Table 24. I/O weight[1] (continued)

Supply segment			Pad	LQFP176				LQFP144/100			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 176	LQFP 144	LQFP 100		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	—	—	PB[11]	1%	—	1%	—	—	—	—	—
	—	—	PD[12]	11%	—	13%	—	—	—	—	—
	2	2	PB[12]	11%	—	13%	—	15%	—	17%	—
			PD[13]	11%	—	13%	—	14%	—	17%	—
			PB[13]	11%	—	13%	—	14%	—	17%	—
			PD[14]	11%	—	13%	—	14%	—	17%	—
			PB[14]	11%	—	13%	—	14%	—	16%	—
			PD[15]	11%	—	13%	—	13%	—	16%	—
			PB[15]	11%	—	13%	—	13%	—	15%	—
	—	—	PI[8]	10%	—	12%	—	—	—	—	—
	—	—	PI[9]	10%	—	12%	—	—	—	—	—
	—	—	PI[10]	10%	—	12%	—	—	—	—	—
	—	—	PI[11]	10%	—	12%	—	—	—	—	—
	—	—	PI[12]	10%	—	12%	—	—	—	—	—
	—	—	PI[13]	10%	—	11%	—	—	—	—	—
	2	2	PA[3]	9%	—	11%	—	11%	—	13%	—
		—	PG[13]	9%	13%	11%	11%	10%	14%	12%	13%
		—	PG[12]	9%	13%	10%	11%	10%	14%	12%	12%
		—	PH[0]	6%	8%	7%	7%	6%	9%	7%	8%
		—	PH[1]	6%	8%	7%	7%	6%	8%	7%	7%
		—	PH[2]	5%	7%	6%	6%	5%	7%	6%	7%
		—	PH[3]	5%	7%	5%	6%	5%	7%	6%	6%
		—	PG[1]	4%	—	5%	—	4%	—	5%	—
		—	PG[0]	4%	5%	4%	5%	4%	5%	4%	5%

4.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 35. ESD absolute maximum ratings(1)(2)

Symbol	Ratings	Conditions	Class	Max value(3)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production

4.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 36. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.12 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. *Figure 11* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 37 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

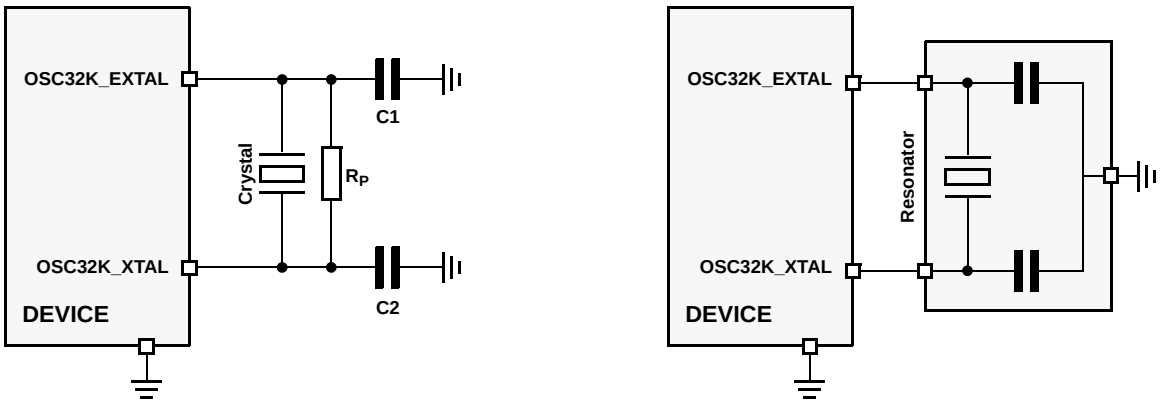
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FXOSC}[2]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA
$t_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 13. Crystal oscillator and resonator connection scheme



Note: OSC32_XTAL/OSC32_EXTAL must not be directly used to drive external circuits

Figure 14. Equivalent circuit of a quartz crystal

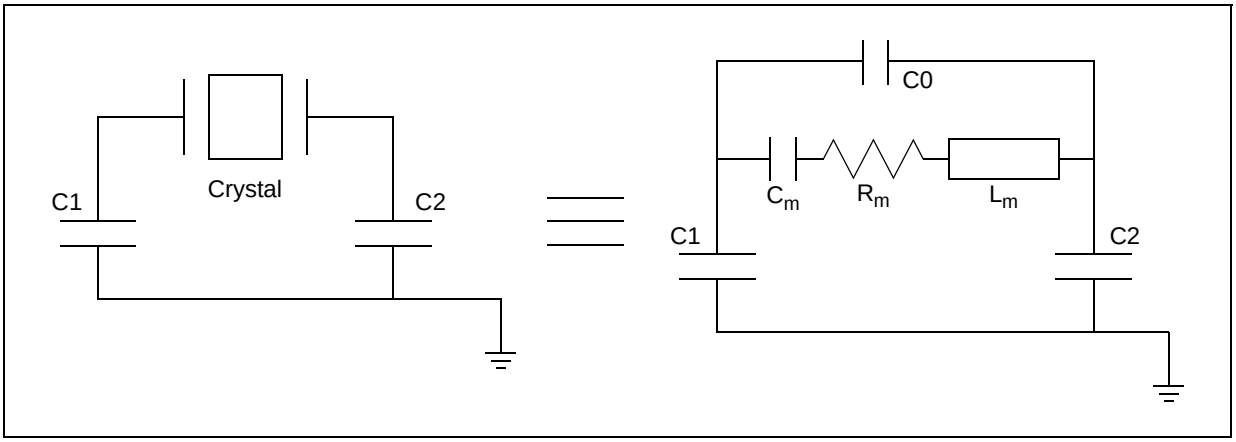


Table 39. Crystal motional characteristics(1)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground(2)	—	18	—	28	pF
R_m(3)	Motional resistance	AC coupled at C0 = 2.85 pF(4)	—	—	65	kW
		AC coupled at C0 = 4.9 pF(4)	—	—	50	
		AC coupled at C0 = 7.0 pF(4)	—	—	35	
		AC coupled at C0 = 9.0 pF(4)	—	—	30	

1. The crystal used is Epson Toyocom MC306.
2. This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3. Maximum ESR (R_m) of the crystal is 50 kΩ.
4. C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

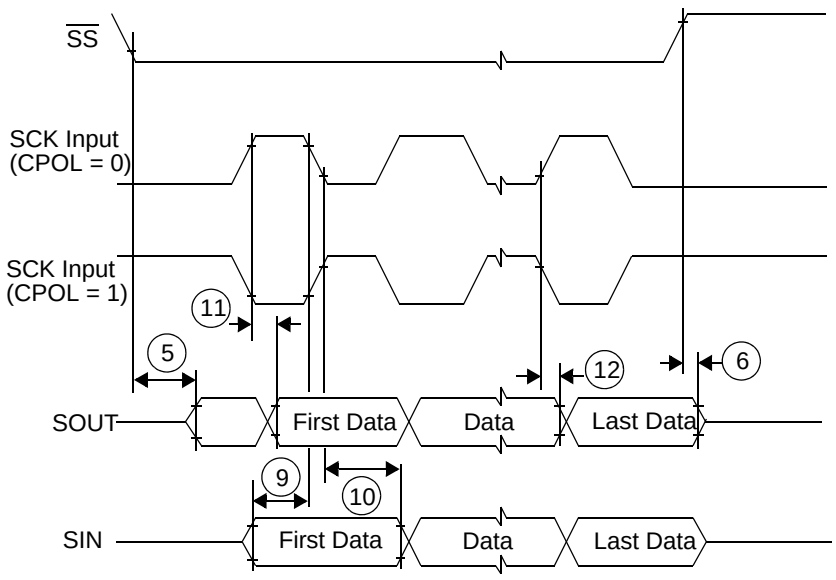
4.18 On-chip peripherals

4.18.1 Current consumption

Table 47. On-chip peripherals current consumption(1)

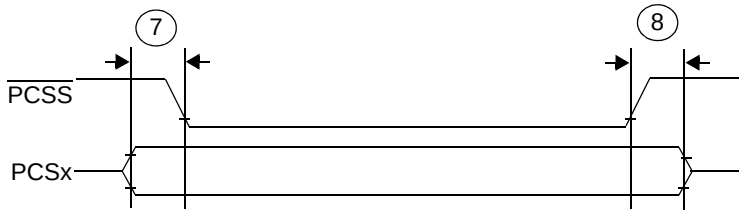
Symbol		C	Parameter	Conditions		Typical value(2)	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	Bitrate: 500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL at 8 MHz used as CAN engine clock source – Message sending period is 580 µs	8 * f_{periph} + 85	µA
				Bitrate: 125 Kbyte/s		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: – eMIOS channel OFF – Global prescaler enabled		29 * f_{periph}	µA
				Dynamic consumption: – It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: – LIN mode – Baudrate: 20 Kbyte/s		5 * f_{periph} + 31	µA
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		16 * f_{periph}	
I_{DD_BV} (ADC_0/ADC_1)	CC	T	ADC_0/ADC_1 supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)(3)	41 * f_{periph}	µA
					Ballast dynamic consumption (continuous conversion)(3)	46 * f_{periph}	
$I_{DD\_HV\_ADC0}$	CC	T	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	3	mA
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
					Analog dynamic consumption (continuous conversion)	4	mA

Figure 29. DSPI modified transfer format timing — slave, CPHA = 1



Note: Numbers shown reference *Table 47*.

Figure 30. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



Note: Numbers shown reference *Table 47*.

4.18.3 Nexus characteristics

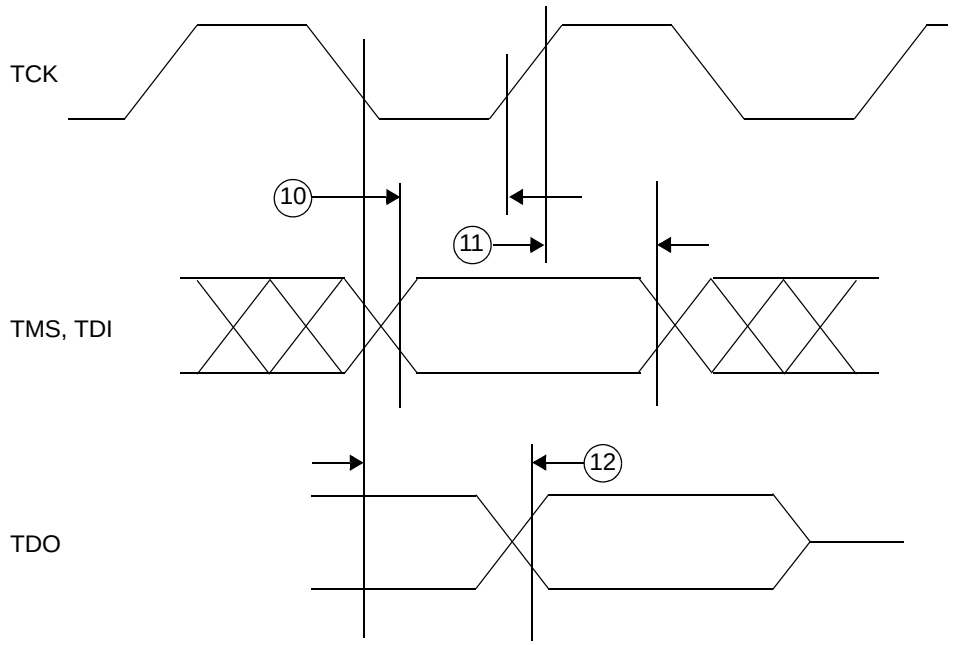
Table 49. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns

Table 49. Nexus characteristics (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
6	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

Figure 31. Nexus TDI, TMS, TDO timing



Note: Numbers shown reference *Table 49*.

Table 53. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.