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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	149
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b64l7b6e0x

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Figure 4. LQFP100 pin configuration

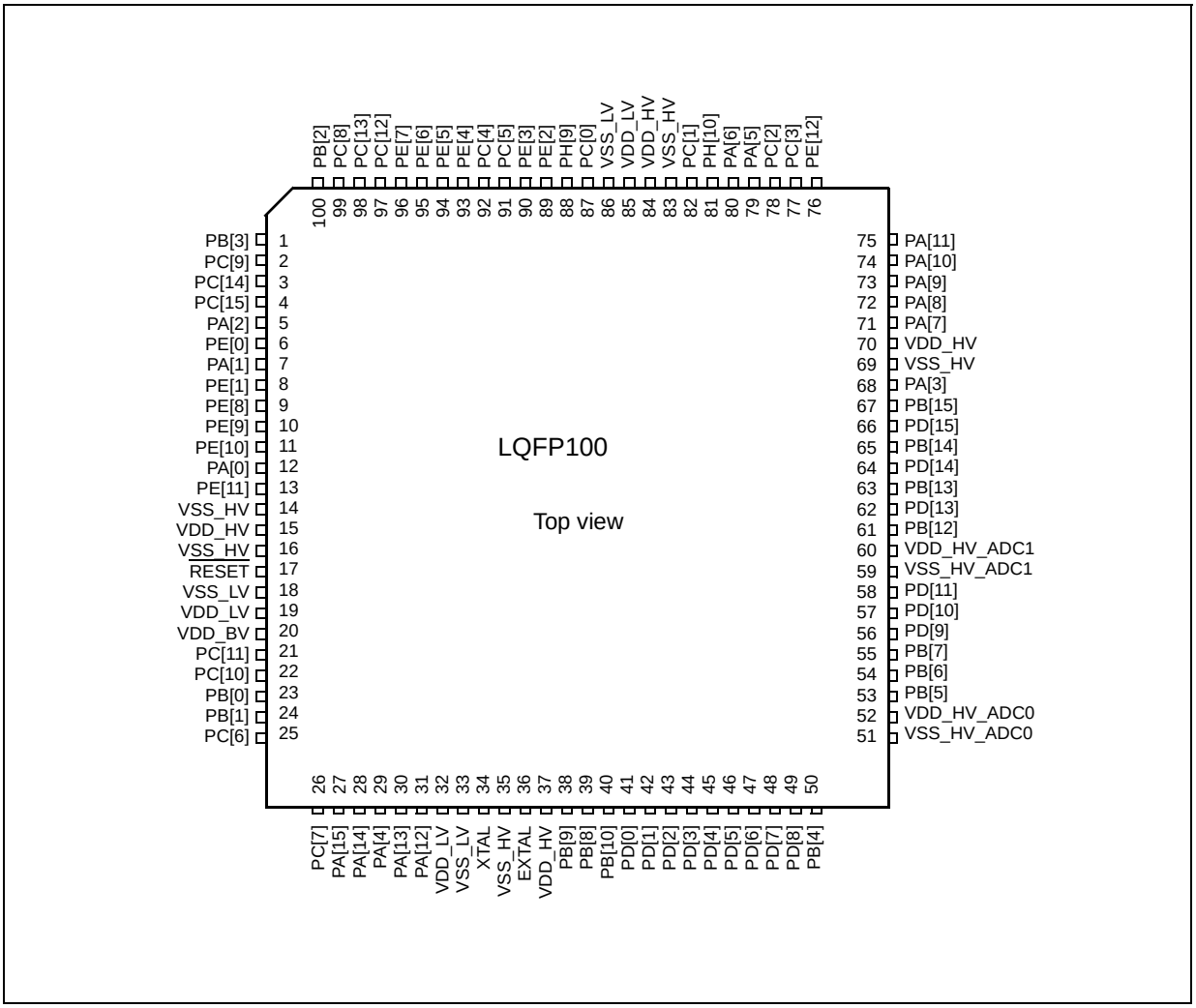


Figure 5 shows the SPC560B54/6x in the LBGA208 package.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC_0	I/O I/O I/O O	M	Tristate	94	133	161	C6
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	95	139	167	B5
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	96	140	168	C4
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	13	21	G2
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7][5] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	10	14	22	G1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PI[5]	PCR[133]	AF0 AF1 AF2 AF3	GPIO[133] E1UC[29] SCK_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O I/O —	S	Tristate	—	—	142	C12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3	GPIO[134] E1UC[30] CS0_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O I/O —	S	Tristate	—	—	11	D2
PI[7]	PCR[135]	AF0 AF1 AF2 AF3	GPIO[135] E1UC[31] CS1_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	12	D3
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	108	J13
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	109	J14

4.5 Thermal characteristics

4.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in *Table 15* LQFP thermal characteristics, considering a thermal resistance of LQFP144 as 48.3 °C/W, at ambient temperature T_A = 125 °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than (150 – 125)/48.3 = 517 mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD\_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD\_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD\_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in *Section 4.5.2: Package thermal characteristics*, it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD\_BV}) < 80$ mA, then no resistor is required.
- If 80 mA < $I_{DD}(V_{DD\_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD\_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV}. For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD\_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD\_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 ms/V. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage detector (LVD) generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD\_BV})$ possible across the external resistor.

4.5.2 Package thermal characteristics

Table 15. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection(3)	Single-layer board — 1s	100	—	—	64	°C/W
					144	—	—	64	
					176	—	—	64	
				Four-layer board — 2s2p	100	—	—	49.7	
					144	—	—	48.3	
					176	—	—	47.3	

Table 18. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

Table 23. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 24 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 24. I/O weight(1)

Supply segment			Pad	LQFP176				LQFP144/100			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 176	LQFP 144	LQFP 100		SRC(2) = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PB[3]	5%	—	6%	—	13%	—	15%	—
			PC[9]	4%	—	5%	—	13%	—	15%	—
			PC[14]	4%	—	4%	—	13%	—	15%	—
			PC[15]	3%	4%	4%	4%	12%	18%	15%	16%
	—	—	PJ[4]	3%	4%	3%	3%	—	—	—	—
1	—	—	PH[15]	2%	3%	3%	3%	—	—	—	—
	—	—	PH[13]	3%	4%	3%	4%	—	—	—	—
	—	—	PH[14]	3%	4%	4%	4%	—	—	—	—
	—	—	PI[6]	4%	—	4%	—	—	—	—	—
	—	—	PI[7]	4%	—	4%	—	—	—	—	—
	4	—	PG[5]	4%	—	5%	—	10%	—	12%	—
		—	PG[4]	4%	6%	5%	5%	9%	13%	11%	12%
		—	PG[3]	4%	—	5%	—	9%	—	11%	—
		—	PG[2]	4%	6%	5%	5%	9%	12%	10%	11%
		4	PA[2]	4%	—	5%	—	8%	—	10%	—
			PE[0]	4%	—	5%	—	8%	—	9%	—
			PA[1]	4%	—	5%	—	8%	—	9%	—
			PE[1]	4%	6%	5%	6%	7%	10%	9%	9%
			PE[8]	4%	6%	5%	6%	7%	10%	8%	9%
			PE[9]	4%	—	5%	—	6%	—	8%	—
			PE[10]	4%	—	5%	—	6%	—	7%	—
			PA[0]	4%	6%	5%	5%	6%	8%	7%	7%
			PE[11]	4%	—	5%	—	5%	—	6%	—

Table 25. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
		P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 30. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	—	years
				Blocks with 1001–10000 P/E cycles	10	—	—	years
				Blocks with 10001–100000 P/E cycles	5	—	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

Symbol		C	Parameter	Conditions(1)	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.10.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

4.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 34. EMI radiated emission measurement(1)(2)

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Figure 12. Fast external crystal oscillator (4 to 16 MHz) timing diagram

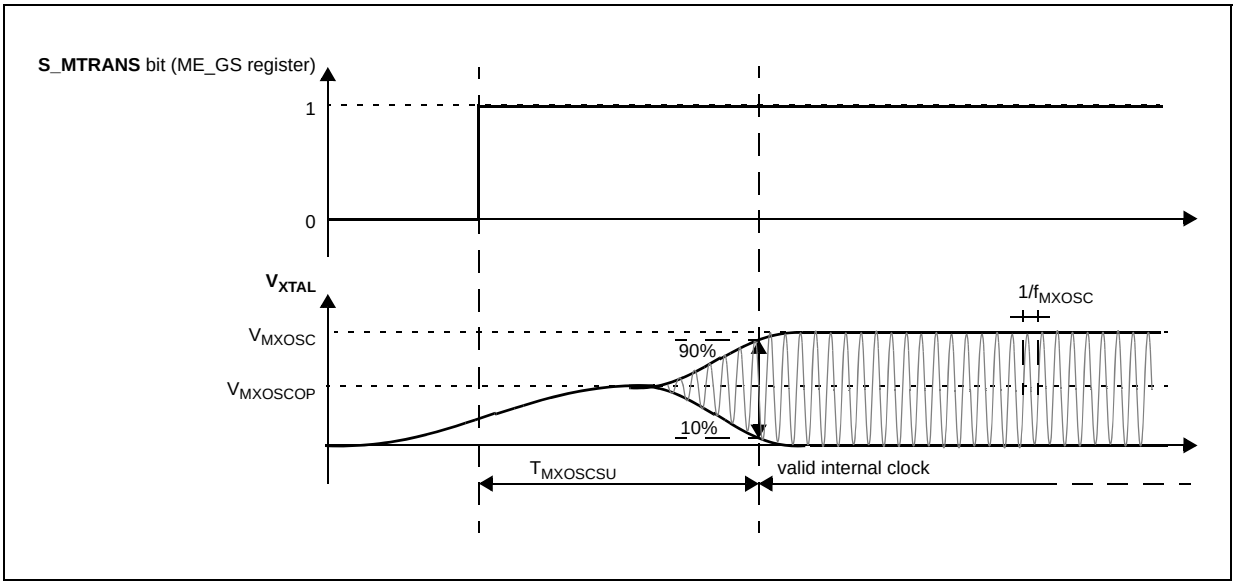


Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	C	Oscillation operating point	—	—	0.95	—	V

Figure 15. Slow external crystal oscillator (32 kHz) timing diagram

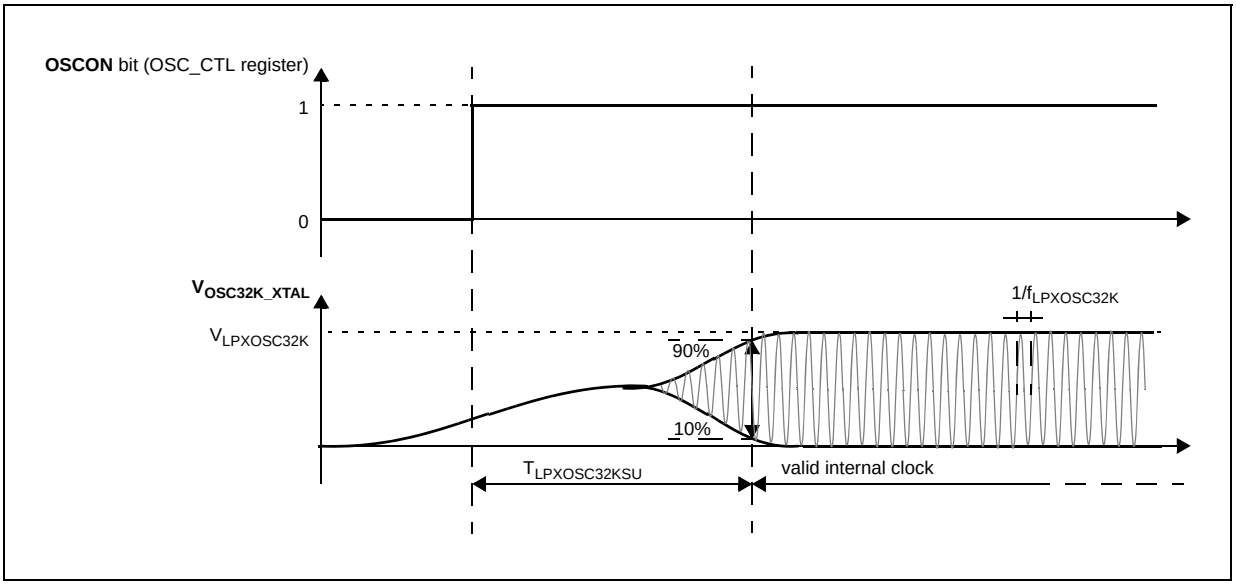


Table 40. Slow external crystal oscillator (32 kHz) electrical characteristics

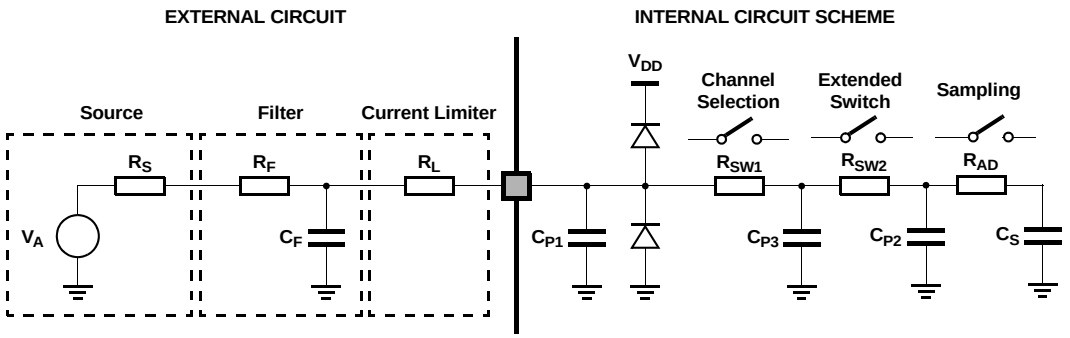
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—		2.5		µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$t_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.
2. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

4.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Figure 18. Input equivalent circuit (extended channels)



R_S Source Impedance

R_F Filter Resistance

C_F Filter Capacitance

R_L Current Limiter Resistance

R_{SW} Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})

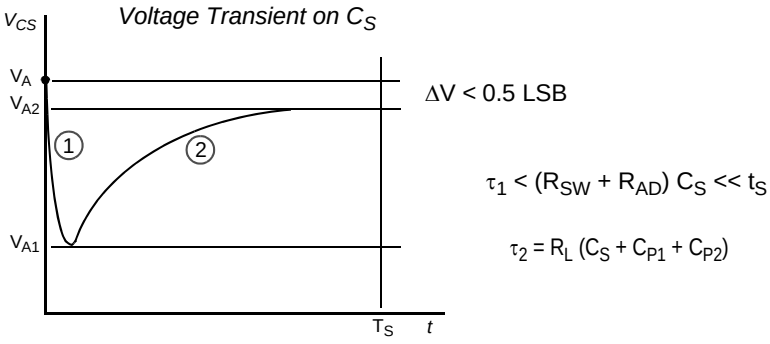
R_{AD}Sampling Switch Impedance

C_P Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})

C_S Sampling Capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 17*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 19. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

Equation 9 ADC_0 (10-bit)

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Equation 10 ADC_1 (12-bit)

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

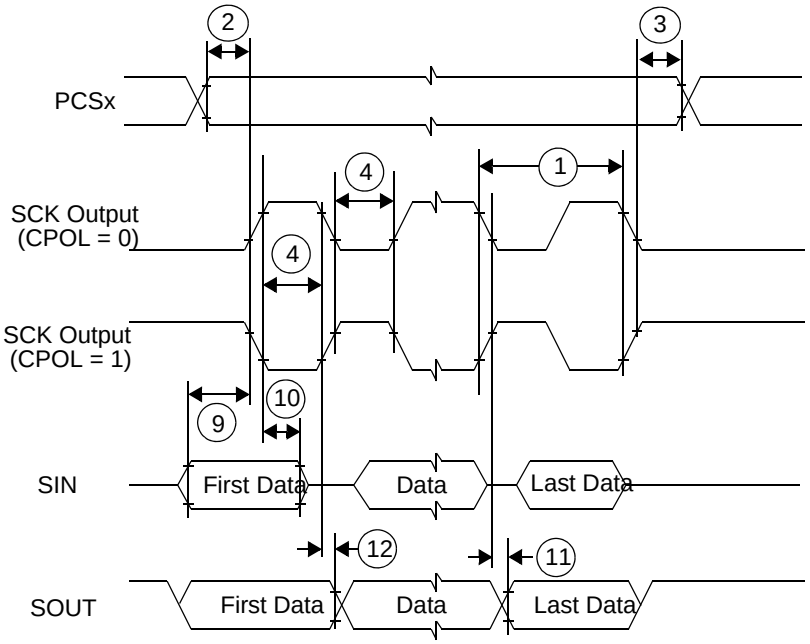
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 11* must be respected (charge balance assuming now C_S already charged at V_{A1}):

4.18.2 DSPI characteristics

Table 48. DSPI characteristics[1]

No.	Symbol		C	Parameter		DSPI0/DSPI1/DSPI3/DSPI5			DSPI2/DSPI4			Unit
						Min	Typ	Max	Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	125	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	125	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Master mode	—	—	130[2]	—	—	15[3]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Master mode	—	—	130[3]	—	—	130[3]	ns
2	t_{CSCext}[4]	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t_{ASCext}[5]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK/2}$	—	—	$t_{SCK/2}$	—	ns
		SR	D		Slave mode	$t_{SCK/2}$	—	—	$t_{SCK/2}$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	—	—	$1/f_{DSPI} + 130$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
7	t_{PCSC}	SR	D	PCSx to $\overline{PCSS}$ time	—	0	—	—	0	—	—	ns
8	t_{PASC}	SR	D	$\overline{PCSS}$ to PCSx time	—	0	—	—	0	—	—	ns

Figure 22. DSPI classic SPI timing — master, CPHA = 0



Note: Numbers shown reference *Table 47*.

5.2.2 LQFP144

Figure 34. LQFP144 package mechanical drawing

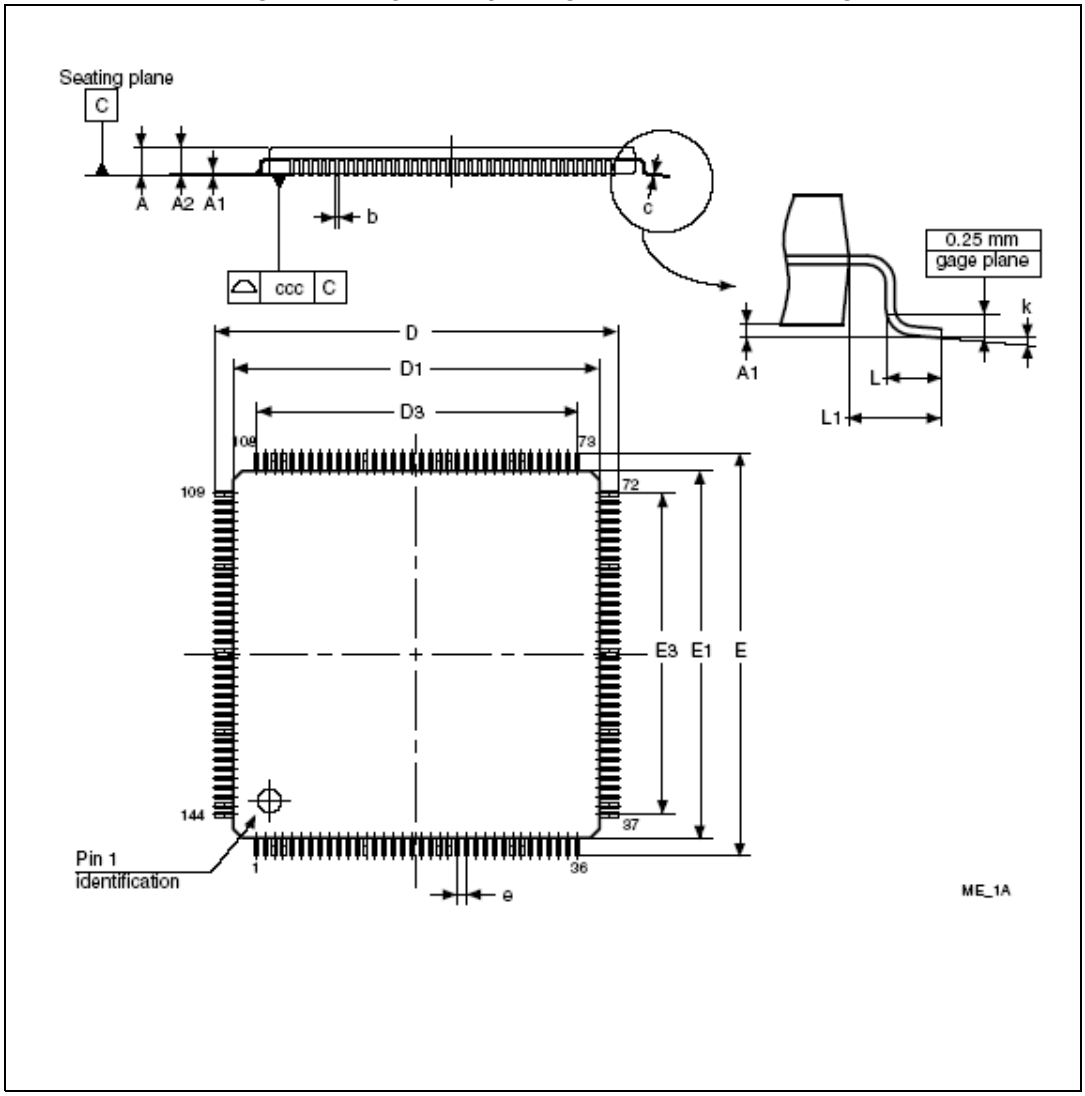


Table 52. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740

Appendix A Abbreviations

Table 55 lists abbreviations used but not defined elsewhere in this document.

Table 55. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal oxide semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Table 56. Revision history (continued)

Date	Revision	Changes
12-Sep- 2011	6	Editorial and formatting changes throughout Replaced instances of “e200z0” with “e200z0h” Device family comparison table: – added 1 MB code flash LQFP100 version – added 1.5 MB code flash LQFP144 version – removed 768 KB code flash LQFP176 version – changed LINFlex count for 144-pin LQFP—was ‘6’; is ‘8’ – changed LINFlex count for 176-pin LQFP—was ‘8’; is ‘10’ – replaced 105 °C with 125 °C in footnote 2 SPC560B54/6x block diagram: added GPIO and VREG to legend SPC560B54/6x series block summary: added acronym “JTAGC”; in WKPU function changed “up to 18 external sources” to “up to 27 external sources” LQFP144 pin configuration: for pins 37–72, restored the pin labels that existed prior to 27 July 2010 LQFP176 pin configuration: corrected name of pin 4: was EPC[15]; is PC[15] Added following sections: – Pad configuration during reset phases – Pad configuration during standby mode exit – Voltage supply pins – Pad types – System pins – Functional port pins – Nexus 2+ pins Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Tables “Absolute maximum ratings” and “Recommended operating conditions (3.3 V)”: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description “Recommended operating conditions (5.0 V)” table: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description; changed 3.6V to 3.0V in footnote 2 Section “External ballast resistor recommendations”: replaced “low voltage monitor” with “low voltage detector (LVD)” “I/O input DC electrical characteristics” table: updated I_{LKG} characteristics “MEDIUM configuration output buffer electrical characteristics” table: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O weight: updated table (includes replacing instances of bit “SRE” with “SRC”) “Reset electrical characteristics” table: updated parameter classification for $\lvert I_{WPU} \rvert$ Updated voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); changed “as well as four low voltage detectors” to “as well as five low voltage detectors”; added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$ Updated section “Power consumption”