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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	149
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b64l7c6e0x

List of figures

Table 2. SPC560B54/6x family comparison[1] (continued)

Feature	SPC560B54		SPC560B60			SPC560B64			
OPWM / ICOC[9]	13 ch	33 ch	13 ch	33 ch	33 ch	13 ch	33 ch	33 ch	33 ch
SCI (LINFlex)	4	8	4	8	10	4	8	10	10
SPI (DSPI)	3	5	3	5	6	3	5	6	6
CAN (FlexCAN)	6								
I2C	1								
32 KHz oscillator	Yes								
GPIO[10]	77	121	77	121	149	77	121	149	149
Debug	JTAG								N2+
Package	LQFP 100	LQFP 144	LQFP 100	LQFP 144	LQFP 176	LQFP 100	LQFP 144	LQFP 176	LBGA208[11]

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature.
3. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
4. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
5. See the eMIOS section of the chip reference manual for information on the channel configuration and functions.
6. Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.
7. Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.
8. Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.
9. Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.
10. Maximum I/O count based on multiplexing with peripherals.
11. LBGA208 available only as development package for Nexus2+.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	141	173	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	174	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 — EIRQ[20]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	M	Tristate	4	4	4	D3
Port D											

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	134	162	A6
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	135	163	B6
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC_0	I/O I/O — O	M	Tristate	—	136	164	D5
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	137	165	C5
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	138	166	A5
PH[9][10]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	88	127	155	B8

4.3 Absolute maximum ratings

Table 12. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV (regulator supply) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- *Table 17* provides weak pull figures. Both pull-up and pull-down resistances are supported.
- *Table 18* provides output driver characteristics for I/O pads when in SLOW configuration.
- *Table 19* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 20* provides output driver characteristics for I/O pads when in FAST configuration.

Table 17. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 18. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	

Table 18. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

Table 25. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
		P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 30. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	—	years
				Blocks with 1001–10000 P/E cycles	10	—	—	years
				Blocks with 10001–100000 P/E cycles	5	—	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

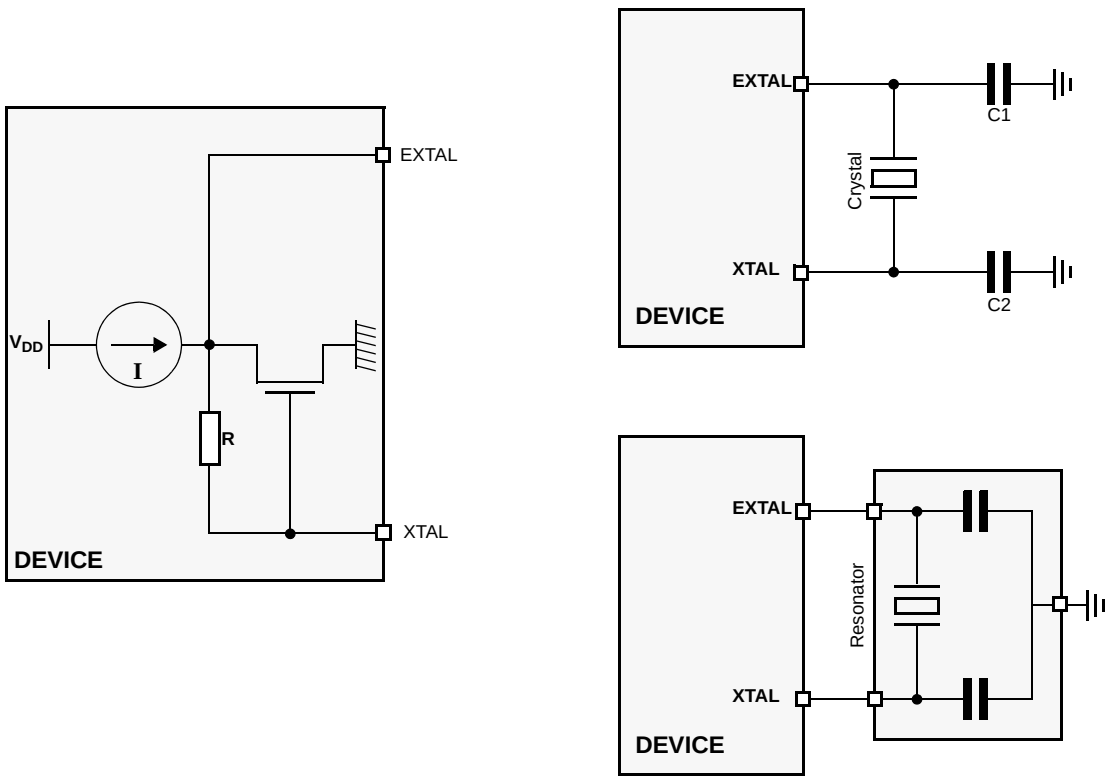
Symbol		C	Parameter	Conditions(1)	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.10.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Figure 11. Crystal oscillator and resonator connection scheme



Notes:
1. XTAL/EXTAL must not be directly used to drive external circuits
2. A series resistor may be required, according to crystal oscillator supplier recommendations.

Table 37. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)(1)	Shunt capacitance between xtalout and xtalin C0(2) (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Figure 12. Fast external crystal oscillator (4 to 16 MHz) timing diagram

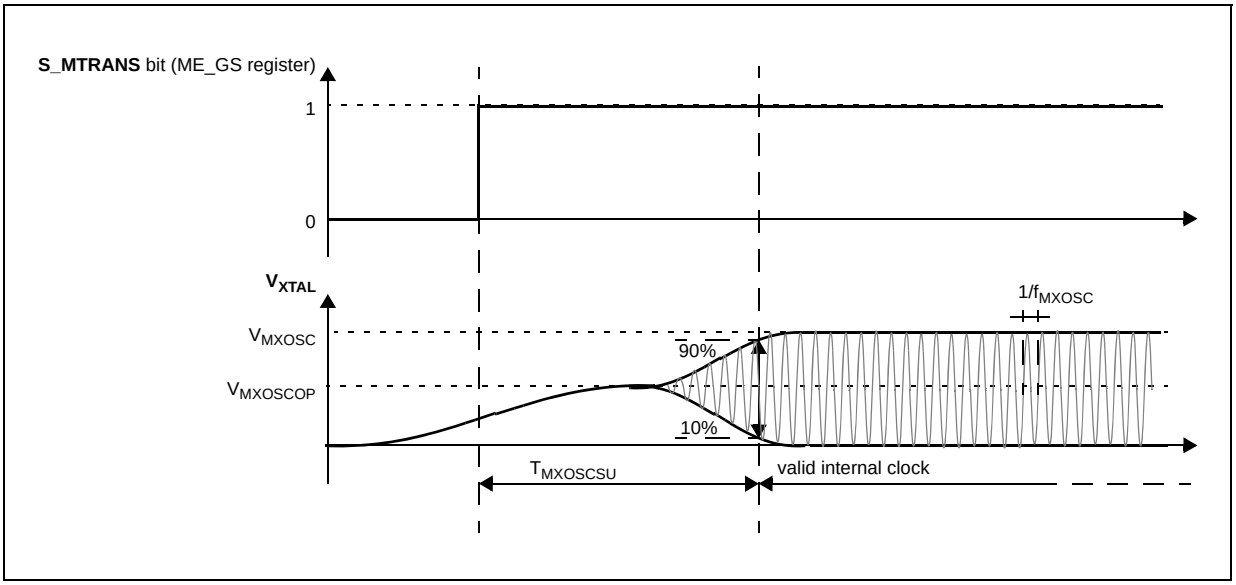


Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	C	Oscillation operating point	—	—	0.95	—	V

Table 41. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	64	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
		P	VCO frequency with frequency modulation	—	245.76	—	532.48	
f_{CPU}	SR	—	System clock frequency	—	—	—	64	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{STJIT}	CC	—	FMPLL short term jitter[4]	f_{sys} maximum	–4	—	4	%
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLCLK} at 64 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ± 4%.
4. Short term jitter is measured on the clock rising edge at cycle n and n+4.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 42. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[2]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	10	µA

Table 43. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	10	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

Figure 21. ADC_1 characteristic and error definitions

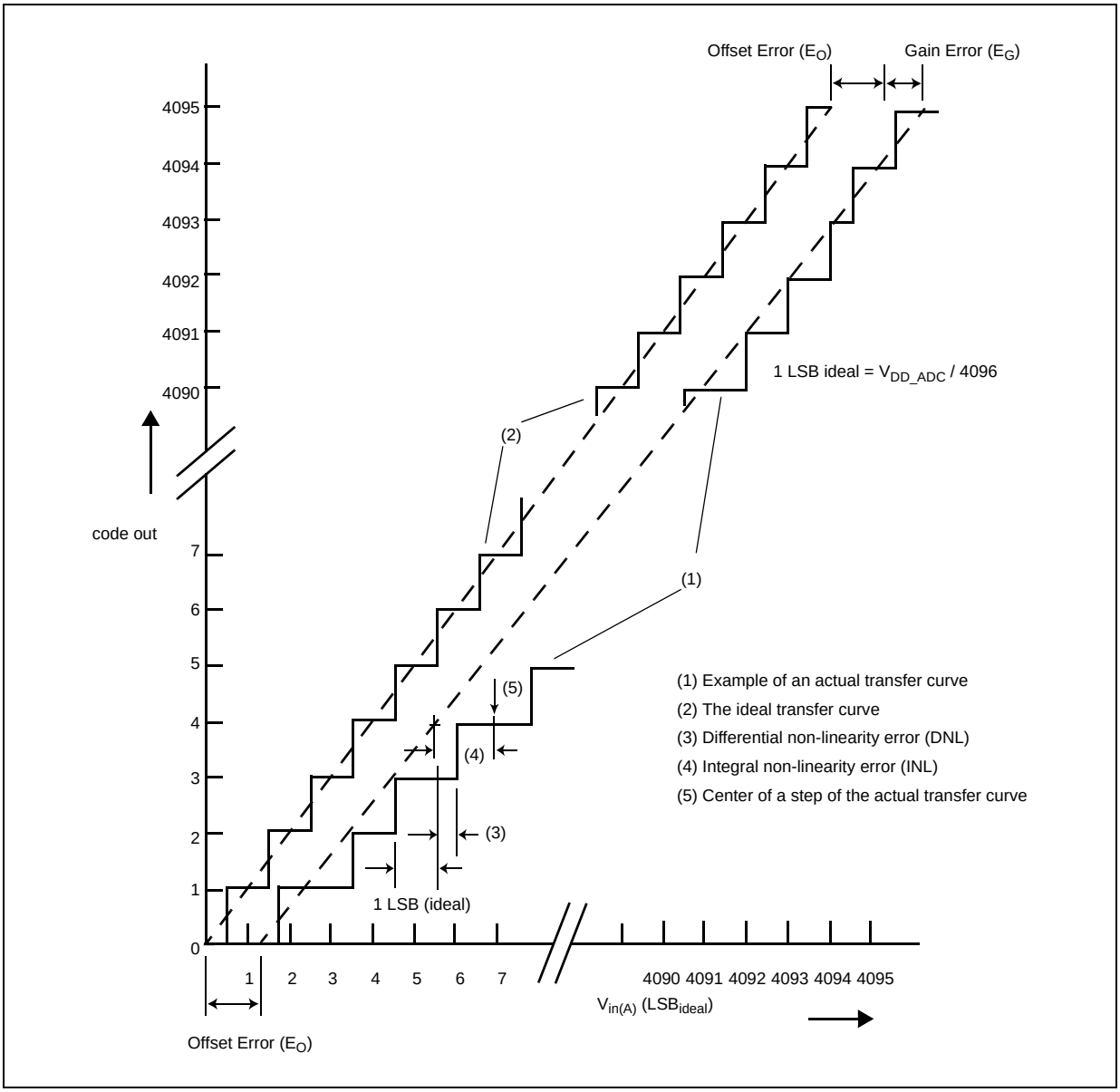


Table 46. ADC_1 conversion characteristics (12-bit ADC_1)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC1}	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC1} – 0.1	—	V_{DD_ADC1} + 0.1	V

4.18.2 DSPI characteristics

Table 48. DSPI characteristics[1]

No.	Symbol		C	Parameter		DSPI0/DSPI1/DSPI3/DSPI5			DSPI2/DSPI4			Unit
						Min	Typ	Max	Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	125	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	125	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Master mode	—	—	130[2]	—	—	15[3]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Master mode	—	—	130[3]	—	—	130[3]	ns
2	t_{CSCext}[4]	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t_{ASCext}[5]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK/2}$	—	—	$t_{SCK/2}$	—	ns
		SR	D		Slave mode	$t_{SCK/2}$	—	—	$t_{SCK/2}$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	—	—	$1/f_{DSPI} + 130$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
7	t_{PCSC}	SR	D	PCSx to $\overline{PCSS}$ time	—	0	—	—	0	—	—	ns
8	t_{PASC}	SR	D	$\overline{PCSS}$ to PCSx time	—	0	—	—	0	—	—	ns

Table 52. LQFP144 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 54. LBGA208 mechanical data (continued)

Symbol	mm			inches[1]			Notes
	Min	Typ	Max	Min	Typ	Max	
D	16.80	17.00	17.20	0.6614	0.6693	0.6772	—
D1	—	15.00	—	—	0.5906	—	—
E	16.80	17.00	17.20	0.6614	0.6693	0.6772	—
E1	—	15.00	—	—	0.5906	—	—
e	—	1.00	—	—	0.0394	—	—
F	—	1.00	—	—	0.0394	—	—
ddd	—	—	0.20	—	—	0.0079	
eee	—	—	0.25	—	—	0.0098	(4)
fff	—	—	0.10	—	—	0.0039	(5)

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   – Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   – The maximum total package height is calculated by the following methodology:
   A2 (Typ) + A1 (Typ) + $\sqrt{(A1^2 + A3^2 + A4^2}$ tolerance values)
   – Low profile: 1.20 mm < A ≤ 1.70 mm
3. The typical ball diameter before mounting is 0.60mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B.
   For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other.
   For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e.
   The axis perpendicular to datum C of each ball must lie within this tolerance zone.
   Each tolerance zone fff in the array is contained entirely in the respective zone eee above.
   The axis of each ball must lie simultaneously in both tolerance zones.

Revision history

Table 56 summarizes revisions to this document.

Table 56. Revision history

Date	Revision	Changes
12-Jan-2009	1	Initial release
07-Dec-2009	2	Updated Device Summary-added LBGA208 Part number Updated Features Replaced 27 IRQs in place of 23 ADC features External Ballast resistor support conditions Updated device summary-added 208 BGA details Updated block diagram to include WKUP Updated block diagram to include 5 ch ADC 12 -bit Updated Block summary table Updated LQFP 144, 176 and 100 pinouts. Applied new naming convention for ADC signals as ADCx_P[x] and ADCx_S[x] Section 1, “General description Updated SPC560B54/60/64 device comparison table Updated block diagram-aligned with 512k Updated block summary-aligned with 512k Section 2, “Package pinouts Updated 100,144,176,208 packages according to cut2.0 changes Added Section 3.5.1, “External ballast resistor recommendations Added NVUSRO [WATCHDOG_EN] field description Updated Absolute maximum ratings Updated LQFP thermal characteristics Updated I/O supply segments Updated Voltage regulator capacitance connection Updated Low voltage monitor electrical characteristics Updated Low voltage power domain electrical characteristics Updated DC electrical characteristics Updated Program/Erase specifications Updated Conversion characteristics (10 bit ADC) Updated FMPLL electrical characteristics Updated Fast RC oscillator electrical characteristics-aligned with SPC560B4x/B5x/C4x/C5x Updated On-chip peripherals current consumption Updated ADC characteristics and error definitions diagram Updated ADC conversion characteristics (10 bit and 12 bit) Added ADC characteristics and error definitions diagram for 12 bit ADC

Table 56. Revision history (continued)

Date	Revision	Changes
12-Sep- 2011	6	Editorial and formatting changes throughout Replaced instances of “e200z0” with “e200z0h” Device family comparison table: – added 1 MB code flash LQFP100 version – added 1.5 MB code flash LQFP144 version – removed 768 KB code flash LQFP176 version – changed LINFlex count for 144-pin LQFP—was ‘6’; is ‘8’ – changed LINFlex count for 176-pin LQFP—was ‘8’; is ‘10’ – replaced 105 °C with 125 °C in footnote 2 SPC560B54/6x block diagram: added GPIO and VREG to legend SPC560B54/6x series block summary: added acronym “JTAGC”; in WKPU function changed “up to 18 external sources” to “up to 27 external sources” LQFP144 pin configuration: for pins 37–72, restored the pin labels that existed prior to 27 July 2010 LQFP176 pin configuration: corrected name of pin 4: was EPC[15]; is PC[15] Added following sections: – Pad configuration during reset phases – Pad configuration during standby mode exit – Voltage supply pins – Pad types – System pins – Functional port pins – Nexus 2+ pins Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Tables “Absolute maximum ratings” and “Recommended operating conditions (3.3 V)”: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description “Recommended operating conditions (5.0 V)” table: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description; changed 3.6V to 3.0V in footnote 2 Section “External ballast resistor recommendations”: replaced “low voltage monitor” with “low voltage detector (LVD)” “I/O input DC electrical characteristics” table: updated I_{LKG} characteristics “MEDIUM configuration output buffer electrical characteristics” table: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O weight: updated table (includes replacing instances of bit “SRE” with “SRC”) “Reset electrical characteristics” table: updated parameter classification for $\lvert I_{WPU} \rvert$ Updated voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); changed “as well as four low voltage detectors” to “as well as five low voltage detectors”; added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$ Updated section “Power consumption”