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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	XCore
Core Size	32-Bit 8-Core
Speed	1000MIPS
Connectivity	-
Peripherals	-
Number of I/O	42
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xl208-256-tq64-i10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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2 XL208-256-TQ64 Features

► Multicore Microcontroller with Advanced Multi-Core RISC Architecture

- Eight real-time logical cores
- Core share up to 500 MIPS
 - Up to 1000 MIPS in dual issue mode
- Each logical core has:
 - Guaranteed throughput of between 1/5 and 1/8 of tile MIPS
 - 16x32bit dedicated registers
- 167 high-density 16/32-bit instructions
 - All have single clock-cycle execution (except for divide)
 - 32x32 \rightarrow 64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions

► Programmable I/O

- 42 general-purpose I/O pins, configurable as input or output
 - Up to 16 x 1bit port, 5 x 4bit port, 3 x 8bit port, 1 x 16bit port
 - 1 xCONNECT link
- Port sampling rates of up to 60 MHz with respect to an external clock
- 32 channel ends for communication with other cores, on or off-chip

Memory

- 256KB internal single-cycle SRAM for code and data storage
- 8KB internal OTP for application boot code

Hardware resources

- 6 clock blocks
- 10 timers
- 4 locks
- JTAG Module for On-Chip Debug

Security Features

• Programming lock disables debug and prevents read-back of memory contents

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- AES bootloader ensures secrecy of IP held on external flash memory
- Ambient Temperature Range
 - Commercial qualification: 0°C to 70°C
 - Industrial qualification: -40 °C to 85 °C
- Speed Grade
 - 10: 500 MIPS
- Power Consumption
 - 310 mA (typical)
- ▶ 64-pin TQFP package 0.5 mm pitch

5 Example Application Diagram



▶ see Section 11 for details on the power supplies and PCB design



ports are available. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The port logic can drive its pins high or low, or it can sample the value on its pins, optionally waiting for a particular condition. Ports are accessed using dedicated instructions that are executed in a single processor cycle. xCORE-200 IO pins can be used as *open collector* outputs, where signals are driven low if a zero is output, but left high impedance if a one is output. This option is set on a per-port basis.

Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

6.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.



A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces. xCORE-200 clock blocks optionally divide the clock input from a 1-bit port.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

6.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

6.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming





Figure 6: Switch, links and channel ends

and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, X2999.

7 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock. The initial PLL multiplication value is shown in Figure 7:

Figure 7: The initial PLL multiplier values

Oscillator	Tile	PLL Ratio	PLL s	settin	gs
Frequency	Frequency		OD	F	R
9-25 MHz	144-400 MHz	16	1	63	0

Figure 7 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, *F* and *R* must be chosen so that $0 \le R \le 63$, $0 \le F \le 4095$, $0 \le OD \le 7$, and $260MHz \le F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \le 1.3GHz$. The *OD*, *F*, and *R* values can be modified by writing to the digital node PLL configuration register.

If a large boot image is to be read in, it is faster to first load a small boot-loader that reads the large image using a faster SPI clock, for example 50 MHz or as fast as the flash device supports.

The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

8.3 Boot from SPI slave

If set to boot from SPI slave, the processor enables the three pins specified in Figure 12 and expects a boot image to be clocked in. The supported clock polarity and phase are 0/0 and 1/1.

Figure 12 SPI slave pins

	Pin	Signal	Description
	X0D00	SS	Slave Select
12:	X0D10	SCLK	Clock
oins	X0D11	MOSI	Master Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

8.4 Boot from xConnect Link

If set to boot from an xConnect Link, the processor enables its link(s) around 2 us after the boot process starts. Enabling the Link switches off the pull-down resistors on the link, drives all the TX wires low (the initial state for the Link), and monitors the RX pins for boot-traffic; they must be low at this stage. If the internal pull-down is too weak to drain any residual charge, external pull-downs of 10K may be required on those pins.

The boot-rom on the core will then:

- 1. Allocate channel-end 0.
- 2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
- 3. Input the boot image specified above, including the CRC.
- 4. Input an END control token.
- 5. Output an END control token to the channel-end received in step 2.
- 6. Free channel-end 0.
- 7. Jump to the loaded code.

The following ground pins are provided:

- PLL_AGND for PLL_AVDD
- ▶ GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 100nF 0402 for each supply pin). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §8). RST_N and must be asserted low during and after power up for 100 ns.

11.1 Land patterns and solder stencils

The package is a 64 pin Thin Quad Flat Package (TQFP) with exposed ground paddle/heat slug on a 0.5mm pitch.

The land patterns and solder stencils will depend on the PCB manufacturing process. We recommend you design them with using the IPC specifications *"Generic Requirements for Surface Mount Design and Land Pattern Standards"* IPC-7351B. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints. The mechanical drawings in Section 13 specify the dimensions and tolerances.

11.2 Ground and Thermal Vias

Vias under the heat slug into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. Typical designs could use 16 vias in a 4 \times 4 grid, equally spaced across the heat slug.

11.3 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour pressure of moisture. Example damage can include bond wire damage, die lifting, internal or external package cracks and/or delamination.

All XMOS devices are Moisture Sensitivity Level (MSL) 3 - devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from *Joint*



IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices J-STD-020 Revision D.



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12.6 Clock

Figure 2 Cloc

	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
	f	Frequency	9	25	25	MHz	
_	SR	Slew rate	0.10			V/ns	
3:	TJ(LT)	Long term jitter (pk-pk)			2	%	A
K	f(MAX)	Processor clock frequency			500	MHz	В

A Percentage of CLK period.

B Assumes typical tile and I/O voltages with nominal activity.

Further details can be found in the XS1-L Clock Frequency Control document,

12.7 xCORE Tile I/O AC Characteristics

Figure 24: I/O AC characteristics

Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

12.8 xConnect Link Performance

	Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
	B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	А, В
Figure 25:	B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
Link	B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	В
rformance	B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	В

Lin performanc

> A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

B.1 RAM base address: 0x00

This register contains the base address of the RAM. It is initialized to 0x00040000.

0x00: RAM base address

<u>_</u>	Bits	Perm	Init	Description
e.	31:2	RW		Most significant 16 bits of all addresses.
s	1:0	RO	-	Reserved

B.2 Vector base address: 0x01

Base address of event vectors in each resource. On an interrupt or event, the 16 most significant bits of the destination address are provided by this register; the least significant 16 bits come from the event vector.

0x01: Vector base address

Bits	Perm	Init	Description	
31:18	RW		The event and interrupt vectors.	
17:0	RO	-	Reserved	

B.3 xCORE Tile control: 0x02

Register to control features in the xCORE tile

Bits	Perm	Init	Description	
31:26	RO	-	Reserved	
25:18	RW	0	RGMII TX data delay value (in PLL output cycle increments)	
17:9	RW	0	RGMII TX clock divider value. TX clk rises when counter (clocked by PLL output) reaches this value and falls when counter reaches (value»1). Value programmed into this field should be actua divide value required minus 1	
8	RW	0	Enable RGMII interface periph ports	
7:6	RO	-	Reserved	
5	RW	0	Select the dynamic mode (1) for the clock divider when the clock divider is enabled. In dynamic mode the clock divider is only activated when all active threads are paused. In static mode the clock divider is always enabled.	
4	RW	0	Enable the clock divider. This divides the output of the PLL to facilitate one of the low power modes.	
3:0	RO	-	Reserved	

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0x02: xCORE Tile control



Bits	Perm	Init	Description
31:11	RO	-	Reserved
10	DRW		Address space indentifier
9	DRW		Determines the issue mode (DI bit) upon Kernel Entry after Exception or Interrupt.
8	RO		Determines the issue mode (DI bit).
7	DRW		When 1 the thread is in fast mode and will continually issue.
6	DRW		When 1 the thread is paused waiting for events, a lock or another resource.
5	RO	-	Reserved
4	DRW		1 when in kernel mode.
3	DRW		1 when in an interrupt handler.
2	DRW		1 when in an event enabling sequence.
1	DRW		When 1 interrupts are enabled for the thread.
0	DRW		When 1 events are enabled for the thread.

0x10: Debug SSR

B.13 Debug SPC: 0x11

This register contains the value of the SPC register when the debugger was called.

0x11: Debug SPC	Bits	Perm	Init	Description
	31:0	DRW		Value.

B.14 Debug SSP: 0x12

This register contains the value of the SSP register when the debugger was called.

0x12:	Bits	Perm	Init	Description
Debug SSP	31:0	DRW		Value.

B.15 DGETREG operand 1: 0x13

The resource ID of the logical core whose state is to be read.

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Ox16:
Debug
interrupt dataBitsPermInitDescription31:0DRWValue.

B.19 Debug core control: 0x18

This register enables the debugger to temporarily disable logical cores. When returning from the debug interrupts, the cores set in this register will not execute. This enables single stepping to be implemented.

0x18: Debug core control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7:0	DRW		1-hot vector defining which threads are stopped when not in debug mode. Every bit which is set prevents the respective thread from running.

B.20 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over JTAG. This is the same set of registers as the Debug Scratch registers in the xCORE tile configuration.

0x20 .. 0x27: Debug scratch

cz7: oug	Bits	Perm	Init	Description		
.tch	31:0	DRW		Value.		

B.21 Instruction breakpoint address: 0x30 .. 0x33

This register contains the address of the instruction breakpoint. If the PC matches this address, then a debug interrupt will be taken. There are four instruction breakpoints that are controlled individually.

0x30 .. 0x33: Instruction breakpoint address

ion bint	Bits	Perm	Init	Description		
ess	31:0	DRW		Value.		

36

B.22 Instruction breakpoint control: 0x40 .. 0x43

This register controls which logical cores may take an instruction breakpoint, and under which condition.

Bits	Perm	Init	Description	
31:24	RO	-	Reserved	
23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.	
15:2	RO	-	Reserved	
1	DRW	0	When 0 break when PC == IBREAK_ADDR. When 1 = break wher PC != IBREAK_ADDR.	
0	DRW	0	When 1 the instruction breakpoint is enabled.	

0x40 .. 0x43: Instruction breakpoint control

B.23 Data watchpoint address 1: 0x50 .. 0x53

This set of registers contains the first address for the four data watchpoints.

0x50 .. 0x53: Data watchpoint address 1

Data point	Bits	Perm	Init	Description
ess 1	31:0	DRW		Value.

B.24 Data watchpoint address 2: 0x60 .. 0x63

This set of registers contains the second address for the four data watchpoints.

0x60 .. 0x63: Data watchpoint address 2

Data npoint	Bits	Perm	Init	Description
ress 2	31:0	DRW		Value.

B.25 Data breakpoint control register: 0x70 .. 0x73

This set of registers controls each of the four data watchpoints.

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C Tile Configuration

The xCORE Tile control registers can be accessed using configuration reads and writes (use write_tile_config_reg(tileref, ...) and read_tile_config_reg(tileref, \rightarrow ...) for reads and writes).

Number	Perm	Description	
0x00	CRO	Device identification	
0x01	CRO	xCORE Tile description 1	
0x02	CRO	xCORE Tile description 2	
0x04	CRW	Control PSwitch permissions to debug registers	
0x05	CRW	Cause debug interrupts	
0x06	CRW	xCORE Tile clock divider	
0x07	CRO	Security configuration	
0x20 0x27	CRW	Debug scratch	
0x40	CRO	PC of logical core 0	
0x41	CRO	PC of logical core 1	
0x42	CRO	PC of logical core 2	
0x43	CRO	PC of logical core 3	
0x44	CRO	PC of logical core 4	
0x45	CRO	PC of logical core 5	
0x46	CRO	PC of logical core 6	
0x47	CRO	PC of logical core 7	
0x60	CRO	SR of logical core 0	
0x61	CRO	SR of logical core 1	
0x62	CRO	SR of logical core 2	
0x63	CRO	SR of logical core 3	
0x64	CRO	SR of logical core 4	
0x65	CRO	SR of logical core 5	
0x66	CRO	SR of logical core 6	
0x67	CRO	SR of logical core 7	

Figure 31: Summary

C.1 Device identification: 0x00

This register identifies the xCORE Tile

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0x04: Control PSwitch permissions to debug registers

Bits	Perm	Init	Description	
31	CRW	0	When 1 the PSwitch is restricted to RO access to all CRW registers from SSwitch, XCore(PS_DBG_Scratch) and JTAG	
30:1	RO	-	Reserved	
0	CRW	0	When 1 the PSwitch is restricted to RO access to all CRW registers from SSwitch	

C.5 Cause debug interrupts: 0x05

This register can be used to raise a debug interrupt in this xCORE tile.

0x05: Cause debug interrupts

Bits	Perm	Init	Description	
31:2	RO	-	Reserved	
1	CRW	0	1 when the processor is in debug mode.	
0	CRW	0	Request a debug interrupt on the processor.	

C.6 xCORE Tile clock divider: 0x06

This register contains the value used to divide the PLL clock to create the xCORE tile clock. The divider is enabled under control of the tile control register

0x06: xCORE Tile clock divider

Bits	Perm	Init	Description	
31	CRW	0	Clock disable. Writing '1' will remove the clock to the tile.	
30:16	RO	-	Reserved	
15:0	CRW	0	Clock divider.	

C.7 Security configuration: 0x07

Copy of the security register as read from OTP.

C.24 SR of logical core 7: 0x67

Value of the SR of logical core 7

0x67				
SR of logical	Bits	Perm	Init	Description
core 7	31:0	CRO		Value.



Bits	Perm	Init	Description
31:28	RW	0	The direction for packets whose dimension is F.
27:24	RW	0	The direction for packets whose dimension is E.
23:20	RW	0	The direction for packets whose dimension is D.
19:16	RW	0	The direction for packets whose dimension is C.
15:12	RW	0	The direction for packets whose dimension is B.
11:8	RW	0	The direction for packets whose dimension is A.
7:4	RW	0	The direction for packets whose dimension is 9.
3:0	RW	0	The direction for packets whose dimension is 8.

0x0D: Directions 8-15

D.12 Reserved: 0x10

Reserved.

	31
0x10:	
Reserved	

В	Bits	Perm	Init	Description
31	1:2	RO	-	Reserved
	1	RW	0	Reserved.
	0	RW	0	Reserved.

D.13 Reserved.: 0x11

Reserved.

0x11: Reserved.

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Reserved.
0	RW	0	Reserved.

D.14 Debug source: 0x1F

Contains the source of the most recent debug event.

The RST_N net should be open-drain, active-low, and have a pull-up to VDDIO.

E.3 Full xSYS header

For a full xSYS header you will need to connect the pins as discussed in Section E.2, and then connect a 2-wire xCONNECT Link to the xSYS header. The links can be found in the Signal description table (Section 4): they are labelled XL0, XL1, etc in the function column. The 2-wire link comprises two inputs and outputs, labelled ${}^{1}_{out}$, ${}^{0}_{out}$, ${}^{0}_{in}$, and ${}^{1}_{in}$. For example, if you choose to use XL0 for xSCOPE I/O, you need to connect up XL0 ${}^{1}_{out}$, XL0 ${}^{0}_{out}$, XL0 ${}^{1}_{in}$, as follows:

- XL0¹_{out} (X0D43) to pin 6 of the xSYS header with a 33R series resistor close to the device.
- XL0⁰_{out} (X0D42) to pin 10 of the xSYS header with a 33R series resistor close to the device.
- > XLO_{in}^{0} (X0D41) to pin 14 of the xSYS header.
- > XLO_{in}^{1} (X0D40) to pin 18 of the xSYS header.

F.5 Boot

- □ The device is connected to a QSPI flash for booting, connected to X0D01, X0D04..X0D07, and X0D10 (Section 8). If not, you must boot the device through OTP or JTAG, or set it to boot from SPI and connect a SPI flash.
- ☐ The Flash that you have chosen is supported by **xflash**, or you have created a specification file for it.

F.6 JTAG, XScope, and debugging

- \Box You have decided as to whether you need an XSYS header or not (Section E)
- □ If you have not included an XSYS header, you have devised a method to program the SPI-flash or OTP (Section E).

F.7 GPIO

- \Box You have not mapped both inputs and outputs to the same multi-bit port.
- Pins X0D04, X0D05, X0D06, and X0D07 are output only and are, during and after reset, pulled high and low appropriately (Section 8)

F.8 Multi device designs

Skip this section if your design only includes a single XMOS device.

- \Box One device is connected to a QSPI or SPI flash for booting.
- Devices that boot from link have, for example, X0D06 pulled high and have link XL0 connected to a device to boot from (Section 8).