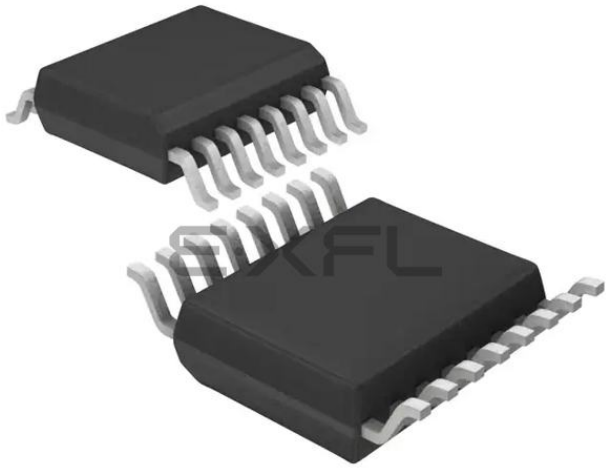

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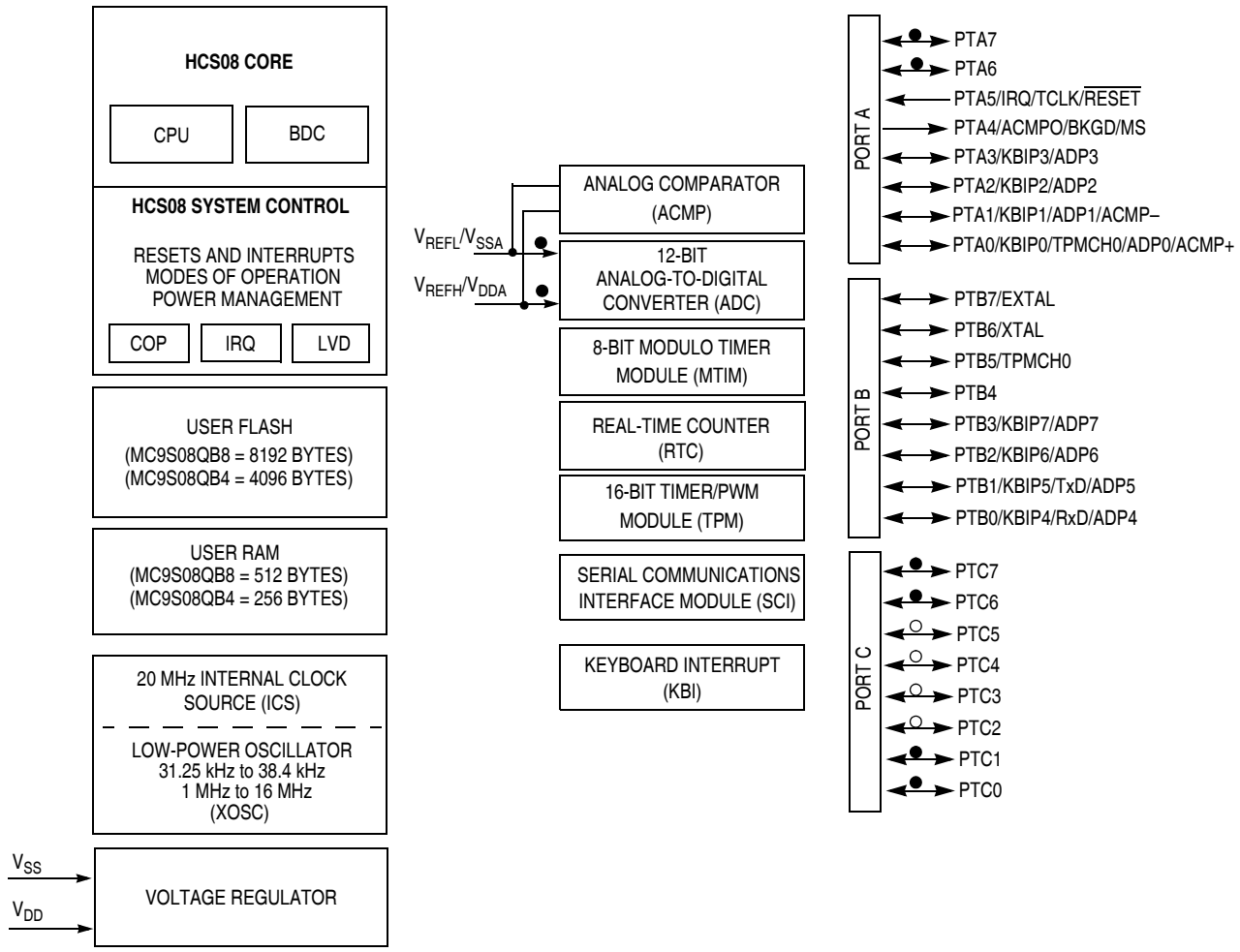
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI
Peripherals	LVD, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qb8ctg

1 MCU Block Diagram

The block diagram shows the structure of the MC9S08QB8 MCU.

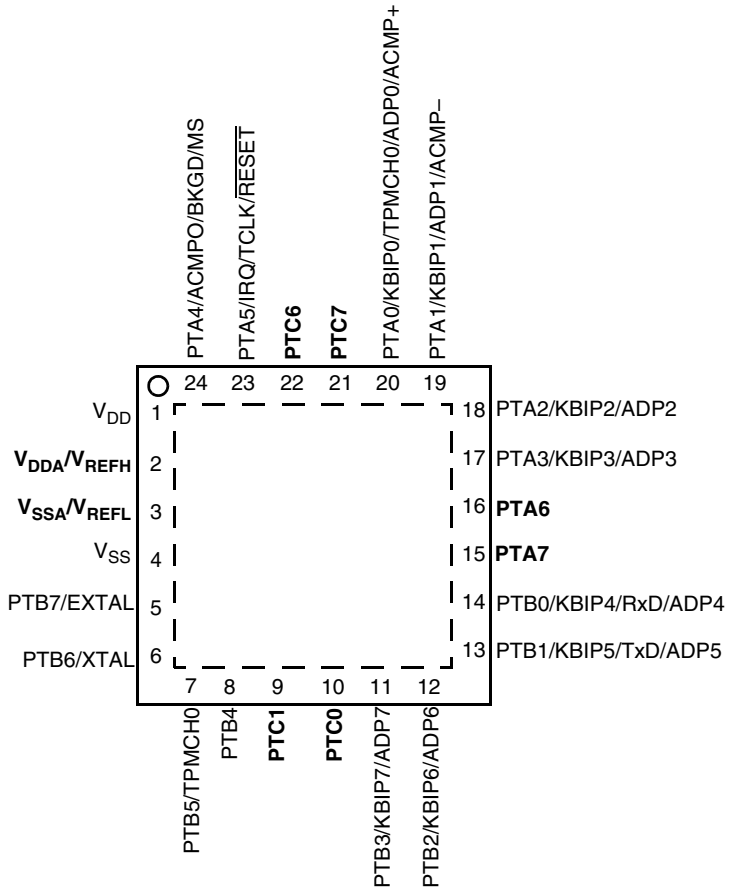


○ pins not available on 24-pin or 16-pin packages

● pins not available on 16-pin package

[1] V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL} are double bonded to V_{DD} and V_{SS} respectively in16-pin package.

Figure 1. MC9S08QB8 Series Block Diagram



Pins shown in bold type are lost in the next lower pin count package.

Figure 3. MC9S08QB8 Series in 24-Pin QFN Packages

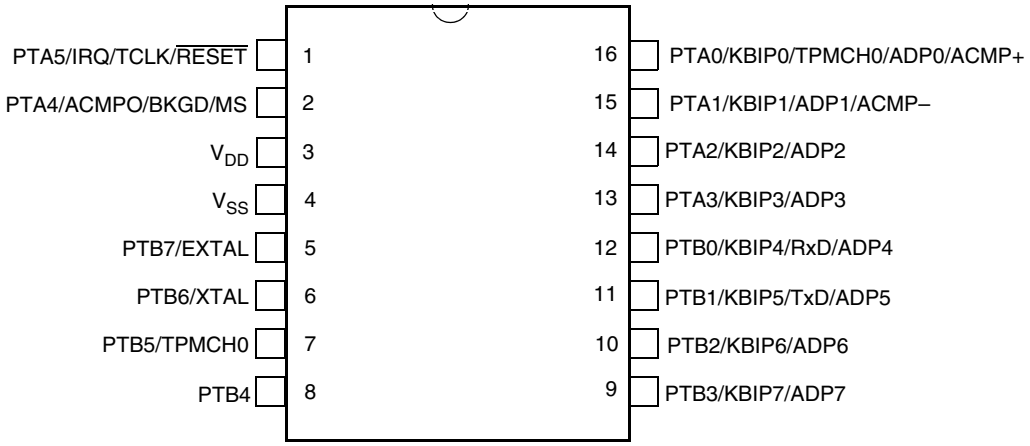


Figure 4. MC9S08QB8 Series in 16-Pin TSSOP Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9S08QB8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance 28-pin SOIC	θ_{JA}	70	°C/W
Thermal resistance 24-pin QFN		92	°C/W
Thermal resistance 16-pin TSSOP		129	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typical[1]	Max	Unit
1	P	Operating Voltage		V_{DD}	—	1.8	—	3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	V_{OUT} < V_{DD}	0	—	–80	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	V_{OUT} > V_{SS}	0	—	80	mA
6	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis	all digital inputs	V_{hys}	—	0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	all input only pins (Per pin)	$\|I_{In}\|$	V_{In} = V_{DD} or V_{SS}	—	—	200	nA
10	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\|I_{OZ}\|$	V_{In} = V_{DD} or V_{SS}	—	—	200	nA

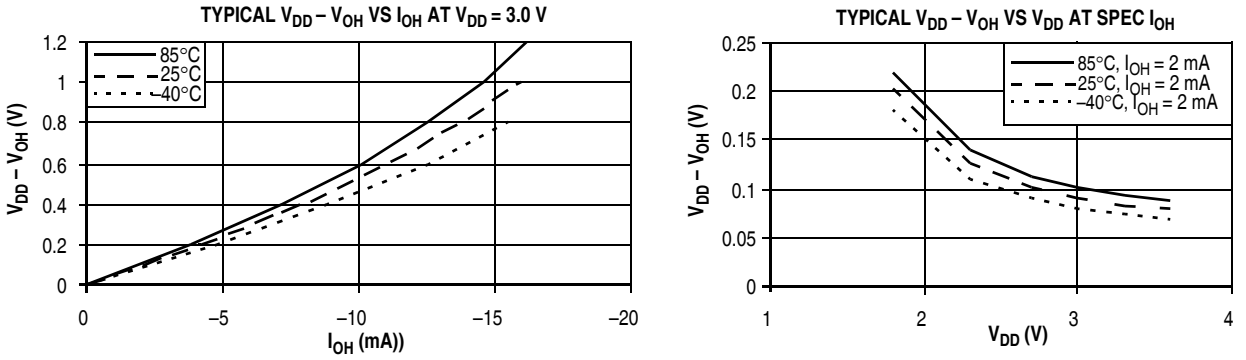


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

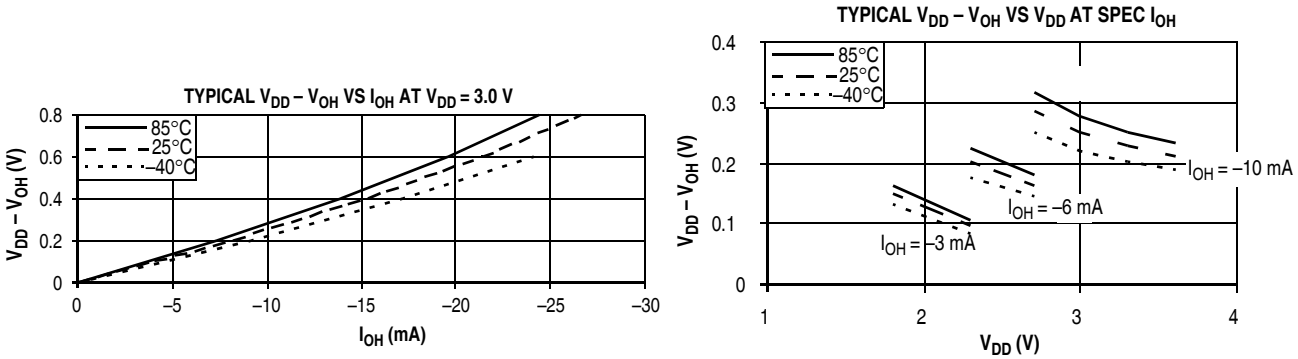


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	10 MHz	3	5.60	6	mA	–40 to 85°C
	T			1 MHz		0.80	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	3	3.60	—	mA	–40 to 85°C
	T			1 MHz		0.75	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3	165	—	µA	–40 to 85°C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off	RI_{DD}	16 kHz FBELP	3	7.3	—	µA	–40 to 85°C
5	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	10 MHz	3	570	—	µA	–40 to 85°C
	T			1 MHz		290	—		
6	T	Wait mode supply current LPRS = 1, all mods off	WI_{DD}	16 kHz FBELP	3	1	—	µA	–40 to 85°C
7	P	Stop2 mode supply current	$S2I_{DD}$	—	3	0.25	0.65	µA	–40 to 25°C
	C			—		0.5	0.8		70°C
	P			—		1	2		85°C
	C			—	2	0.2	0.5		–40 to 25°C
	C			—		0.3	0.6		70°C
	C			—		0.7	1.6		85°C
8	P	Stop3 mode supply current no clocks active	$S3I_{DD}$	—	3	0.45	0.80	µA	–40 to 25°C
	C			—		1	1.8		70°C
	P			—		3	5.8		85°C
	C			—	2	0.3	0.6		–40 to 25°C
	C			—		0.8	1.5		70°C
	C			—		2.5	5.0		85°C

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	**25**°C	**70**°C	**85**°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	µA

Table 9. Stop Mode Adders (continued)

Num	C	Parameter	Condition	Temperature				Units
				–40°C	25°C	70°C	85°C	
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	µA

[1] Not available in stop2 mode.

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 10 and Figure 11 for crystal or resonator circuits.

Table 10. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 20 20	MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.
2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
3 See crystal or resonator manufacturer's recommendation.
4 Proper PC board layout procedures must be followed to achieve specifications.

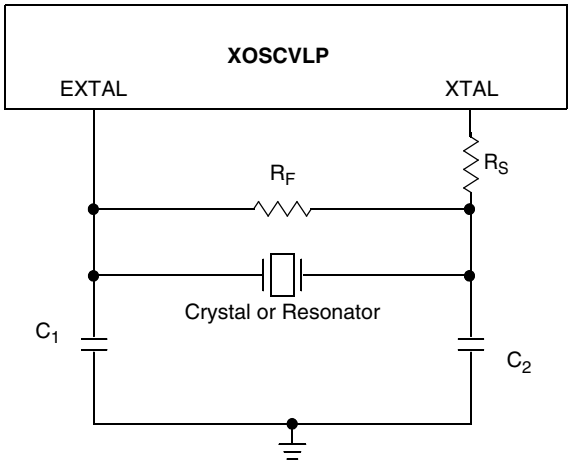


Figure 10. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

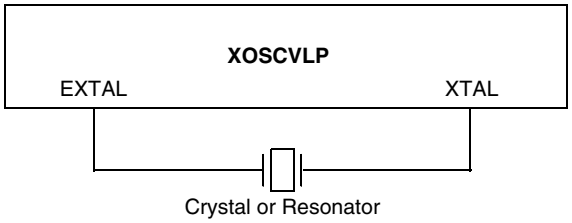


Figure 11. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C	f_{int_t}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed	f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time	t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2] — Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	f_{dco_DMX32}	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	— —	— —	ns
9	D	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	D	Voltage regulator recovery time	t_{VRR}	—	4	—	μs

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

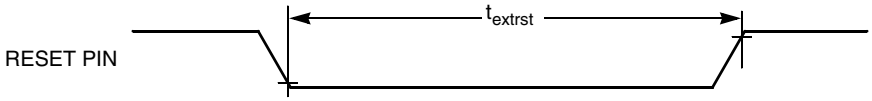


Figure 13. Reset Timing

Table 16. 12-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symbol	Min	Typical[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	202	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	288	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	T	I_{DDAD}	—	0.007	0.8	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC = 1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
	Long Sample (ADLSMP = 1)			—	40	—		
Sample Time	Short Sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP = 1)			—	23.5	—		
Total Unadjusted Error	12-bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	For 28-pin and 24-pin packages only. Includes quantization
	10-bit mode	P		—	±1	—		
	8-bit mode	T		—	±0.5	—		
Total Unadjusted Error	10-bit mode	P	E_{TUE}	—	±1.5	—	LSB[2]	For 16-pin package only. Includes quantization
	8-bit mode	T		—	±0.7	—		
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10-bit mode	P		—	±0.5	—		
	8-bit mode	T		—	±0.3	—		
	Monotonicity and No-Missing-Codes guaranteed							

Table 16. 12-Bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symbol	Min	Typical[1]	Max	Unit	Comment
Integral Non-Linearity	12-bit mode	T	INL	—	±1.5	—	LSB[2]	
	10-bit mode	C		—	±0.5	—		
	8-bit mode			—	±0.3	—		
Zero-Scale Error	12-bit mode	C	E_{ZS}	—	±1.5	—	LSB[2]	For 28-pin and 24-pin packages only. V_{ADIN} = V_{SSA}
	10-bit mode	P		—	±0.5	±1.5		
	8-bit mode	T		—	±0.5	±0.5		
Zero-Scale Error	10-bit mode	P	E_{ZS}	—	±1.5	±2.1	LSB[2]	For 16-pin package only. V_{ADIN} = V_{SSA}
	8-bit mode	T		—	±0.5	±0.7		
Full-Scale Error	12-bit mode	T	E_{FS}	—	±1	—	LSB[2]	For 28-pin and 24-pin packages only. V_{ADIN} = V_{DDA}
	10-bit mode	P		—	±0.5	±1		
	8-bit mode	T		—	±0.5	±0.5		
Full-Scale Error	10-bit mode	T	E_{FS}	—	±1	±1.5	LSB[2]	For 16-pin package only. V_{ADIN} = V_{DDA}
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	12-bit mode	D	E_Q	—	–1 to 0	—	LSB[2]	
	10-bit mode			—	—	±0.5		
	8-bit mode			—	—	±0.5		
Input Leakage Error	12-bit mode	D	E_{IL}	—	±1	—	LSB[2]	Pad leakage[3] * R_{AS}
	10-bit mode			0	±0.2	±4		
	8-bit mode			0	±0.1	±1.2		
Temp Sensor Slope	–40°C– 25°C	D	m	—	1.646	—	mV/°C	
	25°C– 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the memory section.

Table 17. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
D	Byte program time (random location)(2)	t_{prog}		9		t_{Fcyc}
D	Byte program time (burst mode)(2)	t_{Burst}		4		t_{Fcyc}
D	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
D	Mass erase time(2)	t_{Mass}		20,000		t_{Fcyc}
D	Byte program current[3]	RI_{DDBP}	—	4	—	mA
D	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25 °C	—	10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

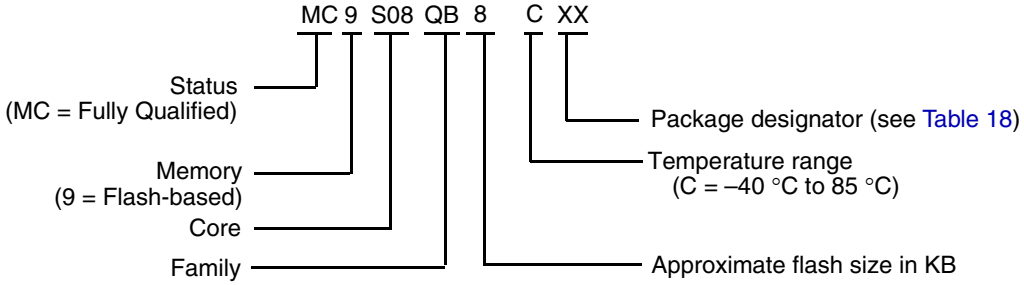
3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



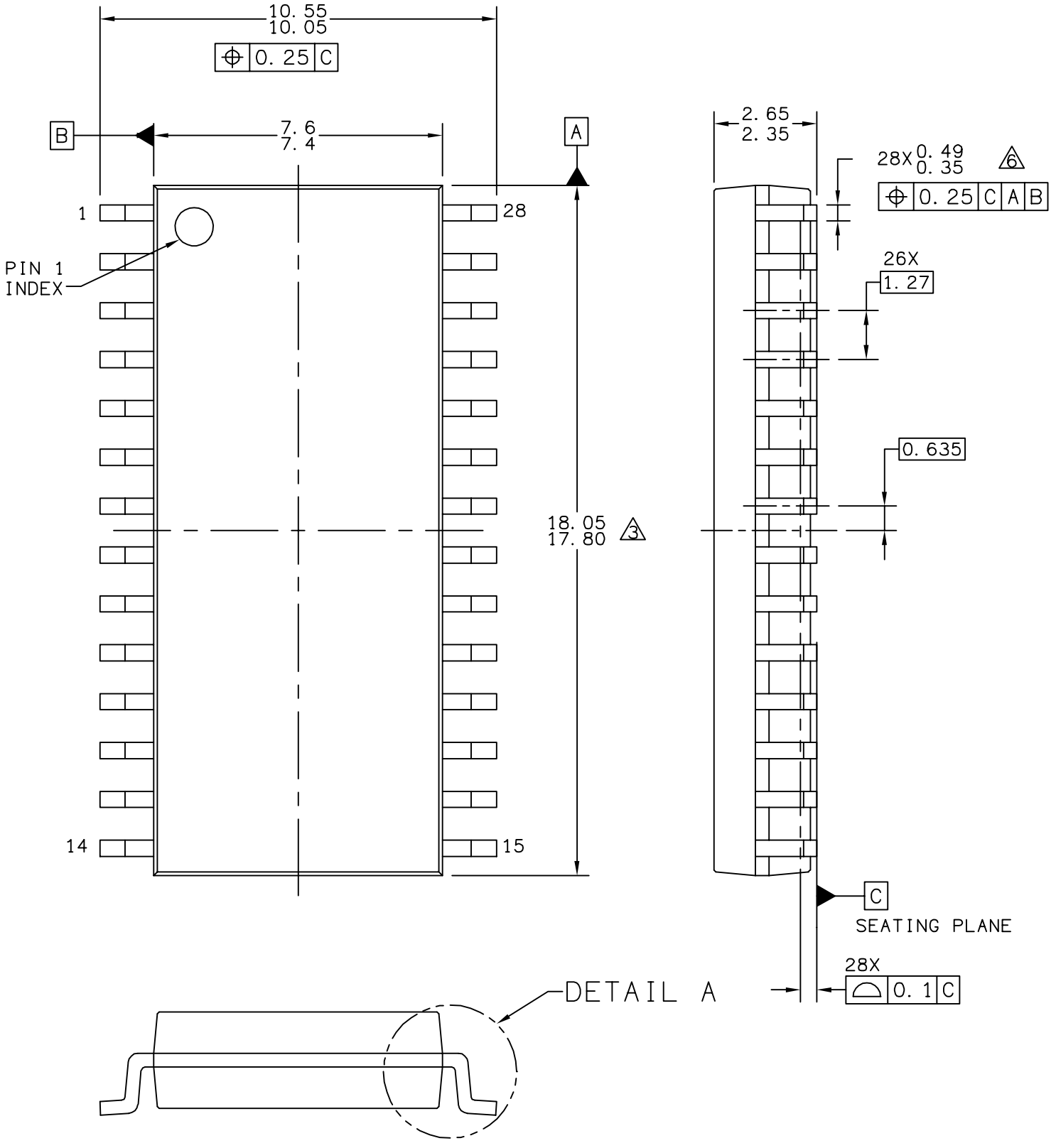
5 Package Information

Table 18. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
24	Quad Flat Non-Leaded	QFN	GK	1982-01	98ARL10608D
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 18.



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05

5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

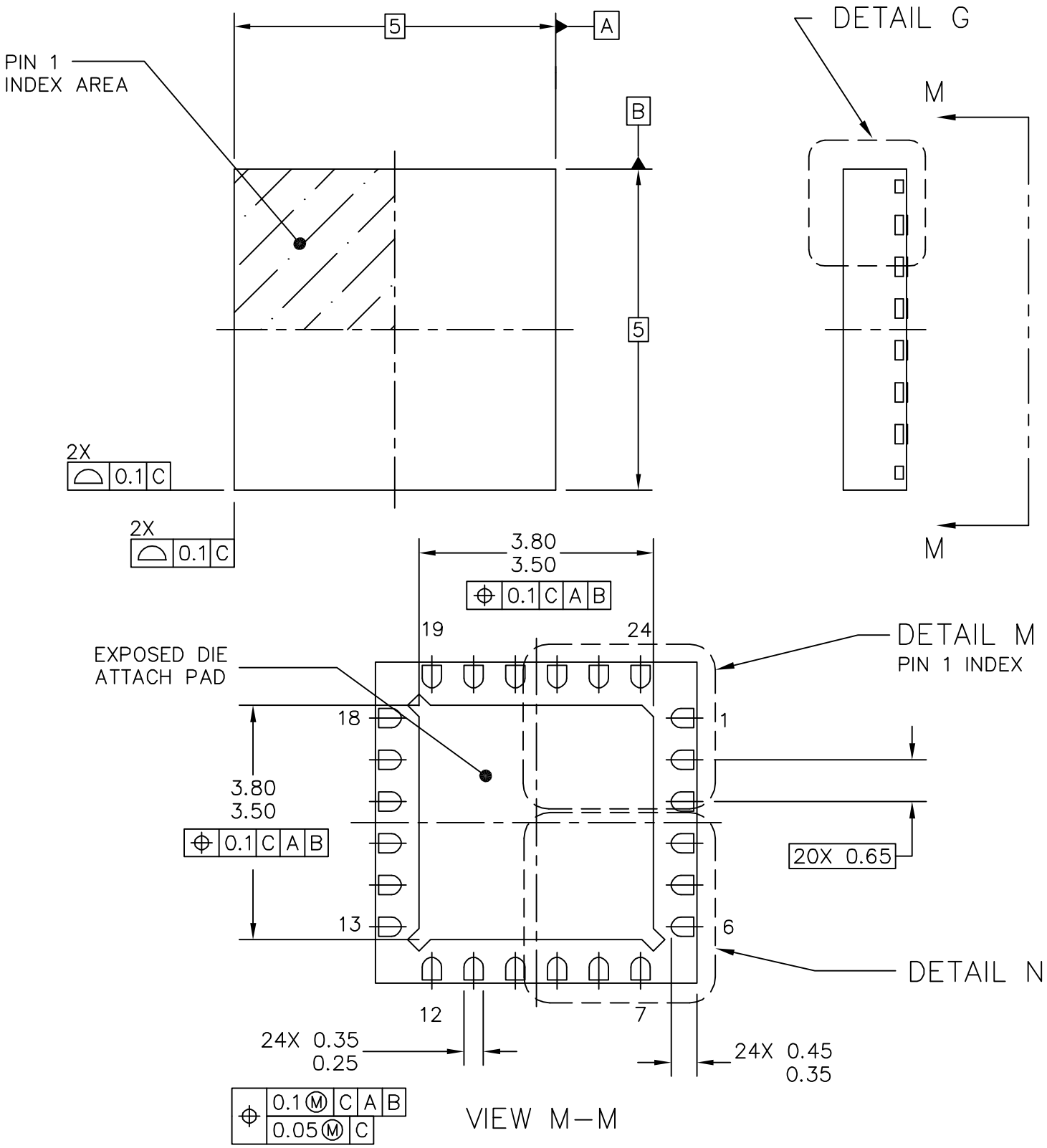
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F–05	10 MAR 2005
	STANDARD: MS–013AE	

MECHANICAL OUTLINES DICTIONARY

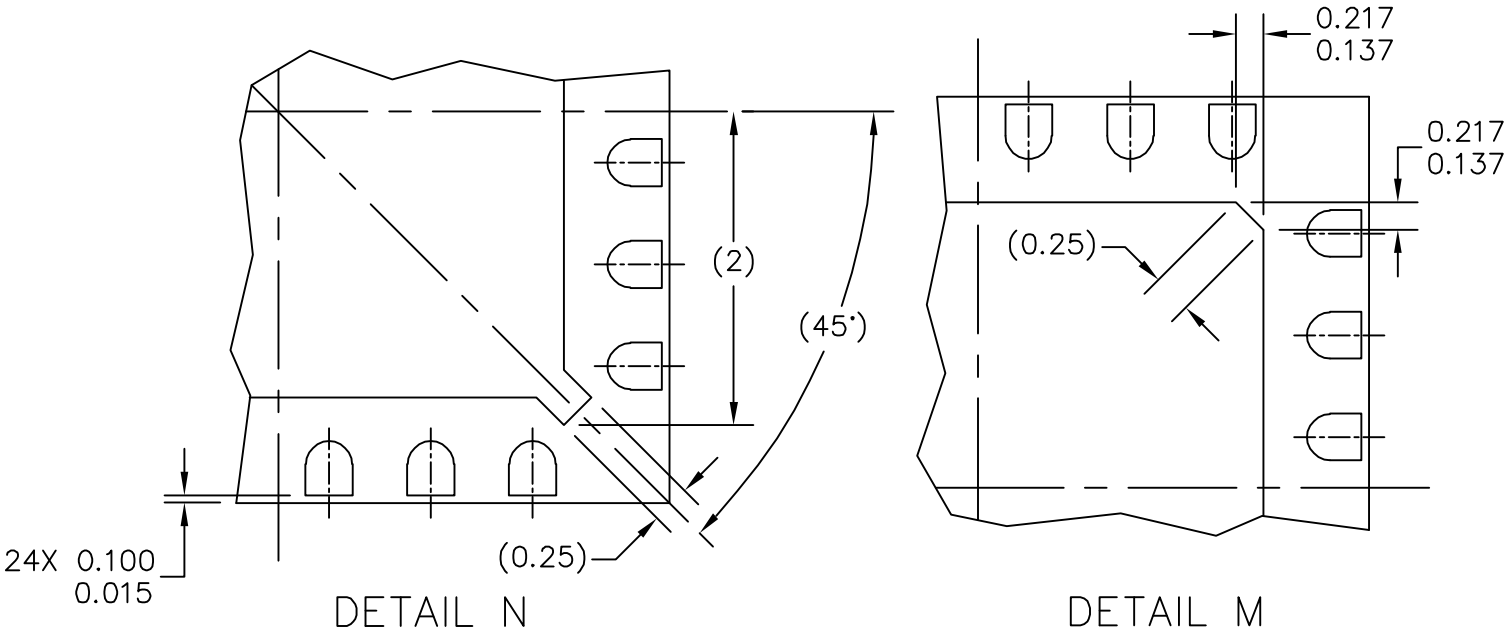
DO NOT SCALE THIS DRAWING

DOCUMENT NO: 98ARL10608D
PAGE: 1982
REV: O



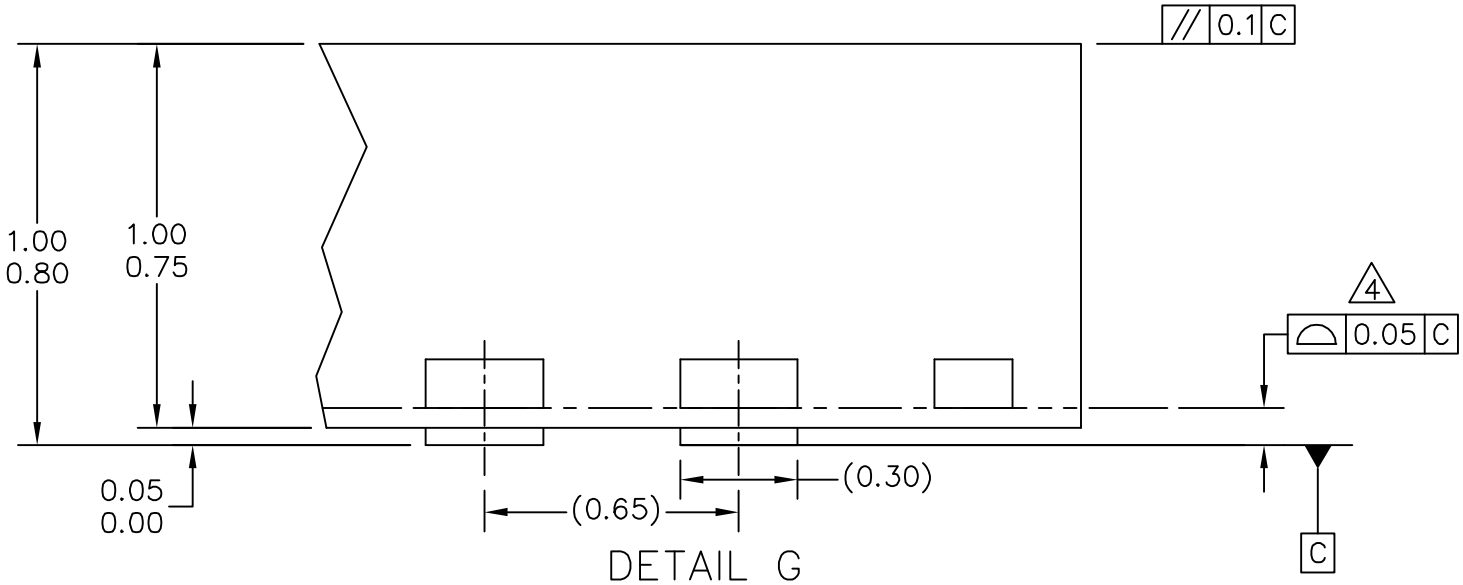
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)

CASE NUMBER: 1982–01
STANDARD: JEDEC–MO–220 VHHC–1
PACKAGE CODE: 6238
SHEET: 1 OF 4



DETAIL N
PREFERRED CORNER CONFIGURATION

DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

SEATING PLANE

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)

CASE NUMBER: 1982-01
STANDARD: JEDEC-MO-220 VHHC-1
PACKAGE CODE: 6238
SHEET: 2 OF 4

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

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