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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI
Peripherals	LVD, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qb8cwl">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qb8cwl</a>

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## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	10/22/2008	Initial public released.
2	12/17/2008	Completed all the TBDs in <a href="#">Table 8</a> .
3	3/6/2009	Corrected the 24-pin QFN package information. Changed $V_{DDAD}$ and $V_{SSAD}$ to $V_{DDA}$ and $V_{SSA}$ separately. In <a href="#">Table 7</a> , updated the $I_{IH}$ , $I_{OZ}$ and added $I_{OZTOT}$ . In <a href="#">Table 11</a> , updated the DCO output frequency range-trimmed, and updated some of the symbols.

## Related Documentation

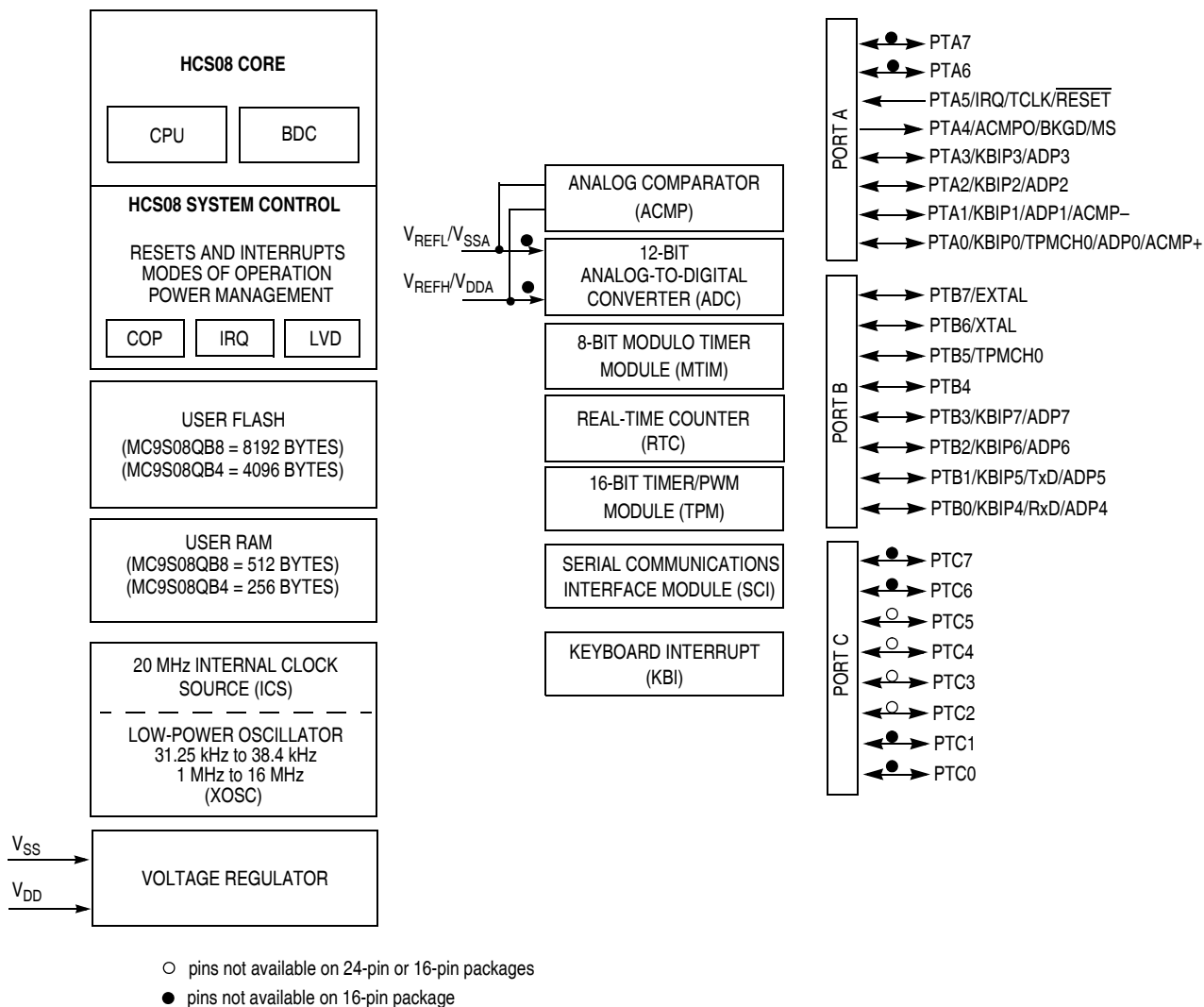
Find the most current versions of all documents at: <http://www.freescale.com>

### Reference Manual (MC9S08QB8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

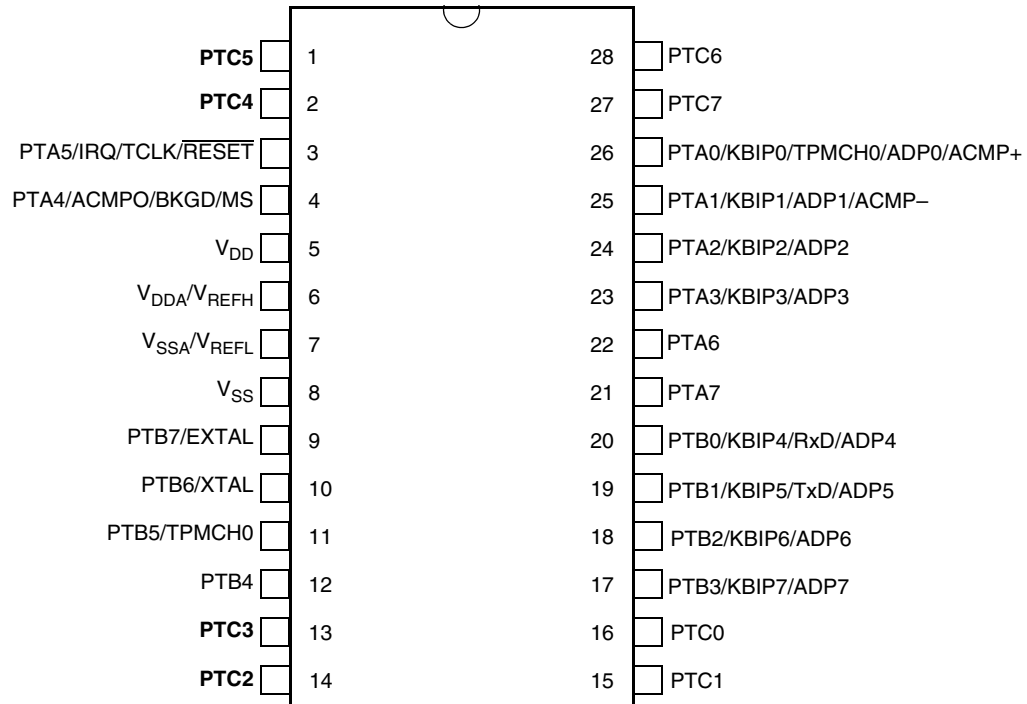
# 1 MCU Block Diagram

The block diagram shows the structure of the MC9S08QB8 MCU.



<sup>1</sup>  $V_{DDA}/V_{REFH}$  and  $V_{SSA}/V_{REFL}$  are double bonded to  $V_{DD}$  and  $V_{SS}$  respectively in 16-pin package.

**Figure 1. MC9S08QB8 Series Block Diagram**



Pins shown in bold type are lost in the next lower pin count package.

**Figure 2. MC9S08QB8 Series in 28-Pin SOIC Package**

## 3 Electrical Characteristics

### 3.1 Introduction

This chapter contains electrical and timing specifications for the MC9S08QB8 series of microcontrollers available at the time of publication.

### 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 2. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 3. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to 3.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	±25	mA
Storage temperature range	$T_{stg}$	-55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins, except for PTA5 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

### 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 4. Thermal Characteristics**

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	$T_A$	$T_L$ to $T_H$ -40 to 85	°C
Maximum junction temperature	$T_{JM}$	95	°C
Thermal resistance 28-pin SOIC	$\theta_{JA}$	70	°C/W
Thermal resistance 24-pin QFN		92	°C/W
Thermal resistance 16-pin TSSOP		129	°C/W

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{\text{HBM}}$	$\pm 2000$	—	V
2	Charge device model (CDM)	$V_{\text{CDM}}$	$\pm 500$	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{\text{LAT}}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

### 3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typical <sup>1</sup>	Max	Unit
1	P	Operating Voltage	$V_{\text{DD}}$	—	1.8	—	3.6	V
2	C	All I/O pins, low-drive strength	$V_{\text{OH}}$	$V_{\text{DD}} > 1.8 \text{ V},$ $I_{\text{Load}} = -2 \text{ mA}$	$V_{\text{DD}} - 0.5$	—	—	V
	P	Output high voltage		$V_{\text{DD}} > 2.7 \text{ V},$ $I_{\text{Load}} = -10 \text{ mA}$	$V_{\text{DD}} - 0.5$	—	—	
	C	All I/O pins, high-drive strength		$V_{\text{DD}} > 1.8 \text{ V},$ $I_{\text{Load}} = -2 \text{ mA}$	$V_{\text{DD}} - 0.5$	—	—	
3	D	Output high current Max total $I_{\text{OH}}$ for all ports	$I_{\text{OHT}}$	$V_{\text{OUT}} < V_{\text{DD}}$	0	—	-80	mA
4	C	All I/O pins, low-drive strength	$V_{\text{OL}}$	$V_{\text{DD}} > 1.8 \text{ V},$ $I_{\text{Load}} = 0.6 \text{ mA}$	—	—	0.5	V
	P	Output low voltage		$V_{\text{DD}} > 2.7 \text{ V},$ $I_{\text{Load}} = 10 \text{ mA}$	—	—	0.5	
	C	All I/O pins, high-drive strength		$V_{\text{DD}} > 1.8 \text{ V},$ $I_{\text{Load}} = 3 \text{ mA}$	—	—	0.5	
5	D	Output low current Max total $I_{\text{OL}}$ for all ports	$I_{\text{OLT}}$	$V_{\text{OUT}} > V_{\text{SS}}$	0	—	80	mA
6	P	Input high voltage	$V_{\text{IH}}$	$V_{\text{DD}} > 2.7 \text{ V}$	$0.70 \times V_{\text{DD}}$	—	—	V
	C	all digital inputs		$V_{\text{DD}} > 1.8 \text{ V}$	$0.85 \times V_{\text{DD}}$	—	—	
7	P	Input low voltage	$V_{\text{IL}}$	$V_{\text{DD}} > 2.7 \text{ V}$	—	—	$0.35 \times V_{\text{DD}}$	
	C	all digital inputs		$V_{\text{DD}} > 1.8 \text{ V}$	—	—	$0.30 \times V_{\text{DD}}$	
8	C	Input hysteresis	$V_{\text{hys}}$	—	$0.06 \times V_{\text{DD}}$	—	—	mV
9	P	Input leakage current	$I_{\text{In}}$	$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$	—	—	200	nA
10	P	Hi-Z (off-state) leakage current	$I_{\text{OZ}}$	$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$	—	—	200	nA

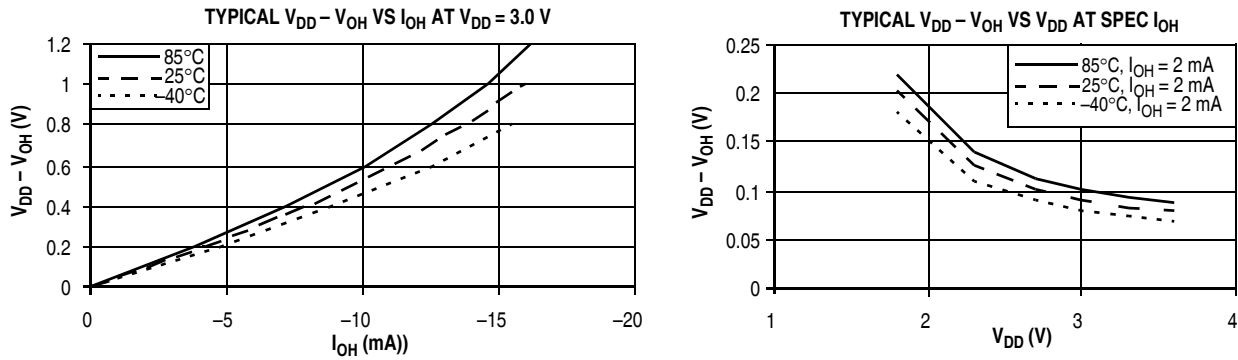


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

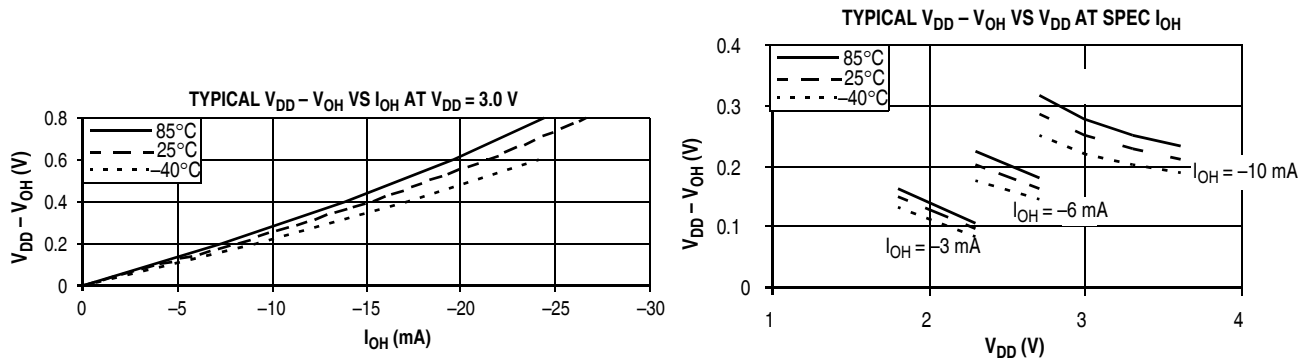


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

### 3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.



Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	R <sub>I</sub> DD	10 MHz	3	5.60	6	mA	-40 to 85°C
	T			1 MHz		0.80	—		
2	T	Run supply current FEI mode, all modules off	R <sub>I</sub> DD	10 MHz	3	3.60	—	mA	-40 to 85°C
	T			1 MHz		0.75	—		
3	T	Run supply current LPRS=0, all modules off	R <sub>I</sub> DD	16 kHz FBILP	3	165	—	μA	-40 to 85°C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off	R <sub>I</sub> DD	16 kHz FBELP	3	7.3	—	μA	-40 to 85°C
5	T	Wait mode supply current FEI mode, all modules off	W <sub>I</sub> DD	10 MHz	3	570	—	μA	-40 to 85°C
	T			1 MHz		290	—		
6	T	Wait mode supply current LPRS = 1, all mods off	W <sub>I</sub> DD	16 kHz FBELP	3	1	—	μA	-40 to 85°C
7	P	Stop2 mode supply current	S2I <sub>DD</sub>	—	3	0.25	0.65	μA	-40 to 25°C
	C			—		0.5	0.8		70°C
	P			—		1	2		85°C
	C			—	2	0.2	0.5		-40 to 25°C
	C			—		0.3	0.6		70°C
	C			—		0.7	1.6		85°C
8	P	Stop3 mode supply current no clocks active	S3I <sub>DD</sub>	—	3	0.45	0.80	μA	-40 to 25°C
	C			—		1	1.8		70°C
	P			—		3	5.8		85°C
	C			—	2	0.3	0.6		-40 to 25°C
	C			—		0.8	1.5		70°C
	C			—		2.5	5.0		85°C

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				-40°C	25°C	70°C	85°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN <sup>1</sup>	—	63	70	77	81	μA

## Electrical Characteristics

- <sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.
- <sup>2</sup> Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE = HGO = 0.
- <sup>3</sup> See crystal or resonator manufacturer's recommendation.
- <sup>4</sup> Proper PC board layout procedures must be followed to achieve specifications.

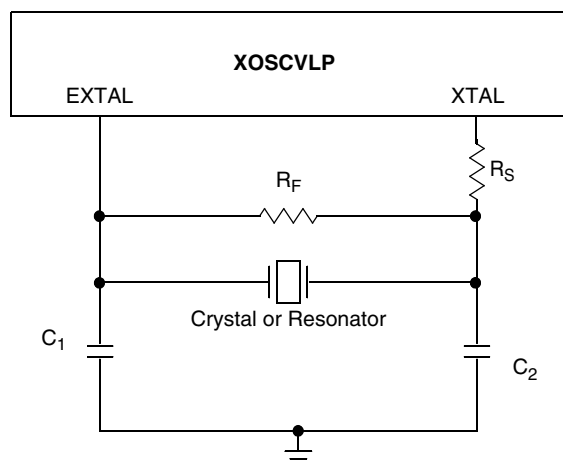


Figure 10. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

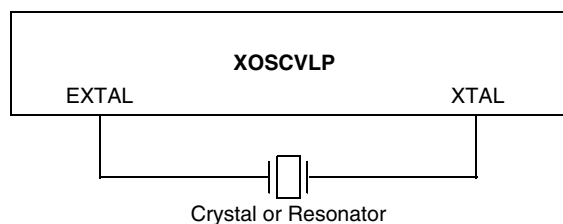


Figure 11. Typical Crystal or Resonator Circuit: Low Range/Low Power

## 3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical <sup>1</sup>	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at $V_{DD} = 3.6$ V and temperature = 25 °C	$f_{int\_t}$	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed	$f_{int\_ut}$	31.25	—	39.06	kHz
3	T	Internal reference start-up time	$t_{IRST}$	—	60	100	μs
4	P	DCO output frequency range — Low range (DRS = 00) trimmed <sup>2</sup>	$f_{dco\_t}$	16	—	20	MHz
5	P	DCO output frequency <sup>2</sup> Reference = 32768 Hz and DMX32 = 1	$f_{dco\_DMX32}$	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	% $f_{dco}$

### 3.11 Analog Comparator (ACMP) Electricals

Table 14. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{PWR}$	1.8	—	3.6	V
D	Supply current (active)	$I_{DDAC}$	—	20	35	$\mu A$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DD}$	V
P	Analog input offset voltage	$V_{AIO}$	—	20	40	mV
C	Analog comparator hysteresis	$V_H$	3.0	9.0	15.0	mV
P	Analog input leakage current	$I_{ALKG}$	—	—	1.0	$\mu A$
C	Analog comparator initialization delay	$t_{AINIT}$	—	—	1.0	$\mu s$

### 3.12 ADC Characteristics

Table 15. 12-Bit ADC Operating Conditions

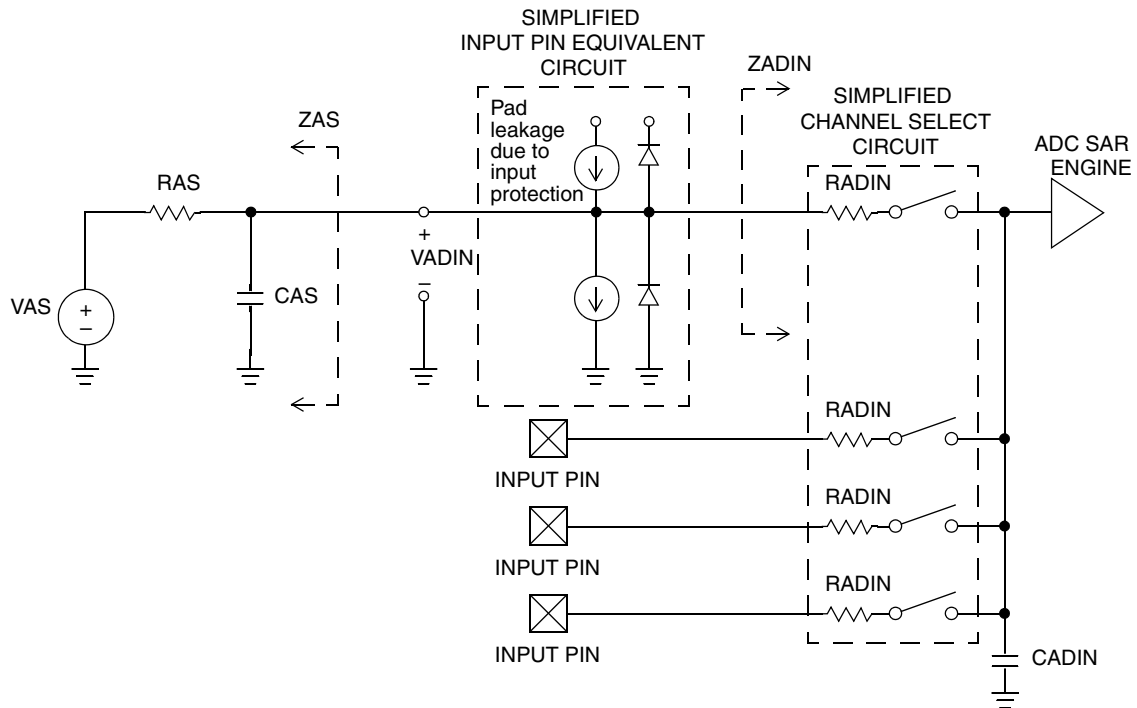
Characteristic	Conditions	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}$	1.8	—	3.6	V	
	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ ) <sup>2</sup>	$\Delta V_{DDA}$	-100	0	100	mV	
Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ ) <sup>2</sup>	$\Delta V_{SSA}$	-100	0	100	mV	
Supply Current	Stop, Reset, Module Off	$I_{DDAD}$	—	0.007	0.8	$\mu A$	
Input Voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
Input Capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input Resistance		$R_{ADIN}$	—	5	7	k $\Omega$	
Analog Source Resistance	12 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	— —	— —	2 5	k $\Omega$	External to MCU
	10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		— —	— —	5 10		
	8 bit mode (all valid $f_{ADCK}$ )		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	$f_{ADCK}$	0.4	—	8.0	MHz	
	Low Power (ADLPC = 1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DDA} = 3.0\text{ V}$ , Temp = 25 °C,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> DC potential difference.

**NOTE**

$V_{DDA}/V_{SSA}$  pins do not exist in 16-pin package. The signals are derived internally by double bonding to  $V_{DD}/V_{SS}$  pair of pins.



**Figure 16. ADC Input Impedance Equivalency Diagram**

Table 16. 12-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)

Characteristic	Conditions	C	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Integral Non-Linearity	12-bit mode	T	INL	—	±1.5	—	LSB <sup>2</sup>	
	10-bit mode	C		—	±0.5	—		
	8-bit mode			—	±0.3	—		
Zero-Scale Error	12-bit mode	C	E <sub>ZS</sub>	—	±1.5	—	LSB <sup>2</sup>	For 28-pin and 24-pin packages only. V <sub>ADIN</sub> = V <sub>SSA</sub>
	10-bit mode	P		—	±0.5	±1.5		
	8-bit mode	T		—	±0.5	±0.5		
Zero-Scale Error	10-bit mode	P	E <sub>ZS</sub>	—	±1.5	±2.1	LSB <sup>2</sup>	For 16-pin package only. V <sub>ADIN</sub> = V <sub>SSA</sub>
	8-bit mode	T		—	±0.5	±0.7		
Full-Scale Error	12-bit mode	T	E <sub>FS</sub>	—	±1	—	LSB <sup>2</sup>	For 28-pin and 24-pin packages only. V <sub>ADIN</sub> = V <sub>DDA</sub>
	10-bit mode	P		—	±0.5	±1		
	8-bit mode	T		—	±0.5	±0.5		
Full-Scale Error	10-bit mode	T	E <sub>FS</sub>	—	±1	±1.5	LSB <sup>2</sup>	For 16-pin package only. V <sub>ADIN</sub> = V <sub>DDA</sub>
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	12-bit mode	D	E <sub>Q</sub>	—	−1 to 0	—	LSB <sup>2</sup>	
	10-bit mode			—	—	±0.5		
	8-bit mode			—	—	±0.5		
Input Leakage Error	12-bit mode	D	E <sub>IL</sub>	—	±1	—	LSB <sup>2</sup>	Pad leakage <sup>3</sup> * R <sub>AS</sub>
	10-bit mode			0	±0.2	±4		
	8-bit mode			0	±0.1	±1.2		
Temp Sensor Slope	−40°C– 25°C	D	m	—	1.646	—	mV/°C	
	25°C– 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V <sub>TEMP25</sub>	—	701.2	—	mV	

<sup>1</sup> Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$

<sup>3</sup> Based on input pad leakage current. Refer to pad electricals.

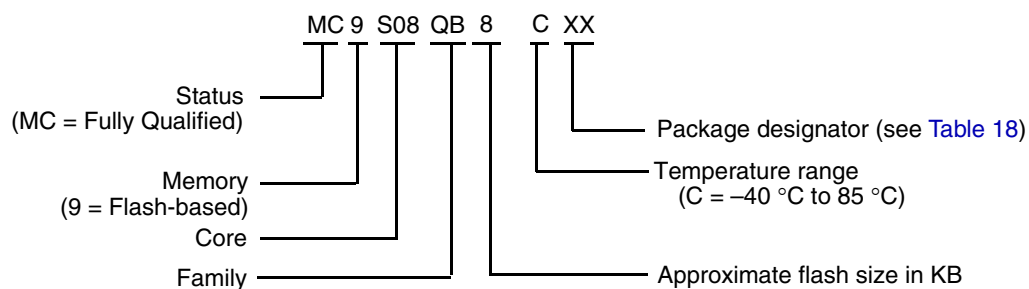
### 3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

## 4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



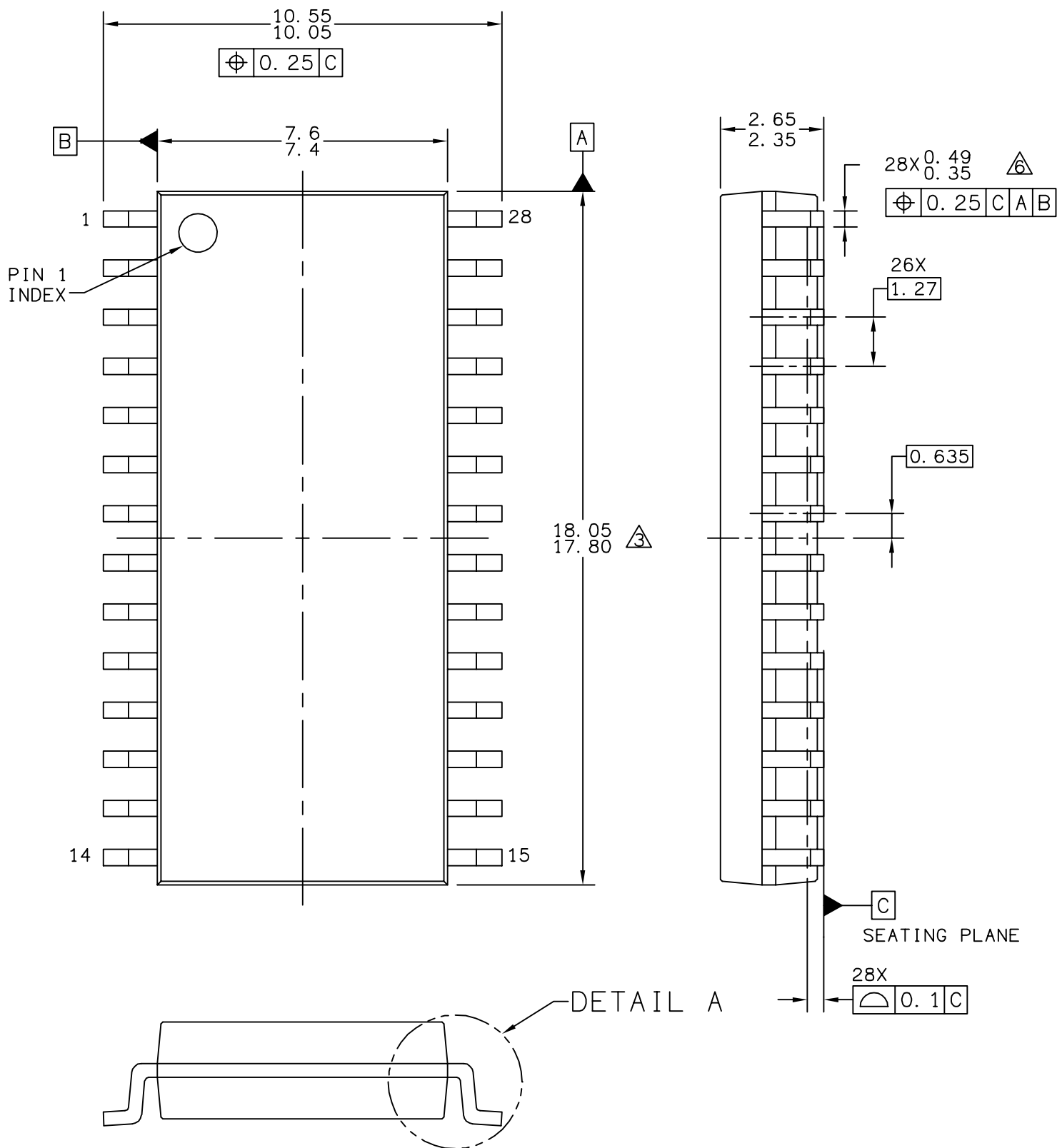
## 5 Package Information

**Table 18. Package Descriptions**

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
24	Quad Flat Non-Leaded	QFN	GK	1982-01	98ARL10608D
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

### 5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in [Table 18](#).



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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B		REV: G
	CASE NUMBER: 751F-05		10 MAR 2005
	STANDARD: MS-013AE		







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### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.
4.  COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

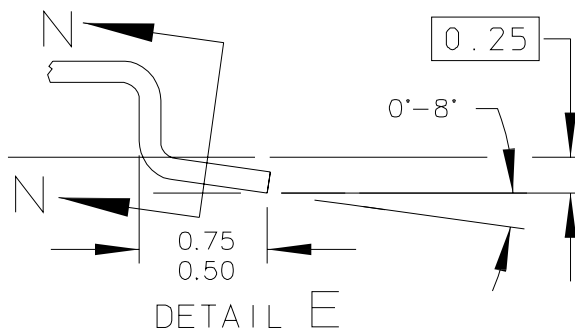
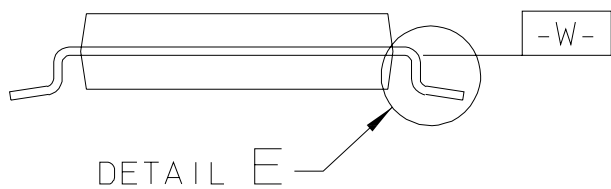
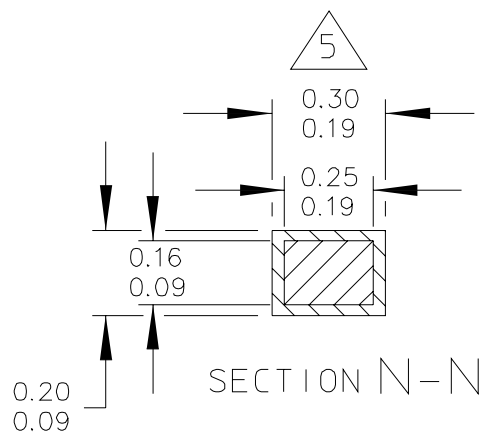
TITLE: THERMALLY ENHANCED QUAD  
FLAT NON-LEADED PACKAGE (QFN)  
24 TERMINAL, 0.65 PITCH (5 X 5 X 1)

CASE NUMBER: 1982-01

STANDARD: JEDEC-MO-220 VHHC-1

PACKAGE CODE: 6238

SHEET: 3 OF 4



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TITLE:  16 LD TSSOP, PITCH 0.65MM		DOCUMENT NO: 98ASH70247A	REV: B
		CASE NUMBER: 948F-01	19 MAY 2005
		STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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TITLE:  16 LD TSSOP, PITCH 0.65MM		DOCUMENT NO: 98ASH70247A		REV: B
		CASE NUMBER: 948F-01		19 MAY 2005
		STANDARD: JEDEC		



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