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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5288lti-lp090

1. Architectural Overview

Introducing the CY8C52LP family of ultra low power, flash Programmable System-on-Chip (PSoC) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5LP platform. The CY8C52LP family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

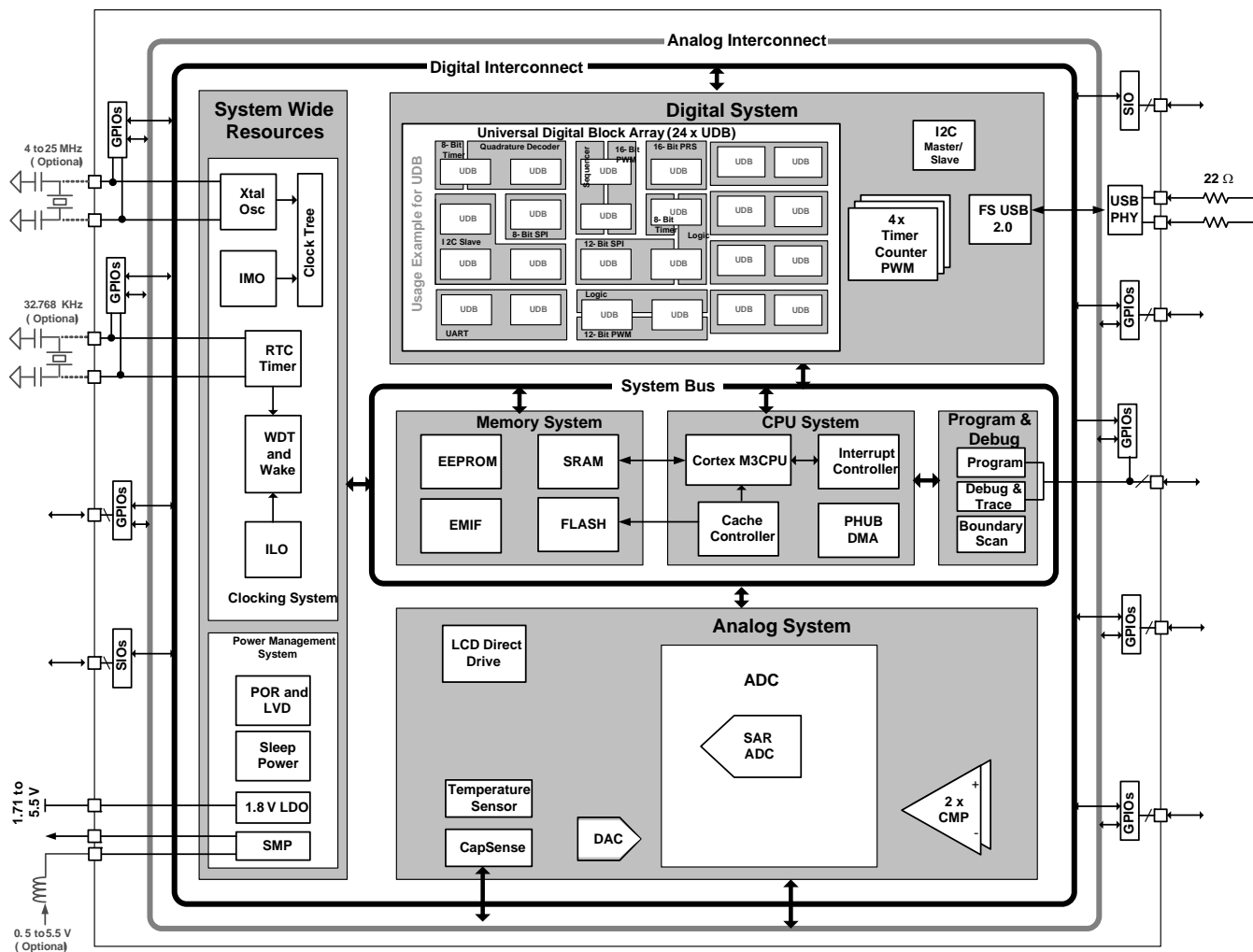
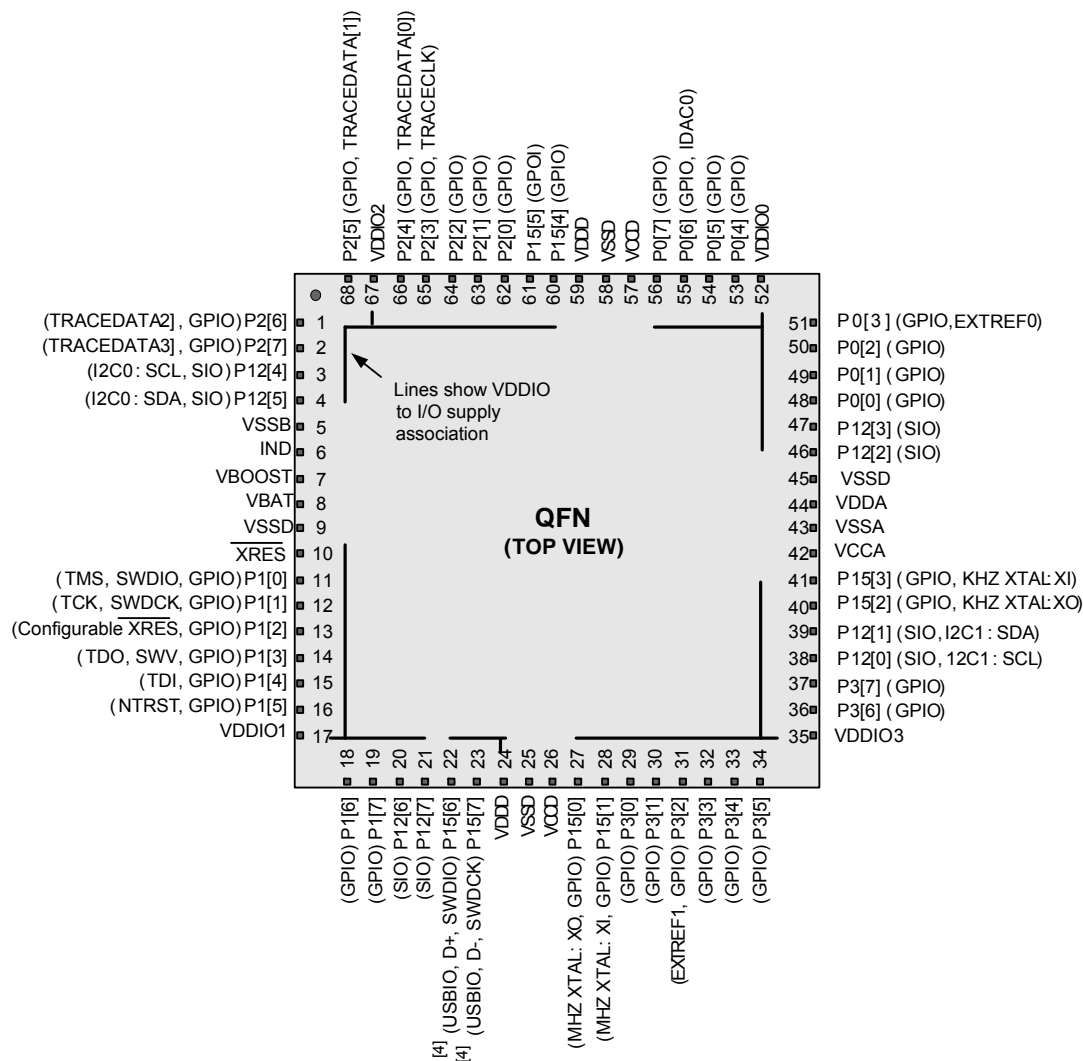


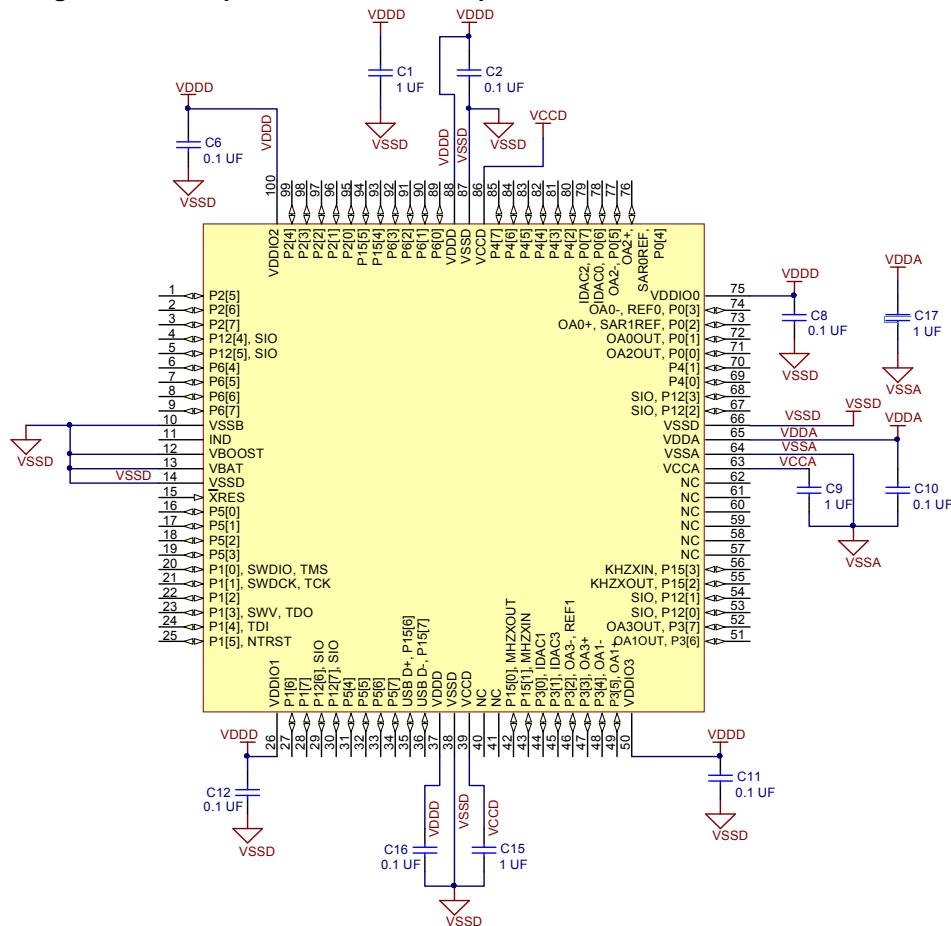
Figure 1-1 illustrates the major components of the CY8C52LP family. They are:

- ARM Cortex-M3 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low power UDBs. PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

Figure 2-3. 68-pin QFN Part Pinout^[3]

Notes

- The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.
- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-5. Example Schematic for 100-pin TQFP Part with Power Connections


Note The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in [Figure 2-6](#).

For more information on pad layout, refer to <http://www.cypress.com/cad-resources/psoc-5lp-cad-libraries>.

5.6 External Memory Interface

CY8C52LP provides an External Memory Interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C52LP only supports one type of external memory device at a time.

External memory is located in the Cortex-M3 external RAM space; it can use up to 24 address bits. See [Table 5-4 on page 22](#) and [Memory Map on page 22](#). The memory can be 8 or 16 bits wide.

Cortex-M3 instructions can be fetched from external memory if it is 16-bit. Other limitations apply; for details, see application note [AN89610, PSoC® 4 and PSoC 5LP ARM Cortex Code Optimization](#). There is no provision for code security in external memory. If code must be kept secure, then it should be placed in internal flash. See [Flash Security on page 19](#) and [Device Security on page 58](#).

Figure 5-1. EMIF Block Diagram

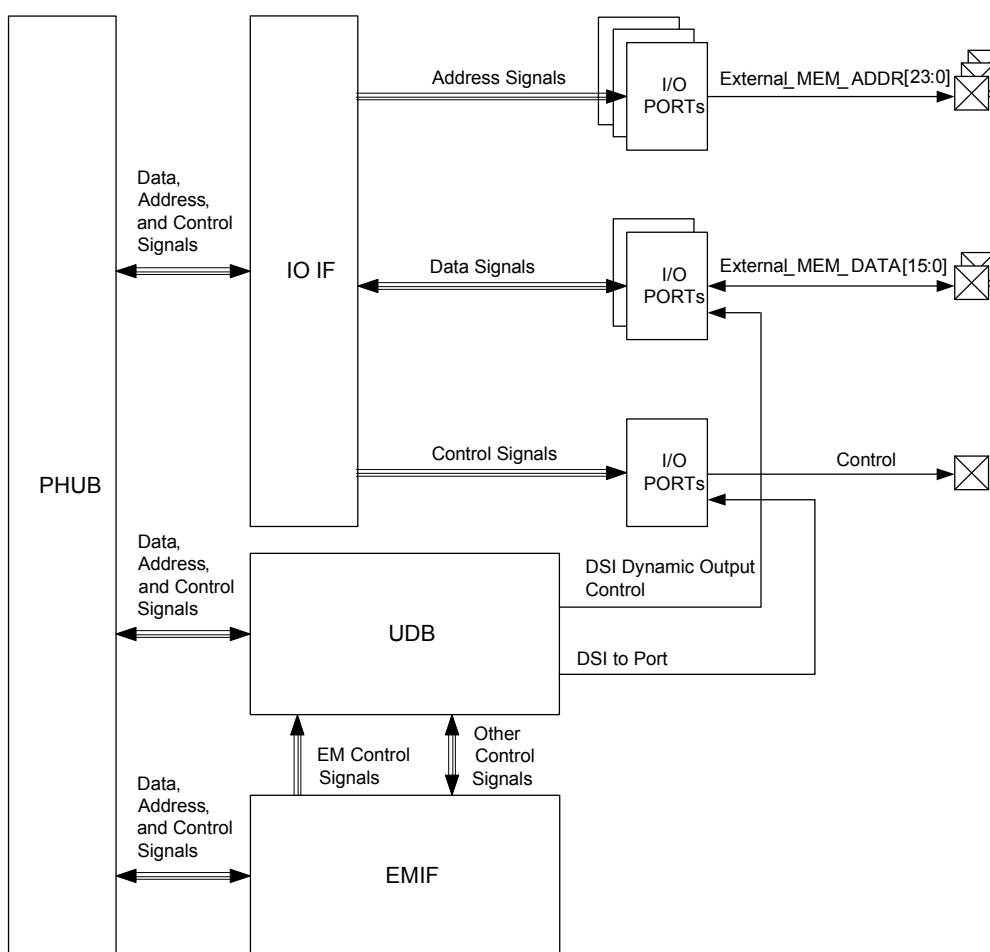
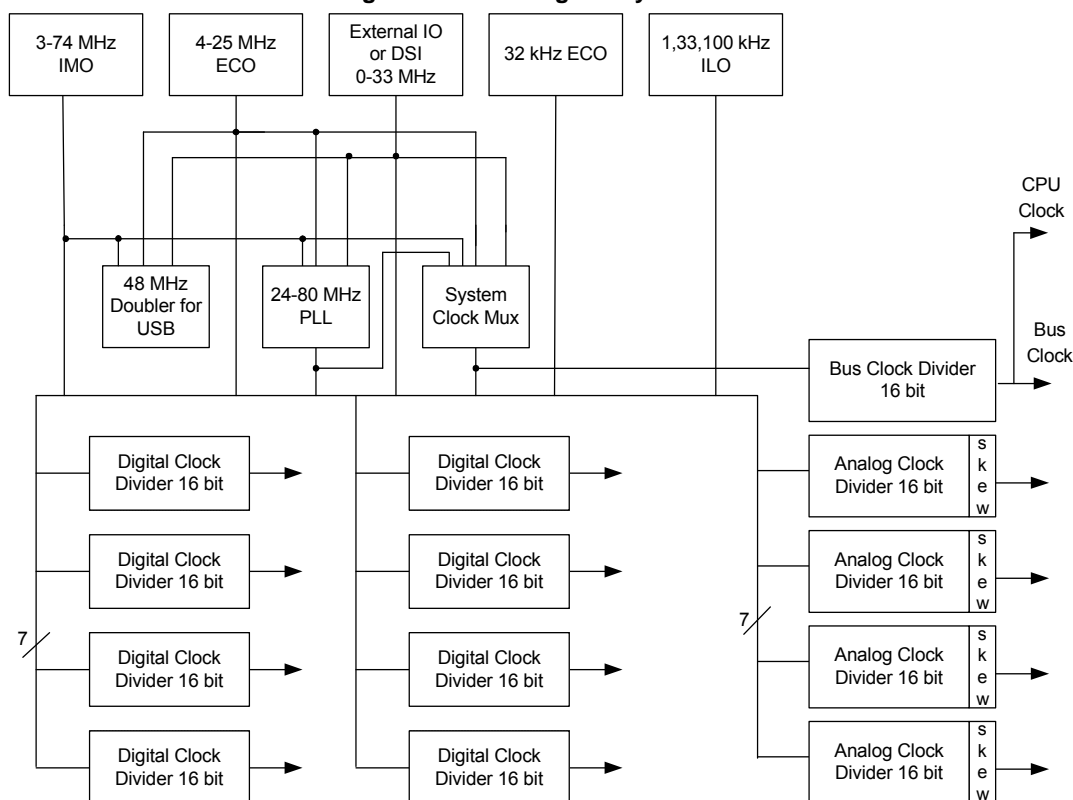


Figure 6-1. Clocking Subsystem


6.1.1 Internal Oscillators

Figure 6-1 shows that there are two internal oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its $\pm 2\%$ accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from $\pm 2\%$ at 3 MHz, up to $\pm 7\%$ at 74 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency (see [USB Clock Domain](#)). The IMO provides clock outputs at 3, 6, 12, 24, 48 and 74 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin).

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time. The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 80 MHz. Its input and feedback dividers supply

4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

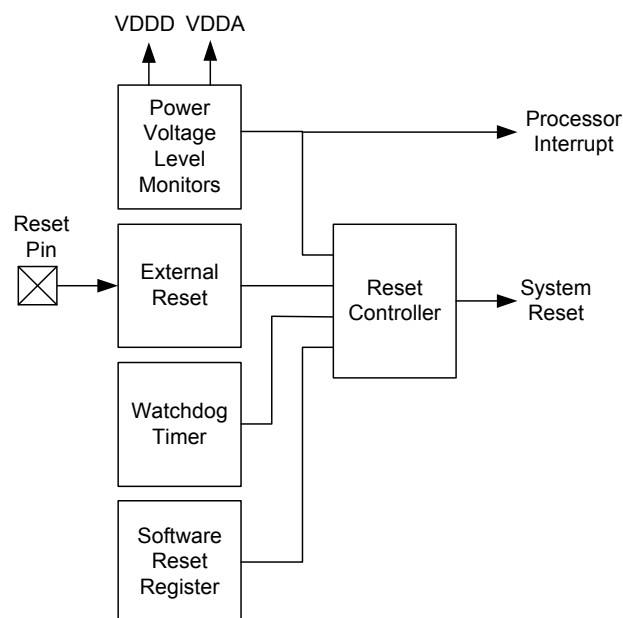
The PLL achieves phase lock within 250 μ s (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO, or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

6.1.1.4 Internal Low Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1-kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

The central timewheel is a 1-kHz, free-running, 13-bit counter clocked by the ILO. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

Figure 6-8. Resets


The term **system reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

■ IPOR - Initial Power-on-Reset

At initial power on, IPOR monitors the power voltages V_{DDD} , V_{DDA} , V_{CCD} and V_{CCA} . The trip level is not precise. It is set to approximately 1 volt (0.75 V to 1.45 V). This is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

■ PRES - Precise Low-Voltage Reset

This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

■ ALVI, DLVI, AHVI - Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt circuits are available to detect when V_{DDA} and V_{DDD} go outside a voltage range. For AHVI, V_{DDA} is compared to a fixed trip level. For ALVI and DLVI, V_{DDA} and V_{DDD} are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V-5.5 V	1.70 V-5.45 V in 250 mV increments
ALVI	VDDA	1.71 V-5.5 V	1.70 V-5.45 V in 250 mV increments
AHVI	VDDA	1.71 V-5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wakeup sequence. The interrupt is then recognized and may be serviced.

The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

■ XRES - External Reset

PSoC 5LP has a dedicated XRES pin, which holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

The external reset is active low. It includes an internal pull up resistor. XRES is active during sleep and hibernate modes.

After XRES has been deasserted, at least 10 μ s must elapse before it can be reasserted.

■ SRES - Software Reset

A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

Another register bit exists to disable this function.

■ WRES - Watchdog Timer Reset

The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

7. Digital Subsystem

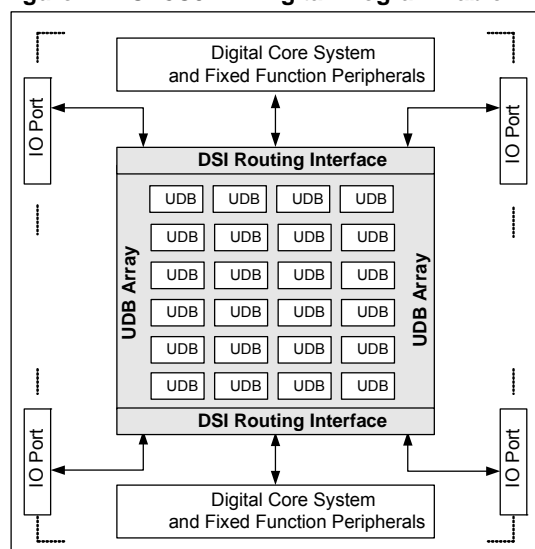
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- **Universal digital blocks (UDB)** - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- **Universal digital block array** - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the digital system interconnect.
- **Digital system interconnect (DSI)** - Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the DSI to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the UDB array.

Figure 7-1. CY8C52LP Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C52LP family's UDBs and analog blocks allow you to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog. However, you may also create your own custom components using PSoC Creator. Using PSoC Creator, you may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C52LP family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C52LP family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **Communications**
 - I²C
 - UART
 - SPI
- **Functions**
 - EMIF
 - PWMs
 - Timers
 - Counters
 -
- **Logic**
 - NOT
 - OR
 - XOR
 - AND

7.1.2 Example Analog Components

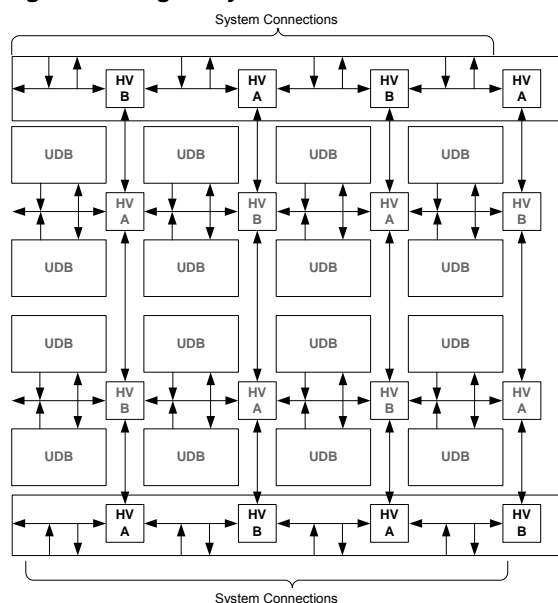
The following is a sample of the analog components available in PSoC Creator for the CY8C52LP family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **ADC**
 - Successive Approximation (SAR ADC)
- **DACs**
 - Current
 - Voltage
 - PWM
- **Comparators**

7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure



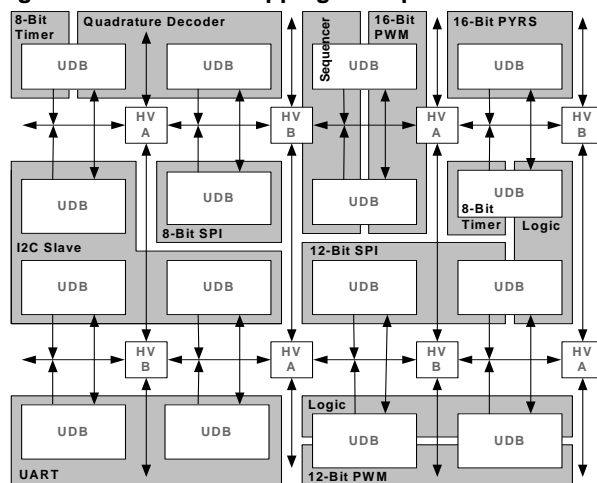
7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can

utilize the unused PLD blocks in the 8-bit timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

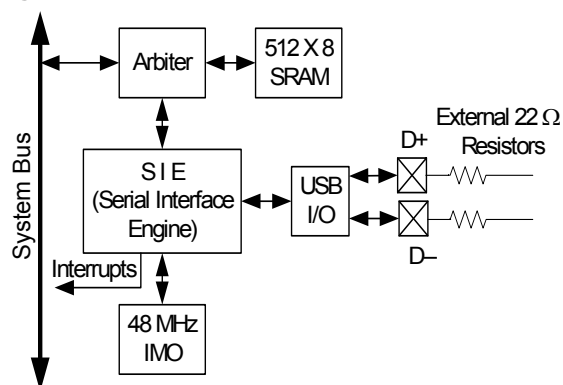
7.5 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the “I/O System and Routing” section on page 32.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
 - Manual Memory Management with No DMA Access
 - Manual Memory Management with Manual DMA Access
 - Automatic Memory Management with Automatic DMA Access
- Internal 3.3 V regulator for transceiver
- Internal 48 MHz oscillator that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-14. USB



7.6 Timers, Counters, and PWMs

The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded

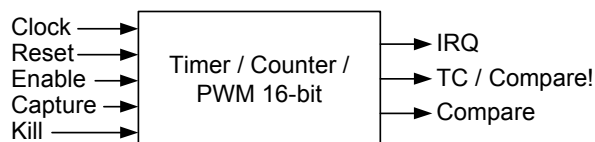
peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit timer/counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-15. Timer/Counter/PWM

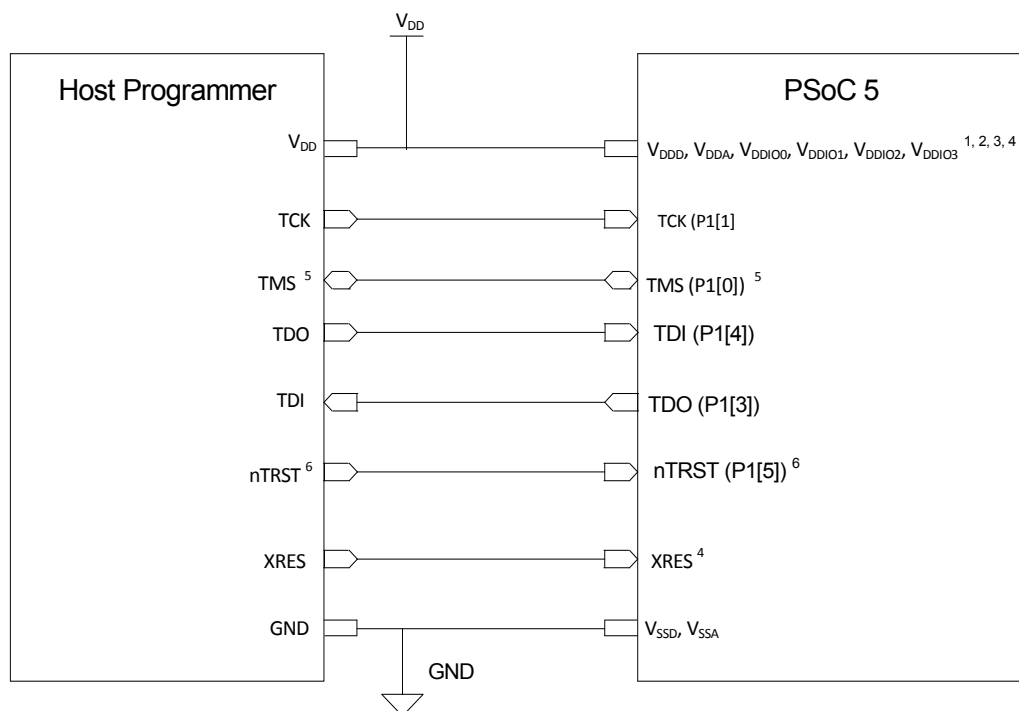


9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG clock frequency can be up to 12 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit

transfers, whichever is least. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as General Purpose I/O (GPIO) instead. The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

Figure 9-1. JTAG Interface Connections between PSoC 5LP and Programmer



¹ The voltage levels of Host Programmer and the PSoC 5 voltage domains involved in Programming should be same. The Port 1 JTAG pins and XRES pin are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD}. Rest of PSoC 5 voltage domains (V_{DD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

² V_{DDA} must be greater than or equal to all other power supplies (V_{DD}, V_{DDIO}'s) in PSoC 5.

³ For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (V_{DD}, V_{DDA}, All V_{DDIO}'s) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, V_{DDA} must be greater than or equal to all other supplies.

⁴ For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS, TCK, TDI, TDO pins of PSoC 5, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

⁵ By default, PSoC 5 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 5 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

⁶ nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controller during first time programming of PSoC 5 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

9.2 SWD Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D- pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

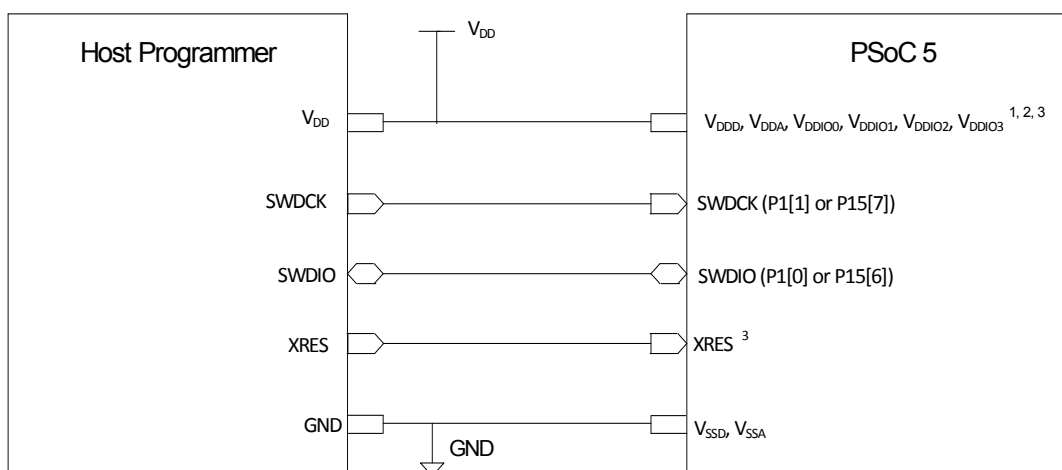
SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 μ s (key window) after reset, that pin pair

(JTAG or USB) receives a predetermined acquire sequence of 1s and 0s. If the NVL latches are set for SWD (see [Section 5.5](#)), this sequence need not be applied to the JTAG pin pair. The acquire sequence must always be applied to the USB pin pair.

SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenables the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Figure 9-2. SWD Interface Connections between PSoC 5LP and Programmer



¹ The voltage levels of the Host Programmer and the PSoC 5 voltage domains involved in programming should be the same. The XRES pin is powered by VDDIO1. The USB SWD pins are powered by VDD. So for Programming using the USB SWD pins with XRES pin, the VDD, VDDIO1 of PSoC 5 should be at the same voltage level as Host VDD. Rest of PSoC 5 voltage domains (VDDA, VDDIO0, VDDIO2, VDDIO3) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by VDDIO1. So VDDIO1 of PSoC 5 should be at same voltage level as host VDD for Port 1 SWD programming. Rest of PSoC 5 voltage domains (VDD, VDDA, VDDIO0, VDDIO2, VDDIO3) need not be at the same voltage level as host Programmer.

² VDDA must be greater than or equal to all other power supplies (VDD, VDDIO's) in PSoC 5.

³ For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (VDD, VDDA, All VDDIO's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

11.4 Inputs and Outputs

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

When the power supplies ramp up, there are low-impedance connections between each GPIO pin and its V_{DDIO} supply. This causes the pin voltages to track V_{DDIO} until both V_{DDIO} and V_{DDA} reach the IPOR voltage, which can be as high as 1.45 V. At that point the low-impedance connections no longer exist, and the pins change to their normal NVL settings.

Also, if V_{DDA} is less than V_{DDIO} , a low-impedance path may exist between a GPIO and V_{DDA} , causing the GPIO to track V_{DDA} until V_{DDA} becomes greater than or equal to V_{DDIO} .

11.4.1 GPIO

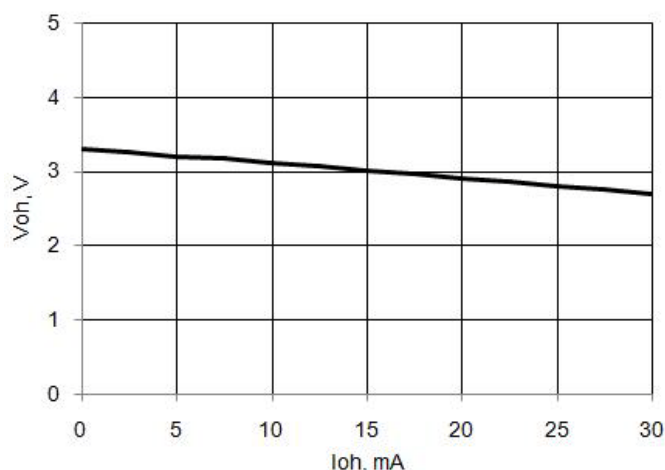
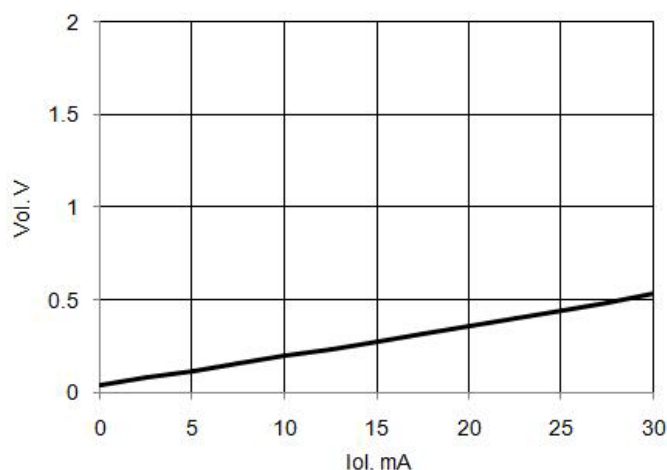
Table 11-8. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input, $PRT[x]CTL = 0$	$0.7 \times V_{DDIO}$	—	—	V
V_{IL}	Input voltage low threshold	CMOS Input, $PRT[x]CTL = 0$	—	—	$0.3 \times V_{DDIO}$	V
V_{IH}	Input voltage high threshold	LVTTL Input, $PRT[x]CTL = 1, V_{DDIO} < 2.7\text{ V}$	$0.7 \times V_{DDIO}$	—	—	V
V_{IH}	Input voltage high threshold	LVTTL Input, $PRT[x]CTL = 1, V_{DDIO} \geq 2.7\text{ V}$	2.0	—	—	V
V_{IL}	Input voltage low threshold	LVTTL Input, $PRT[x]CTL = 1, V_{DDIO} < 2.7\text{ V}$	—	—	$0.3 \times V_{DDIO}$	V
V_{IL}	Input voltage low threshold	LVTTL Input, $PRT[x]CTL = 1, V_{DDIO} \geq 2.7\text{ V}$	—	—	0.8	V
V_{OH}	Output voltage high	$I_{OH} = 4\text{ mA}$ at 3.3 V_{DDIO}	$V_{DDIO} - 0.6$	—	—	V
		$I_{OH} = 1\text{ mA}$ at 1.8 V_{DDIO}	$V_{DDIO} - 0.5$	—	—	V
V_{OL}	Output voltage low	$I_{OL} = 8\text{ mA}$ at 3.3 V_{DDIO}	—	—	0.6	V
		$I_{OL} = 3\text{ mA}$ at 3.3 V_{DDIO}	—	—	0.4	V
		$I_{OL} = 4\text{ mA}$ at 1.8 V_{DDIO}	—	—	0.6	V
R_{pullup}	Pull up resistor		3.5	5.6	8.5	$k\Omega$
$R_{pulldown}$	Pull down resistor		3.5	5.6	8.5	$k\Omega$
I_{IL}	Input leakage current (absolute value) ^[31]	$25\text{ }^{\circ}\text{C}, V_{DDIO} = 3.0\text{ V}$	—	—	2	nA
C_{IN}	Input capacitance ^[31]	P0.0, P0.1, P0.2, P3.6, P3.7	—	17	20	pF
		P0.3, P0.4, P3.0, P3.1, P3.2	—	10	15	pF
		P0.6, P0.7, P15.0, P15.6, P15.7 ^[32]	—	7	12	pF
		All other GPIOs	—	5	9	pF
V_H	Input voltage hysteresis (Schmitt-Trigger) ^[31]		—	40	—	mV
I_{diode}	Current through protection diode to V_{DDIO} and V_{SSIO}		—	—	100	μA
R_{global}	Resistance pin to analog global bus	$25\text{ }^{\circ}\text{C}, V_{DDIO} = 3.0\text{ V}$	—	320	—	Ω
R_{mux}	Resistance pin to analog mux bus	$25\text{ }^{\circ}\text{C}, V_{DDIO} = 3.0\text{ V}$	—	220	—	Ω

Notes

31. Based on device characterization (Not production tested).

32. For information on designing with PSoC oscillators, refer to the application note, AN54439 - PSoC® 3 and PSoC 5 External Oscillator.

Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode

Figure 11-23. USBIO Output Low Voltage and Current, GPIO Mode

Table 11-14. USBIO AC Specifications^[38]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ V _{DD} ≤ 5.5 V	–	–	20	MHz
		V _{DD} = 1.71 V	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V _{DD}	V _{DD} > 3 V, 25 pF load	–	–	12	ns
		V _{DD} = 1.71 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V _{DD}	V _{DD} > 3 V, 25 pF load	–	–	12	ns
		V _{DD} = 1.71 V, 25 pF load	–	–	40	ns

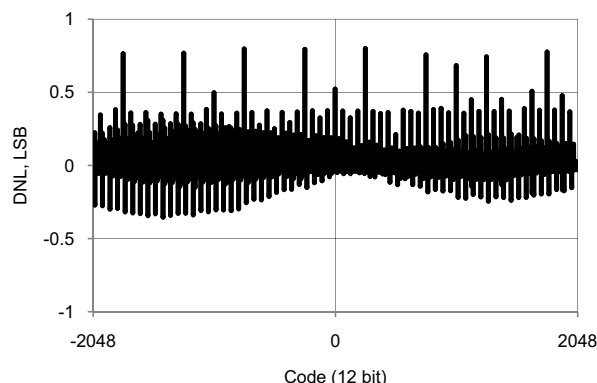
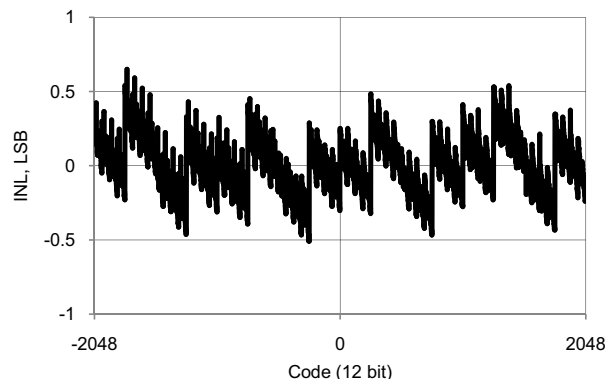
Note

38. Based on device characterization (Not production tested).

11.5.2 SAR ADC

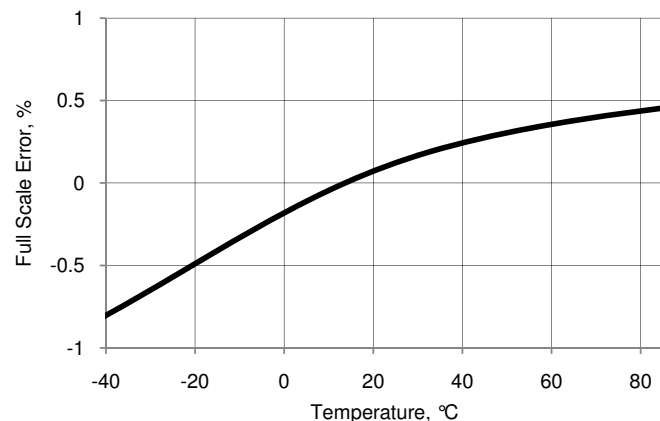
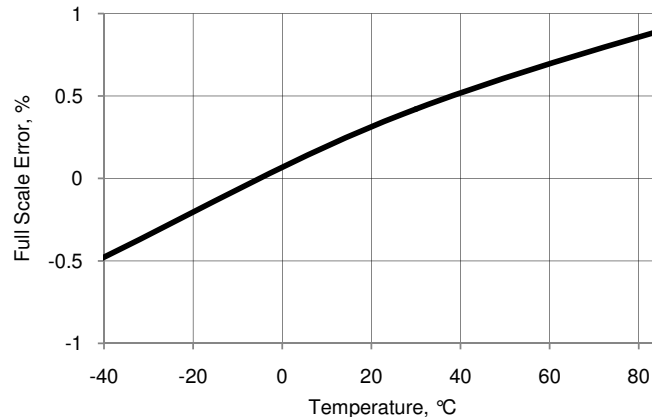
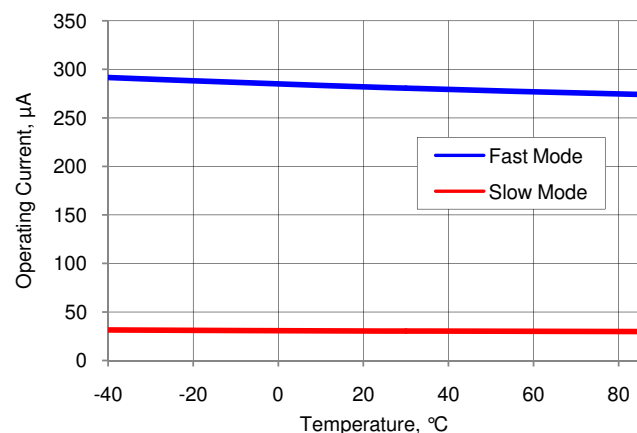
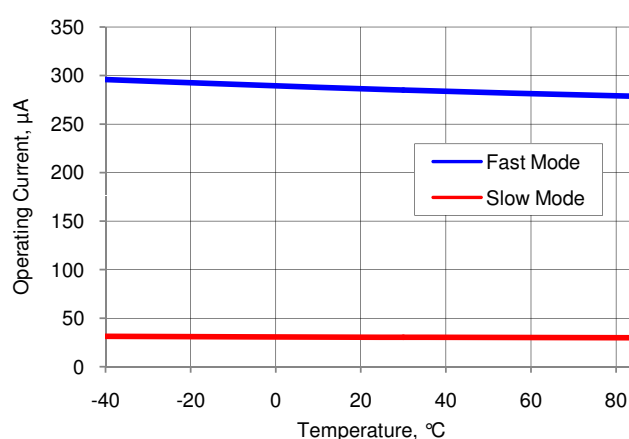
Table 11-19. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity ^[40]		Yes	–	–	
Ge	Gain error ^[41]	External reference	–	–	±0.1	%
V _{OS}	Input offset voltage		–	–	±2	mV
I _{DD}	Current consumption ^[40]		–	–	1	mA
	Input voltage range – single-ended ^[40]		V _{SSA}	–	V _{DDA}	V
	Input voltage range – differential ^[40]		V _{SSA}	–	V _{DDA}	V
PSRR	Power supply rejection ratio ^[40]		70	–	–	dB
CMRR	Common mode rejection ratio		70	–	–	dB
INL	Integral non linearity ^[40]	V _{DDA} 1.71 to 5.5 V, 1 Msps, V _{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1.5	LSB
		V _{DDA} 2.0 to 3.6 V, 1 Msps, V _{REF} 2 to V _{DDA} , bypassed at ExtRef pin	–	–	±1.2	LSB
		V _{DDA} 1.71 to 5.5 V, 500 kpsps, V _{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	±1.3	LSB
DNL	Differential non linearity ^[40]	V _{DDA} 1.71 to 5.5 V, 1 Msps, V _{REF} 1 to 5.5 V, bypassed at ExtRef pin	–	–	+2/–1	LSB
		V _{DDA} 2.0 to 3.6 V, 1 Msps, V _{REF} 2 to V _{DDA} , bypassed at ExtRef pin No missing codes	–	–	1.7/–0.99	LSB
		V _{DDA} 1.71 to 5.5 V, 500 kpsps, V _{REF} 1 to 5.5 V, bypassed at ExtRef pin No missing codes	–	–	+2/–0.99	LSB
R _{IN}	Input resistance ^[40]		–	180	–	kΩ

Figure 11-25. SAR ADC DNL vs Output Code, Bypassed Internal Reference Mode

Figure 11-26. SAR ADC INL vs Output Code, Bypassed Internal Reference Mode

Notes

40. Based on device characterization (Not production tested).

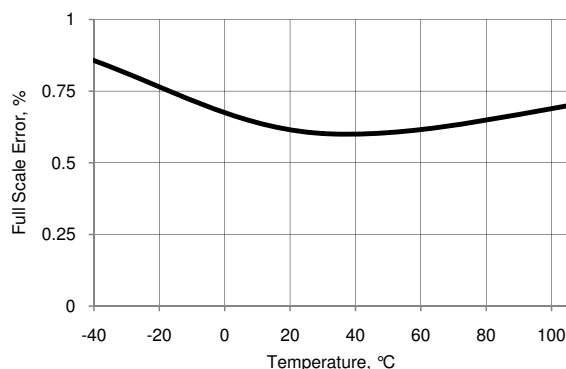
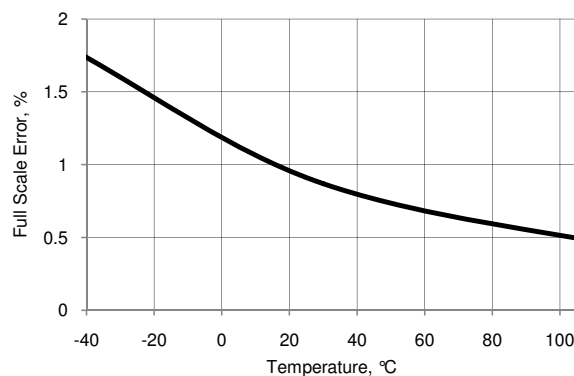
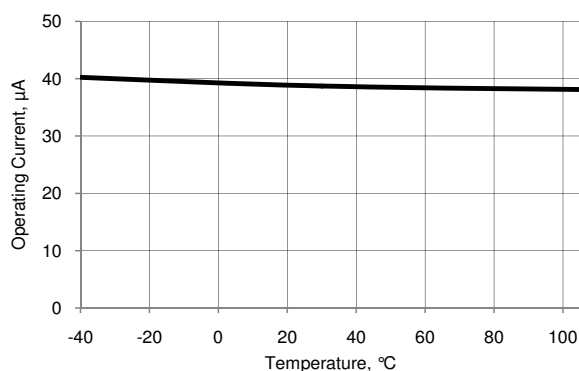
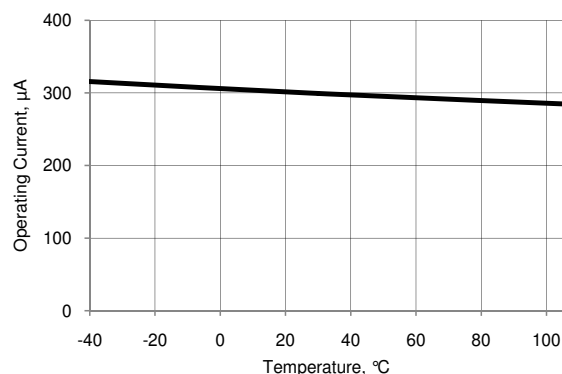
41. For total analog system I_{dd} < 5 mA, depending on package used. With higher total analog system currents it is recommended that the SAR ADC be used in differential mode.

Figure 11-37. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Source Mode

Figure 11-38. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Sink Mode

Figure 11-39. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Source Mode

Figure 11-40. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Sink Mode

Table 11-26. IDAC AC Specifications^[50]

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{DAC}	Update rate		–	–	8	Msp/s
T _{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 μ A, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
		Range = 255 μ A, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 μ A, source mode, fast mode, V _{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Note

50. Based on device characterization (Not production tested).

Figure 11-49. VDAC Full Scale Error vs Temperature, 1 V Mode

Figure 11-50. VDAC Full Scale Error vs Temperature, 4 V Mode

Figure 11-51. VDAC Operating Current vs Temperature, 1V Mode, Slow Mode

Figure 11-52. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode

Table 11-28. VDAC AC Specifications^[53]

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{DAC}	Update rate	1 V scale	—	—	1000	ksps
		4 V scale	—	—	250	ksps
T _{settleP}	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	—	0.45	1	µs
		4 V scale, Cload = 15 pF	—	0.8	3.2	µs
T _{settleN}	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	—	0.45	1	µs
		4 V scale, Cload = 15 pF	—	0.7	3	µs
	Voltage noise	Range = 1 V, fast mode, V _{DDA} = 5 V, 10 kHz	—	750	—	nV/sqrtHz

Note

53. Based on device characterization (Not production tested).

11.6 Digital Peripherals

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component datasheet in PSoC Creator.

Table 11-32. Timer DC Specifications^[55]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	80 MHz		–	360	–	μA

Table 11-33. Timer AC Specifications^[55]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	80.01	MHz
	Capture pulse width (Internal) ^[56]		15	–	–	ns
	Capture pulse width (external)		30	–	–	ns
	Timer resolution ^[56]		15	–	–	ns
	Enable pulse width ^[56]		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width ^[56]		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component datasheet in PSoC Creator.

Table 11-34. Counter DC Specifications^[55]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	80 MHz		–	360	–	μA

Table 11-35. Counter AC Specifications^[55]

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	80.01	MHz
	Capture pulse ^[56]		15	–	–	ns
	Resolution ^[56]		15	–	–	ns
	Pulse width ^[56]		15	–	–	ns
	Pulse width (external)		30			ns

Notes

55. Based on device characterization (Not production tested).

56. For correct operation, the minimum Timer/Counter/PWM input pulse width is the period of bus clock.

11.7.3 Nonvolatile Latches (NVL)

Table 11-46. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V _{DDD} pin	1.71	–	5.5	V

Table 11-47. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1K	–	–	program/erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	program/erase cycles
	NVL data retention time	Average ambient temp. T _A ≤ 55 °C	20	–	–	years
		Average ambient temp. T _A ≤ 85 °C	10	–	–	years

11.7.4 SRAM

Table 11-48. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{SRAM}	SRAM retention voltage ^[62]		1.2	–	–	V

Table 11-49. SRAM AC Specifications

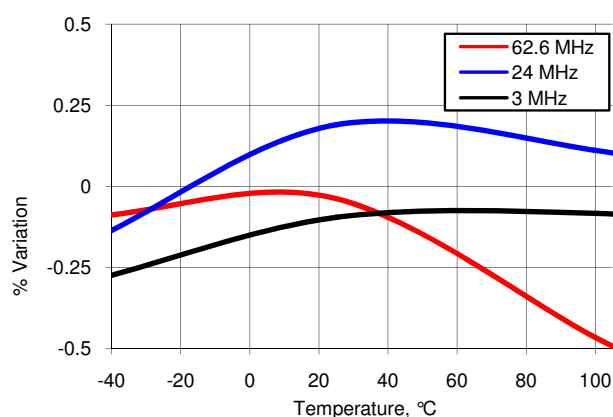
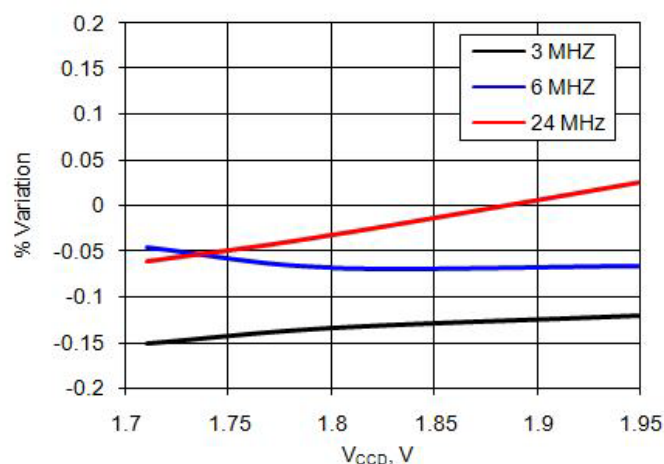
Parameter	Description	Conditions	Min	Typ	Max	Units
F _{SRAM}	SRAM operating frequency		DC	–	80.01	MHz

Note

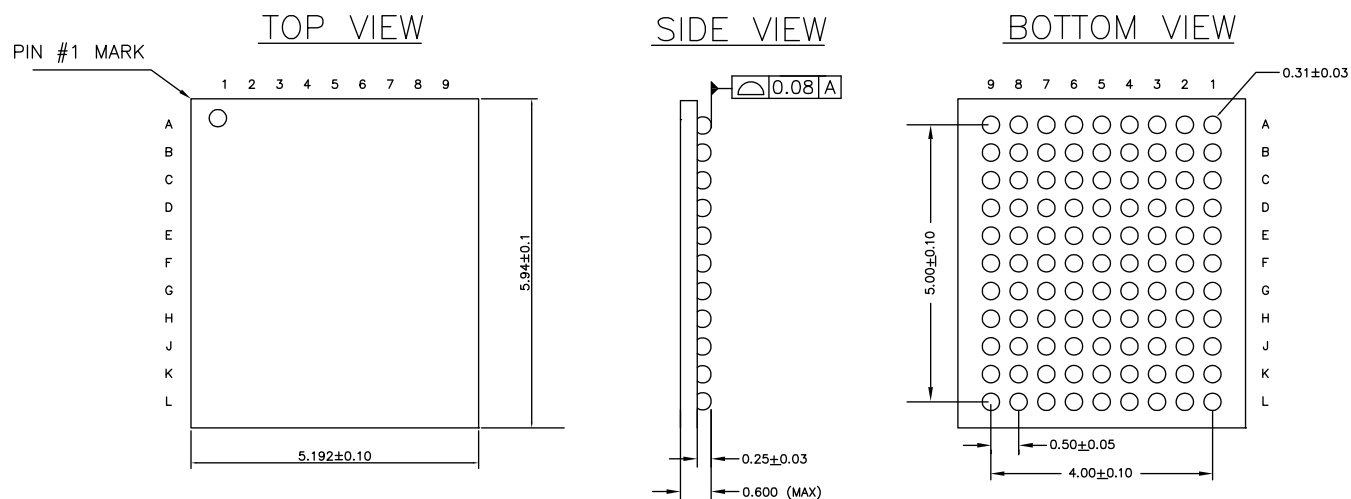
62. Based on device characterization (Not production tested).

Table 11-61. IMO AC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Jp-p	Jitter (peak to peak) ^[78]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term) ^[78]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Figure 11-63. IMO Frequency Variation vs. Temperature

Figure 11-64. IMO Frequency Variation vs. V_{CC}

Note

78. Based on device characterization (Not production tested).

Figure 13-3. WLCSP Package (5.192 x 5.940 x 0.6 mm)

NOTES:

1. REFERENCE JEDEC Publication 95: Design Guide 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

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