Renesas Electronics America Inc - M38039GCHHP#U0 Datasheet

Welcome to E-XFL.COM

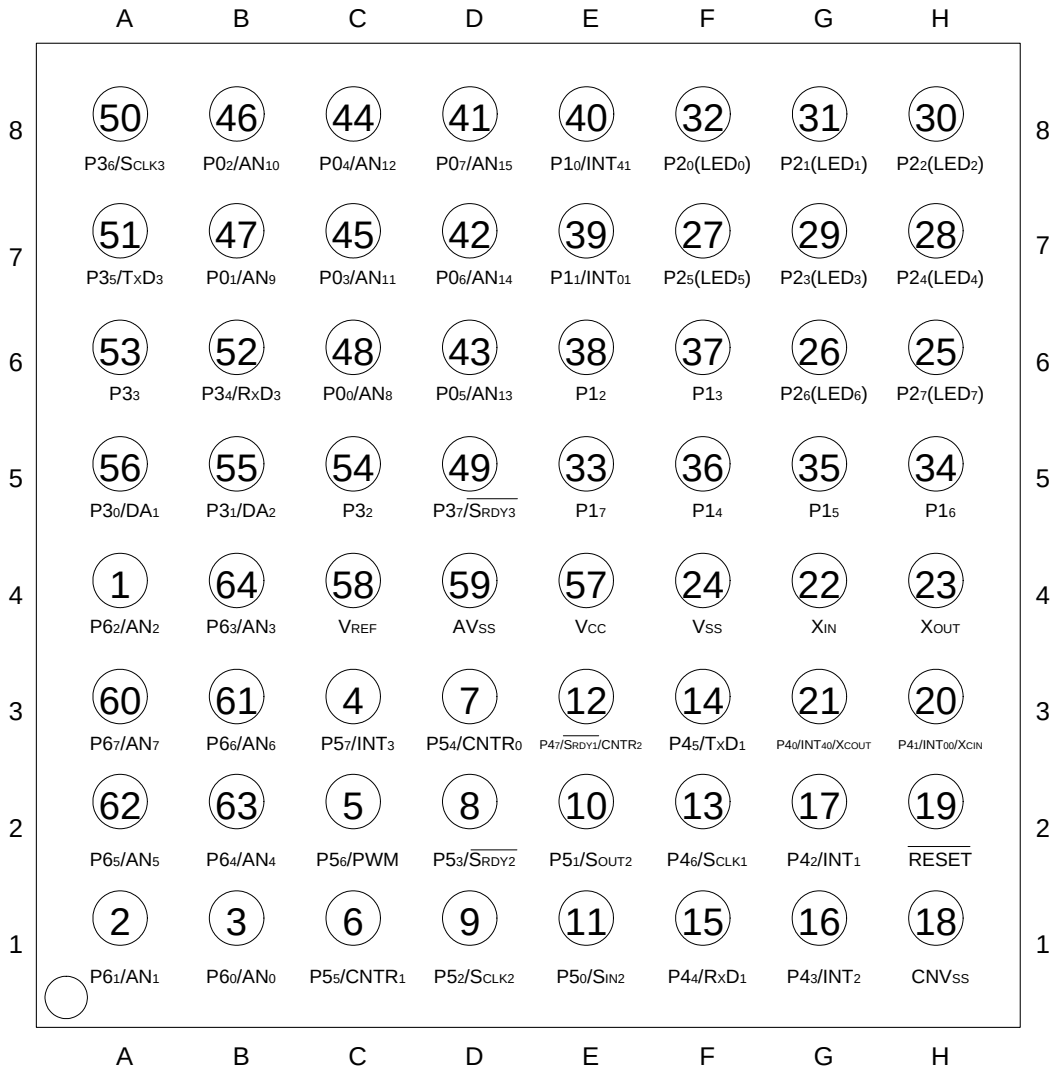
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	16.8MHz
Connectivity	SIO, UART/USART
Peripherals	LED, PWM, WDT
Number of I/O	56
Program Memory Size	48KB (48K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m38039gchhp-u0

PIN CONFIGURATION (TOP VIEW)



Package code : PTLG0064JA-A (64F0G)

Note : The numbers in circles corresponds with the number on the packages HP/KP.

Package (TOP VIEW)

Fig 3. Pin configuration (Top view) (PTLG0064JA-A (64F0G))

Table 1 Performance overview

Parameter				Function
Number of basic instructions				71
Minimum instruction execution time				0.24 μs (Oscillation frequency 16.8 MHz)
Oscillation frequency				16.8 MHz (Maximum)
Memory sizes			ROM	16 to 48 Kbytes
			RAM	2048 Kbytes
I/O port	P0, P1, P2, P3, P4, P5, P6			56 pins
Software pull-up resistors				Built-in
Interrupt				21 sources, 16 vectors (8 external, 12 internal, 1 software)
Timer				8-bit × 4 (with 8-bit prescaler) 16-bit × 1
Serial interface				8-bit × 2 (UART or Clock-synchronized) 8-bit × 1 (Clock-synchronized)
PWM				8-bit × 1 (with 8-bit prescaler)
A/D converter				10-bit × 16 channels (8-bit reading enabled)
D/A converter				8-bit × 2 channels
Watchdog timer				16-bit × 1
LED direct drive port				8 (average current: 10 mA, peak current: 20 mA, total current: 80 mA)
Clock generating circuits				Built-in 2 circuits (connect to external ceramic resonator or quartz-crystal oscillator)
Power source voltage	In high-speed mode	At 16.8 MHz		4.5 to 5.5 V
		At 12.5 MHz		4.0 to 5.5 V
		At 8.4 MHz		2.7 to 5.5 V
		At 4.2 MHz		2.2 to 5.5 V
		At 2.1 MHz		2.0 to 5.5 V
	In middle-speed mode	At 16.8 MHz		4.5 to 5.5 V
		At 12.5 MHz		2.7 to 5.5 V
		At 8.4 MHz		2.2 to 5.5 V
		At 6.3 MHz		1.8 to 5.5 V
	In low-speed mode	At 32 kHz		1.8 to 5.5 V
Power dissipation	In high-speed mode			Std. 40 mW (V_{CC}=5.0V, f(X_{IN})=16.8 MHz, Ta=25 °C)
	In low-speed mode			Std. 45 μW (V_{CC}=3.0V, f(X_{IN})=Stop, f(X_{CIN})=32kHz, Ta=25 °C)
Input/Output characteristics	Input/Output withstand voltage			V_{CC}
	Output current			10 mA
Operating temperature range				-20 to 85 °C
Device structure				CMOS silicon gate
Package				64-pin plastic molded SDIP/LQFP/FLGA

Table 3 Support products

Product name	QzROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38039G4H-XXXHP	16384 (16254) (3)	2048	PLQP0064KB-A (64P6Q-A)	QzROM version (Programmed shipment) (1)
M38039G4H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039G6H-XXXHP	24576 (24446) (3)		PLQP0064KB-A (64P6Q-A)	
M38039G6H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039G8H-XXXHP	32768 (32638) (3)		PLQP0064KB-A (64P6Q-A)	
M38039G8H-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039GCH-XXXHP	49152 (49022) (3)		PLQP0064KB-A (64P6Q-A)	
M38039GCH-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039GCH-XXXWG			PTLG0064JA-A (64F0G)	
M38039G4HSP	16384 (16254) (3)		PRDP0064BA-A (64F4B)	QzROM version (blank) (2)
M38039G4HHP			PLQP0064KB-A (64P6Q-A)	
M38039G4HKP			PLQP0064GA-A (64P6U-A)	
M38039G6HSP	24576 (24446) (3)		PRDP0064BA-A (64P4B)	
M38039G6HHP			PLQP0064KB-A (64P6Q-A)	
M38039G6HKP			PLQP0064GA-A (64P6U-A)	
M38039G8HSP	32768 (32638) (3)		PRDP0064BA-A (64P4B)	
M38039G8HHP			PLQP0064KB-A (64P6Q-A)	
M38039G8HKP			PLQP0064GA-A (64P6U-A)	
M38039GCHSP	49152 (49022) (3)		PRDP0064BA-A (64P4B)	
M38039GCHHP			PLQP0064KB-A (64P6Q-A)	
M38039GCHKP			PLQP0064GA-A (64P6U-A)	
M38039GCHWG			PTLG0064JA-A (64F0G)	

NOTES:
1. This means a shipment of which User ROM has been programmed.
2. The user ROM area of a blank product is blank.
3. ROM size includes the ID code protect area.

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is “1”.

Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can execute decimal arithmetic.

Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to –128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

MISRG

(1) Bit 0 of address 0010$_{16}$: Oscillation stabilizing time set after STP instruction released bit

When the MCU stops the clock oscillation by the STP instruction and the STP instruction has been released by an external interrupt source, usually, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = 01$_{16}$, Prescaler 12 = FF$_{16}$) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by setting "1" to bit 0 of MISRG (address 0010$_{16}$).
However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.
Figure 10 shows the structure of MISRG.

(2) Bits 1, 2, 3 of address 0010$_{16}$: Middle-speed Mode Automatic Switch Function

In order to switch the clock mode of an MCU which has a sub-clock, the following procedure is necessary:
set CPU mode register (003B$_{16}$) --> start main clock oscillation --> wait for oscillation stabilization --> switch to middle-speed mode (or high-speed mode).
However, the 3803 group (Spec.H QzROM version) has the built-in function which automatically switches from low to middle-speed mode by program.

• Middle-speed mode automatic switch by program

The middle-speed mode can also be automatically switched by program while operating in low-speed mode. By setting the middle-speed automatic switch start bit (bit 3) of MISRG (address 0010$_{16}$) to "1" in the condition that the middle-speed mode automatic switch set bit is "1" while operating in low-speed mode, the MCU will automatically switch to middle-speed mode. In this case, the oscillation stabilizing time of the main clock can be selected by the middle-speed automatic switch wait time set bit (bit 2) of MISRG (address 0010$_{16}$).

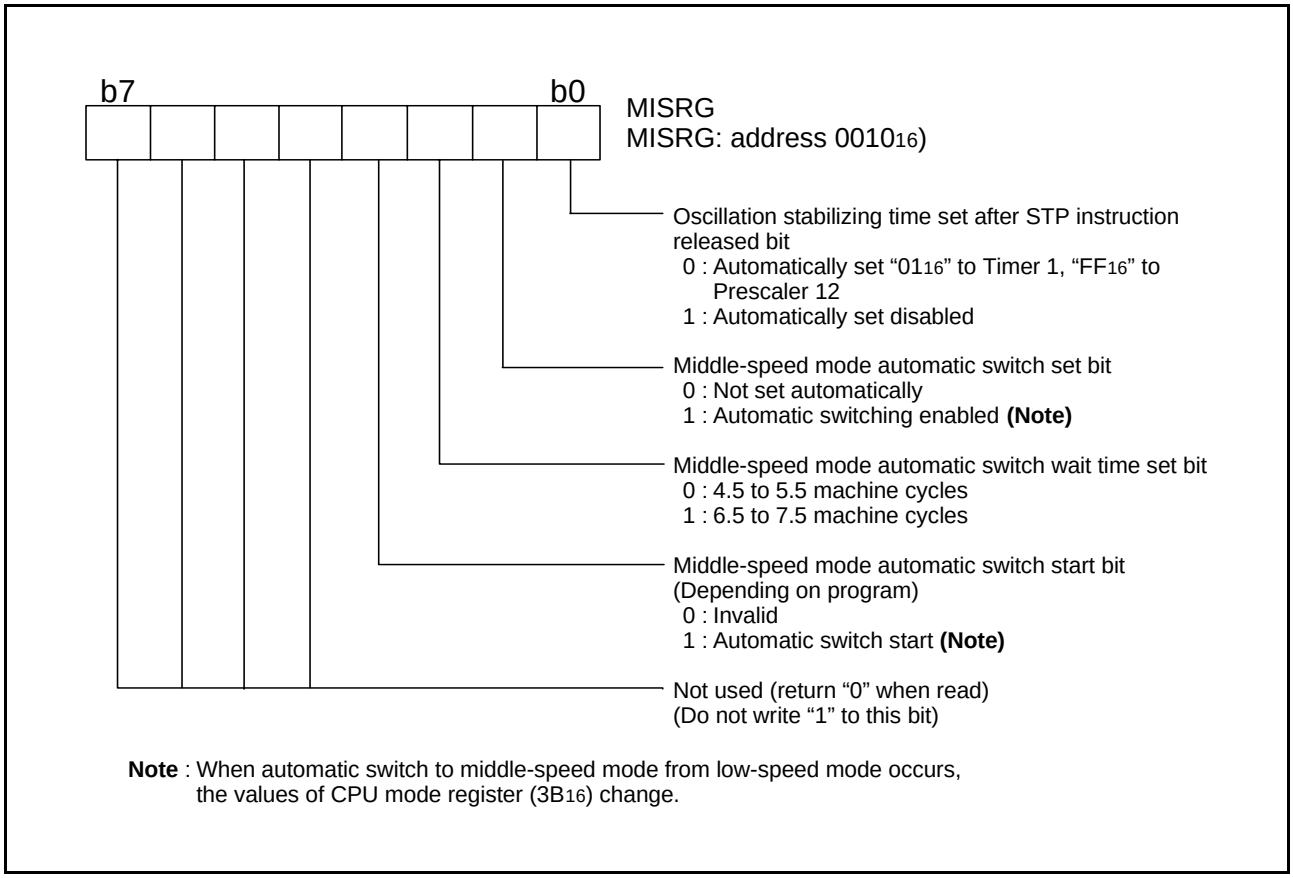


Fig 10. Structure of MISRG

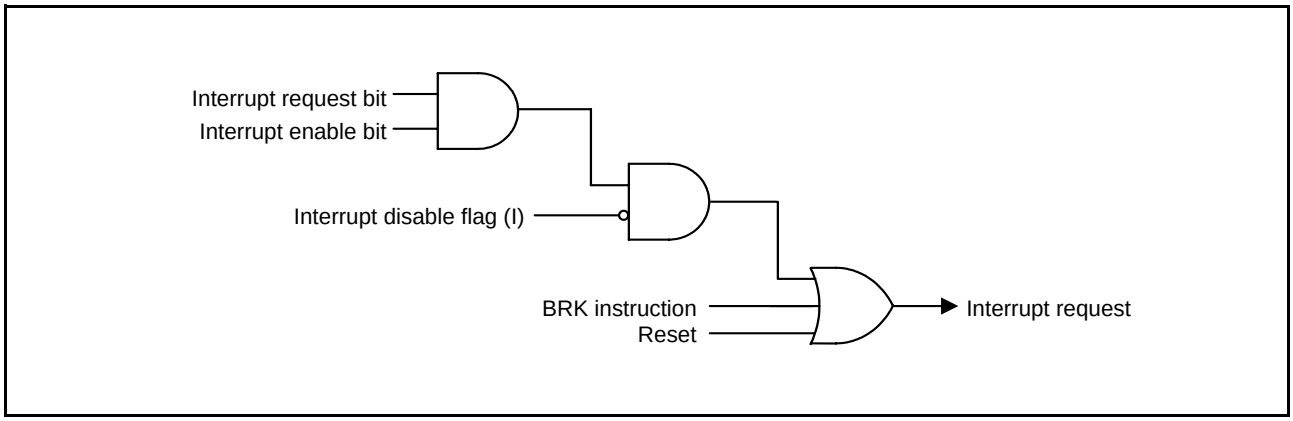


Fig 20. Interrupt control diagram

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", acceptance of interrupt requests is enabled. This flag is set to "1" with the SET instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled. To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", acceptance of the corresponding interrupt request is enabled.

Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

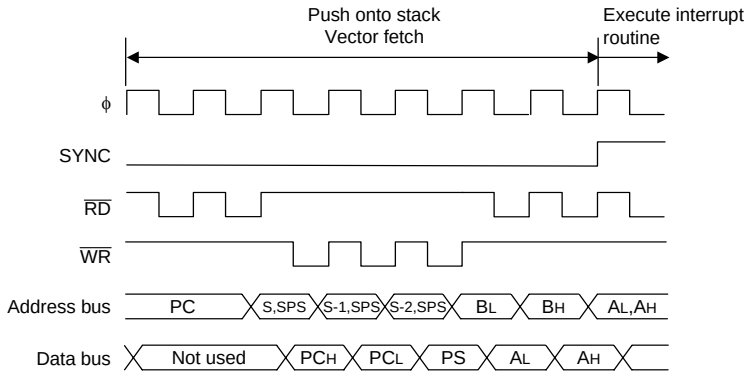
• Interrupt Source Selection

Any of the following combinations can be selected by the interrupt source selection register (0039_{16}).

1. INT_0 or timer Z
2. $CNTR_1$ or Serial I/O3 reception
3. Serial I/O2 or timer Z
4. INT_4 or $CNTR_2$
5. A/D conversion or serial I/O3 transmission

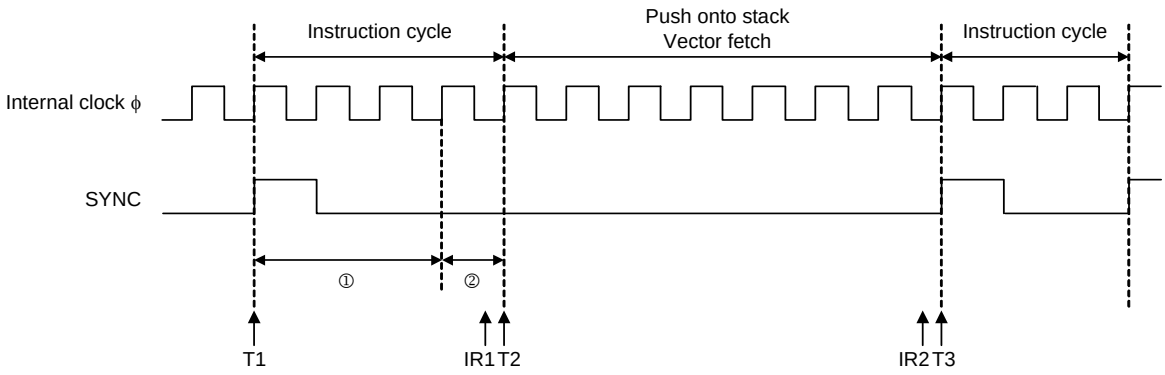
• External Interrupt Pin Selection

For external interrupts INT_0 and INT_4, the INT_0, INT_4 interrupt switch bit in the interrupt edge selection register (bit 6 of address $003A_{16}$) can be used to select INT_{00} and INT_{40} pin input or INT_{01} and INT_{41} pin input.



SYNC : CPU operation code fetch cycle
(This is an internal signal that cannot be observed from the external unit.)
BL, BH: Vector address of each interrupt
AL, AH: Jump destination address of each interrupt
SPS : "00_{16}" or "01_{16}"
([SPS] is a page selected by the stack page selection bit of CPU mode register.)

Fig 23. Interrupt sequence



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig 24. Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

<Notes>

The interrupt request bit may be set to "1" in the following cases.

- When setting the external interrupt active edge
  Related bits:
  INT_0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register (address $003A_{16}$))
  INT_1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register (address $003A_{16}$))
  INT_2 interrupt edge selection bit
  (bit 3 of interrupt edge selection register (address $003A_{16}$))
  INT_3 interrupt edge selection bit
  (bit 4 of interrupt edge selection register (address $003A_{16}$))
  INT_4 interrupt edge selection bit
  (bit 5 of interrupt edge selection register (address $003A_{16}$))
  $CNTR_0$ activate edge switch bit
  (bit 2 of timer XY mode register (address 0023_{16}))
  $CNTR_1$ activate edge switch bit
  (bits 6 of timer XY mode register (address 0023_{16}))
  $CNTR_2$ activate edge switch bit
  (bits 5 of timer Z mode register (address $002A_{16}$))

- When switching the interrupt sources of an interrupt vector address where two or more interrupt sources are assigned
  Related bits:
  INT_0, INT_4 interrupt switch bit
  (bit 6 of interrupt edge selection register (address $003A_{16}$))
  INT_0/Timer Z interrupt source selection bit
  (bit 0 of interrupt source selection register (address 0039_{16}))
  Serial I/O2/Timer Z interrupt source selection bit
  (bit 1 of interrupt source selection register (address 0039_{16}))
  INT_4/$CNTR_2$ interrupt source selection bit
  (bit 4 of interrupt source selection register (address 0039_{16}))
  $CNTR_1$/Serial I/O3 receive interrupt source selection bit
  (bit 6 of interrupt source selection register (address 0039_{16}))
  AD conversion/Serial I/O3 transmit interrupt source selection bit
  (bit 6 of interrupt source selection register (address 0039_{16}))

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

(1) Set the corresponding enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to "1" (enabled).

TIMERS

8-bit Timers

The 3803 group (Spec.H QzROM version) has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.
The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.
The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch. All timers are down-counters. When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

• Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address 003B$_{16}$). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X_{IN} is selected. When these bits are "10" (low-speed mode), X_{CIN} is selected.

• Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of f(X_{IN}) or f(X_{CIN}).

• Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

• Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or f(X_{CIN}). The count source is selected by the timer 12, X count source selection register (address 000E$_{16}$) and the timer Y, Z count source selection register (address 000F$_{16}$) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of f(X_{IN}) or f(X_{CIN}); and f(X_{CIN}).

• Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023$_{16}$).

(1) Timer mode

• Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

• Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023$_{16}$).
When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

(2) Pulse Output Mode

• Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

• Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR$_0$/CNTR$_1$ pin. Regardless of the timer counting or not the output of CNTR$_0$/CNTR$_1$ pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the CNTR$_0$ active edge switch bit (bit 2) and the CNTR$_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023$_{16}$) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.
Switching the CNTR$_0$ or CNTR$_1$ active edge switch bit will reverse the output level of the corresponding CNTR$_0$ or CNTR$_1$ pin.

• Precautions

Set the double-function port of CNTR$_0$/CNTR$_1$ pin and port P5$_4$/P5$_5$ to output in this mode.

(3) Event Counter Mode

• Mode selection

This mode can be selected by setting "10" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023$_{16}$).

• Explanation of operation

The operation is the same as the timer mode's except that the timer counts signals input from the CNTR$_0$ or CNTR$_1$ pin. The valid edge for the count operation depends on the CNTR$_0$ active edge switch bit (bit 2) or the CNTR$_1$ active edge switch bit (bit 6) of the timer XY mode register (address 0023$_{16}$). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

• Precautions

Set the double-function port of CNTR$_0$/CNTR$_1$ pin and port P5$_4$/P5$_5$ to input in this mode.

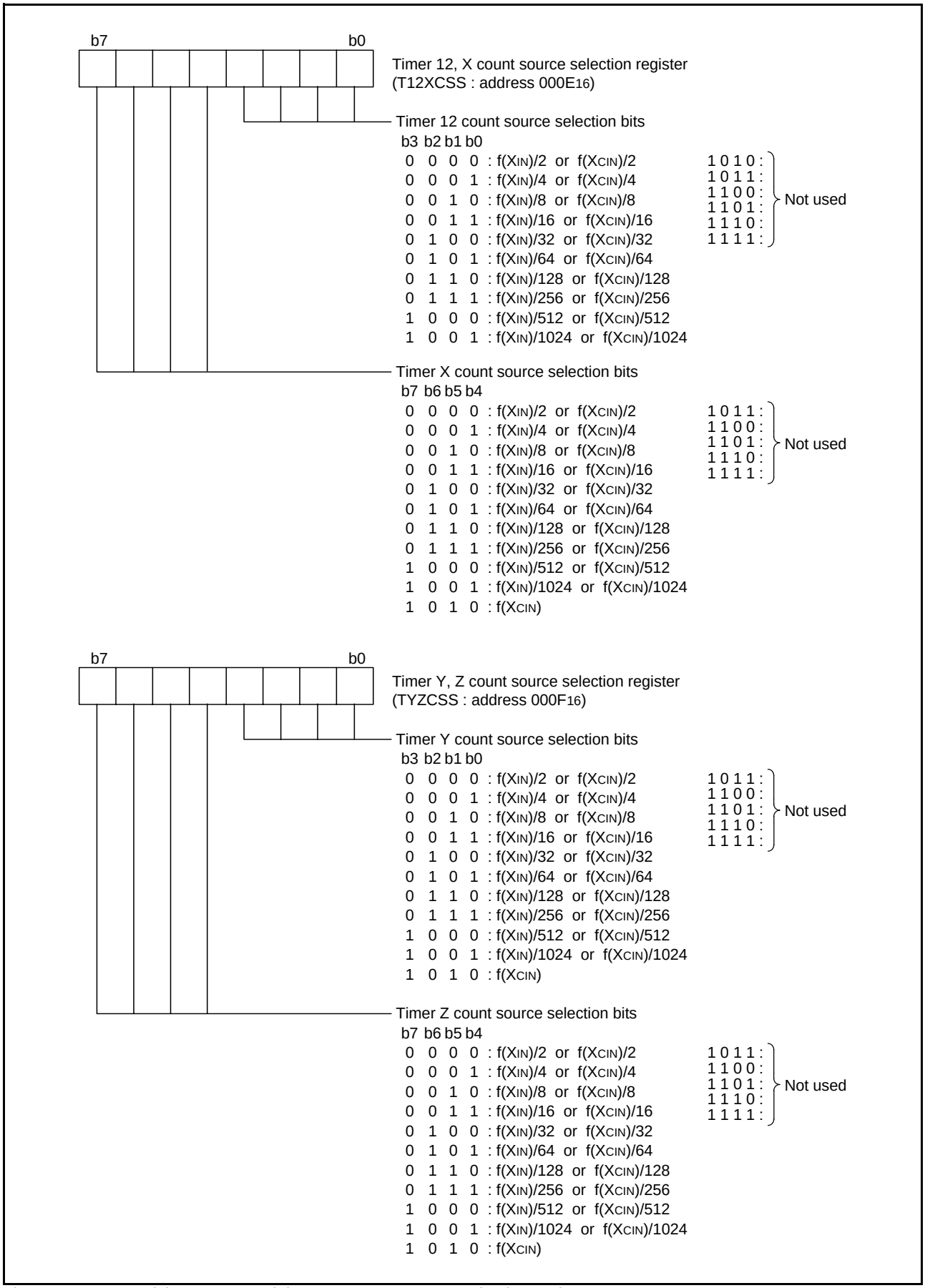


Fig 27. Structure of timer 12, X and timer Y, Z count source selection registers

<Notes regarding all modes>

• Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

• Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped. However, a read-out of timer latch value is impossible.

• Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

• Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

• Usage of CNTR2 pin as normal I/O port P47

To use the CNTR2 pin as normal I/O port P47, set timer Z operating mode bits (b2, b1, b0) of timer Z mode register (address 002A16) to "000".

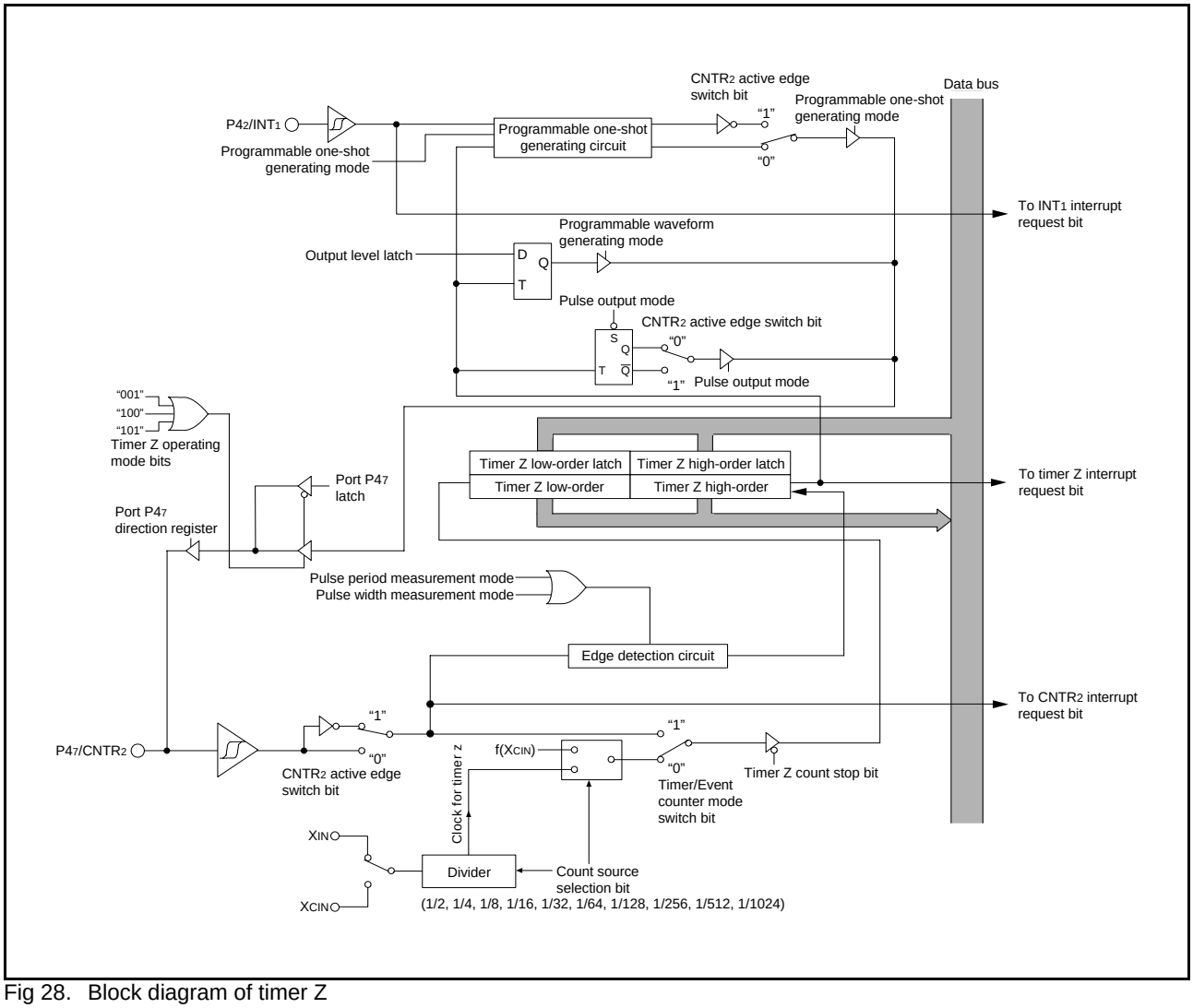


Fig 28. Block diagram of timer Z

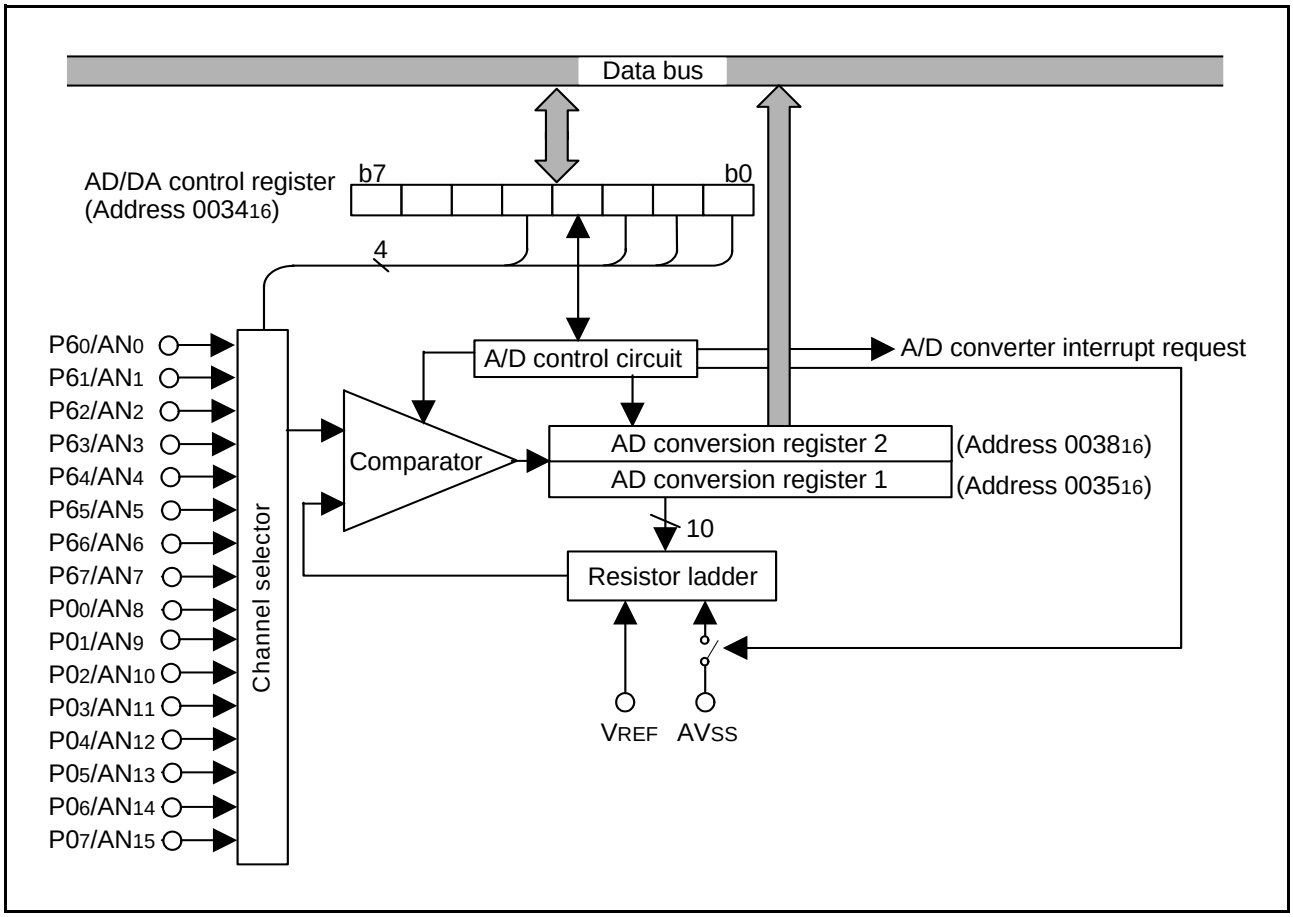


Fig 56. Block diagram of A/D converter

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 16 cycles or more of XIN. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 1.8 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.29 V for VCC of 1.8 V.

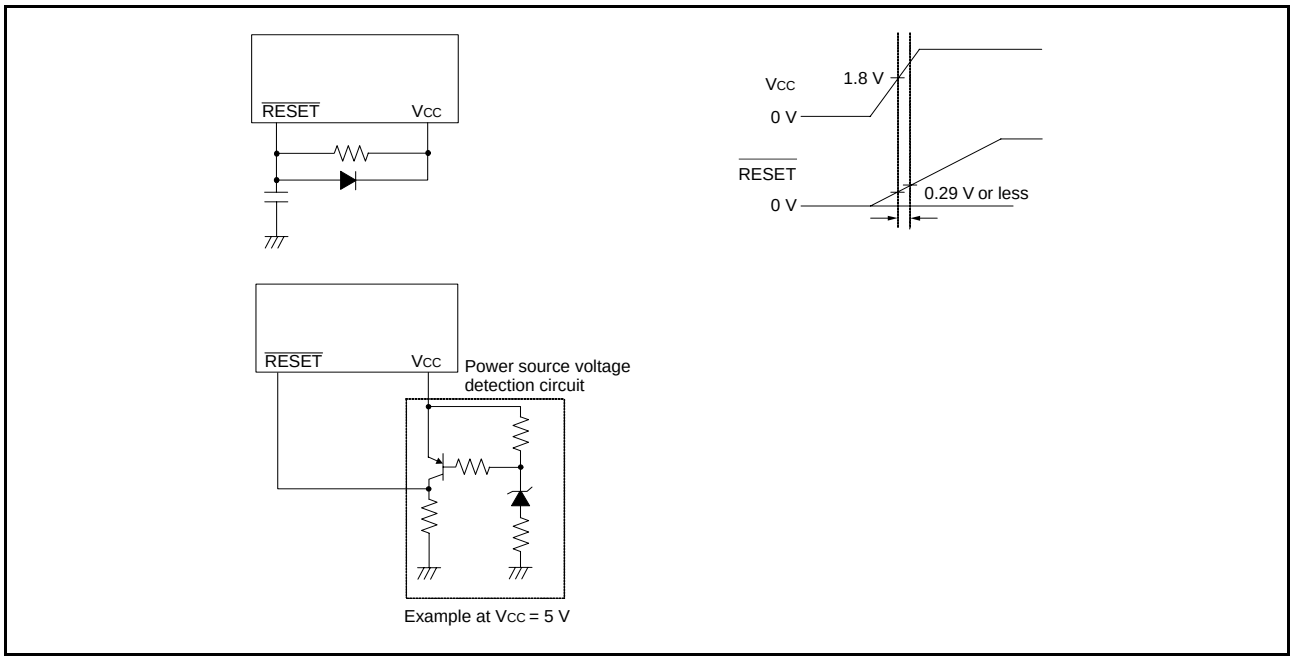
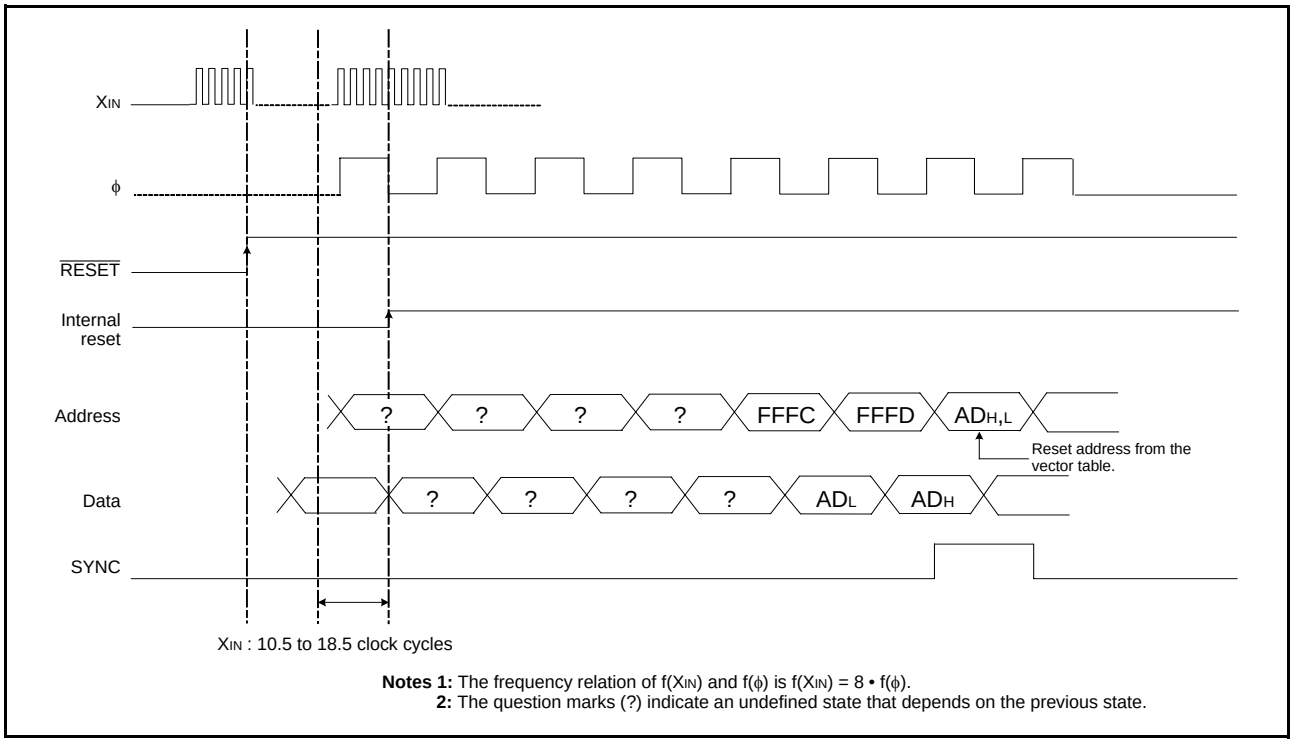


Fig 61. Reset circuit example



Notes 1: The frequency relation of f(XIN) and f(ϕ) is f(XIN) = 8 • f(ϕ).
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig 62. Reset sequence

CLOCK GENERATING CIRCUIT

The 3803 group (Spec.H QzROM version) has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip.(An external feed-back resistor may be needed depending on conditions.) However, an external feed-back resistor is needed between XCIN and XCOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

• Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.
The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit (bit 0 of address 0010_{16}) is "0", the prescaler 12 is set to "FF_{16}" and timer 1 is set to "01_{16}". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.
After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.
When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

<Notes>

- If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3×f(XCIN).
- When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.
- When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

6. Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the SRDY signal, set the transmit enable bit, the receive enable bit, and the SRDY output enable bit to "1".
Serial I/O1 continues to output the final bit from the TxD1 pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.
When in serial I/Os 1 and 3 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is "H".

7. A/D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.
Therefore, make sure that f(XIN) in the middle/high-speed mode is at least on 500 kHz during an A/D conversion.
Do not execute the STP instruction during an A/D conversion.

8. D/A Converter

The accuracy of the D/A converter becomes rapidly poor under the VCC = 4.0 V or less condition; a supply voltage of VCC ≥ 4.0 V is recommended. When a D/A converter is not used, set all values of DAi conversion registers (i=1, 2) to "0016".

9. Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The period of the internal clock ϕ is double of the XIN period in high-speed mode.

10.Reserved Area, Reserved Bit

Do not write any data to the reserved area in the SFR area and the special page. (Do not change the contents after reset.)

11.CPU Mode Register

Be sure to fix bit 3 of the CPU mode register (address 003B16) to "1".

COUNTERMEASURES AGAINST NOISE

(1) Shortest wiring length

1. Wiring for $\overline{\text{RESET}}$ pin
   Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the VSS pin with the shortest possible wiring (within 20 mm).

• Reason
The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

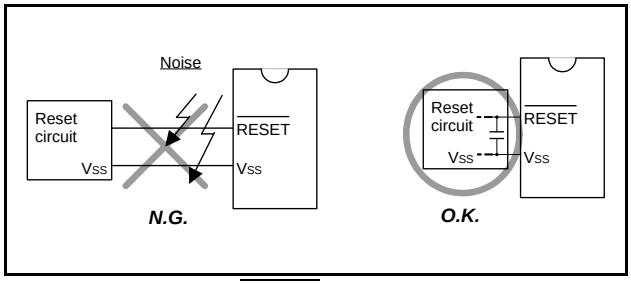


Fig. 76 Wiring for the $\overline{\text{RESET}}$ pin

2. Wiring for clock input/output pins
   - Make the length of wiring which is connected to clock I/O pins as short as possible.
   - Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the VSS pin of a microcomputer as short as possible.
   - Separate the VSS pattern only for oscillation from other VSS patterns.

• Reason
If noise enters clock I/O pins, clock waveforms may be deformed.
This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the VSS level of a microcomputer and the VSS level of an oscillator, the correct clock will not be input in the microcomputer.

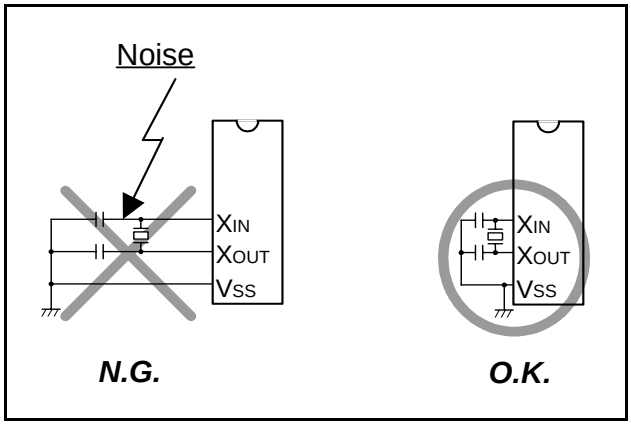


Fig. 77 Wiring for clock I/O pins

(2) Connection of bypass capacitor across VSS line and VCC line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 µF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

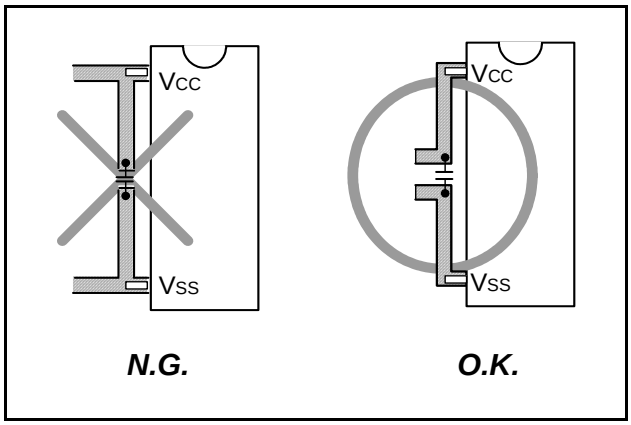


Fig. 78 Bypass capacitor across the VSS line and the VCC line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage and temperature is wide.

Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

1. Keeping oscillator away from large current signal lines
   Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

• Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

2. Installing oscillator away from signal lines where potential levels change frequently
   Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

• Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

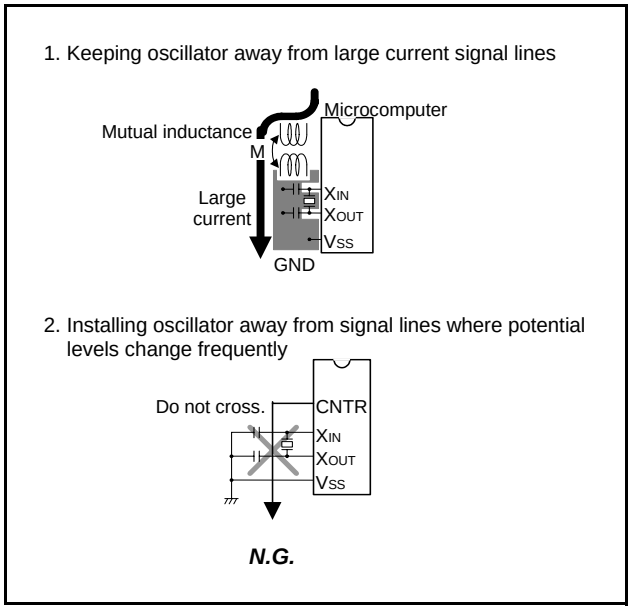


Fig. 79 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory size

When memory size differ in one group, actual values such as an electrical characteristics, A/D conversion accuracy, and the amount of proof of noise incorrect operation may differ from the ideal values.

When these products are used switching, perform system evaluation for each product of every after confirming product specification.

Notes on Interrupts

1. Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address 003A16)
- Timer XY mode register (address 002316)
- Timer Z mode register (address 002A16)

Set the above listed registers or bits as the following sequence.

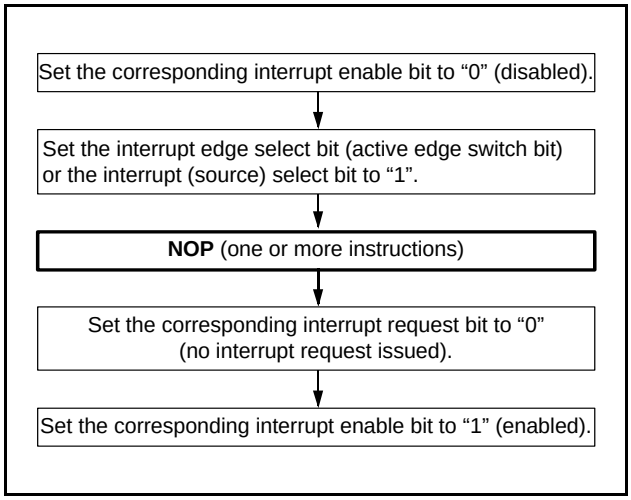


Fig 80. Sequence of changing relevant register

<Reason>
The interrupt request bit may be set to "1" in the following cases.

- When setting the external interrupt active edge
  Related bits:
  INT0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register (address 003A16))
  INT1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register (address 003A16))
  INT2 interrupt edge selection bit
  (bit 3 of interrupt edge selection register (address 003A16))
  INT3 interrupt edge selection bit
  (bit 4 of interrupt edge selection register (address 003A16))
  INT4 interrupt edge selection bit
  (bit 5 of interrupt edge selection register (address 003A16))
  CNTR0 activate edge switch bit
  (bit 2 of timer XY mode register (address 002316))
  CNTR1 activate edge switch bit
  (bits 6 of timer XY mode register (address 002316))
  CNTR2 activate edge switch bit
  (bits 5 of timer Z mode register (address 002A16))
- When switching the interrupt sources of an interrupt vector address where two or more interrupt sources are assigned
  Related bits:
  INT0, INT4 interrupt switch bit
  (bit 6 of interrupt edge selection register (address 003A16))
  INT0/Timer Z interrupt source selection bit
  (bit 0 of interrupt source selection register (address 003916))
  Serial I/O2/Timer Z interrupt source selection bit
  (bit 1 of interrupt source selection register (address 003916))
  INT4/CNTR2 interrupt source selection bit
  (bit 4 of interrupt source selection register (address 003916))
  CNTR1/Serial I/O3 receive interrupt source selection bit
  (bit 6 of interrupt source selection register (address 003916))
  AD conversion/Serial I/O3 transmit interrupt source selection bit
  (bit 6 of interrupt source selection register (address 003916))

2. Check of interrupt request bit

When executing the BBC or BBS instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to "0", execute one or more instructions before executing the BBC or BBS instruction.

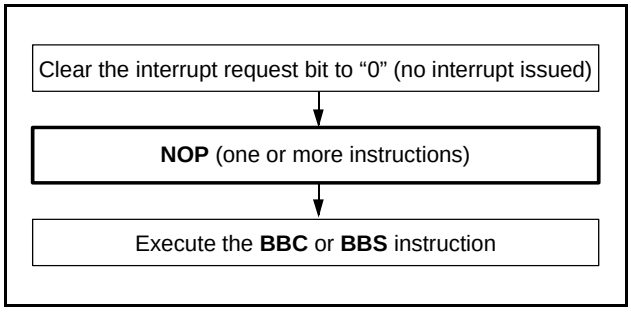


Fig 81. Sequence of check of interrupt request bit

<Reason>
If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

Notes on 8-bit Timer (timer 1, 2, X, Y)

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.
  Therefore, select the timer count source before set the value to the prescaler and the timer.
- Set the double-function port of the CNTR0/CNTR1 pin and port P54/P55 to output in the pulse output mode.
- Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in the event counter mode and the pulse width measurement mode.

3. Clock frequency during A/D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A/D conversion.

- f(XIN) is 500 kHz or more
- Do not execute the STP instruction

4. Difference between at 8-bit reading in 10-bit A/D mode and at 8-bit A/D mode

At 8-bit reading in the 10-bit A/D mode, "–1/2 LSB" correction is not performed to the A/D conversion result.
In the 8-bit A/D mode, the A/D conversion characteristics is the same as 3802 group's characteristics because "–1/2 LSB" correction is performed.

Notes on D/A Converter

1. VCC when using D/A converter

The D/A converter accuracy when VCC is 4.0 V or less differs from that of when VCC is 4.0 V or more. When using the D/A converter, we recommend using a VCC of 4.0 V or more.

2. D/Ai conversion register when not using D/A converter

When a D/A converter is not used, set all values of the D/Ai conversion registers (i = 1, 2) to "00$_{16}$". The initial value after reset is "00$_{16}$".

Notes on Watchdog Timer

- Make sure that the watchdog timer H does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.
- When the STP instruction function selection bit has been set to "1", it is impossible to switch it to "0" by a program.

Notes on $\overline{\text{RESET}}$ Pin

Connecting capacitor
In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the VSS pin.
Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following:

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

Notes on Low-speed Operation Mode

1. Using sub-clock

To use a sub-clock, fix bit 3 of the CPU mode register to "1" or control the Rd (refer to Figure 83) resistance value to a certain level to stabilize an oscillation. For resistance value of Rd, consult the oscillator manufacturer.

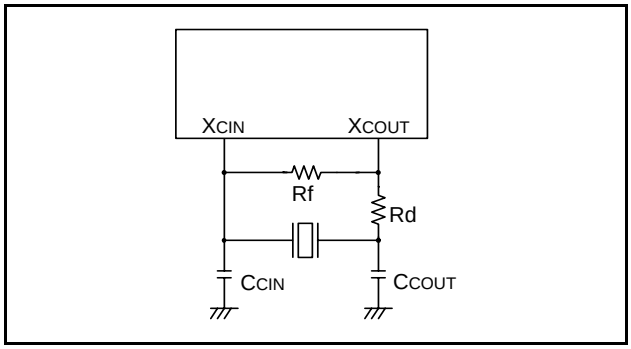


Fig 83. Ceramic resonator circuit

<Reason>
When bit 3 of the CPU mode register is set to "0", the sub-clock oscillation may stop.

2. Switch between middle/high-speed mode and low-speed mode

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3×f(XCIN).

Quartz-Crystal Oscillator

When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.

Notes on Restarting Oscillation

- Restarting oscillation

Usually, when the MCU stops the clock oscillation by STP instruction and the STP instruction has been released by an external interrupt source, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = "01$_{16}$", Prescaler 12 = "FF$_{16}$") are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by writing "1" to bit 0 of MISRG (address 0010$_{16}$).
However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.
<Reason>
Oscillation will restart when an external interrupt is received. However, internal clock ϕ is supplied to the CPU only when Timer 1 starts to underflow. This ensures time for the clock oscillation using the ceramic resonators to be stabilized.

Timing requirements and switching characteristics

Table 18 Timing requirements (1)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width		16			X_{IN} cycle
$t_{C(XIN)}$	Main clock X_{IN} input cycle time	4.5 ≤ V_{CC} ≤ 5.5 V	59.5			ns
		4.0 ≤ V_{CC} < 4.5 V	10000/(86 V_{CC} – 219)			
		2.7 ≤ V_{CC} < 4.0 V	26 × 10^3/(82 V_{CC} - 3)			
		2.2 ≤ V_{CC} < 2.7 V	10000/(84 V_{CC} – 143)			
		2.0 ≤ V_{CC} < 2.2 V	10000/(105 V_{CC} – 189)			
$t_{WH(XIN)}$	Main clock X_{IN} input “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	25			ns
		4.0 ≤ V_{CC} < 4.5 V	4000/(86 V_{CC} – 219)			
		2.7 ≤ V_{CC} < 4.0 V	10000/(82 V_{CC} – 3)			
		2.2 ≤ V_{CC} < 2.7 V	4000/(84 V_{CC} – 143)			
		2.0 ≤ V_{CC} < 2.2 V	4000/(105 V_{CC} – 189)			
$t_{WL(XIN)}$	Main clock X_{IN} input “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	25			ns
		4.0 ≤ V_{CC} < 4.5 V	4000/(86 V_{CC} – 219)			
		2.7 ≤ V_{CC} < 4.0 V	10000/(82 V_{CC} – 3)			
		2.2 ≤ V_{CC} < 2.7 V	4000/(84 V_{CC} – 143)			
		2.0 ≤ V_{CC} < 2.2 V	4000/(105 V_{CC} – 189)			
$t_{C(XCIN)}$	Sub-clock X_{CIN} input cycle time		20			μs
$t_{WH(XCIN)}$	Sub-clock X_{CIN} input “H” pulse width		5			μs
$t_{WL(XCIN)}$	Sub-clock X_{CIN} input “L” pulse width		5			μs
$t_{C(CNTR)}$	$CNTR_0$–$CNTR_2$ input cycle time	4.5 ≤ V_{CC} ≤ 5.5 V	120			ns
		4.0 ≤ V_{CC} < 4.5 V	160			
		2.7 ≤ V_{CC} < 4.0 V	250			
		2.2 ≤ V_{CC} < 2.7 V	500			
		2.0 ≤ V_{CC} < 2.2 V	1000			
$t_{WH(CNTR)}$	$CNTR_0$–$CNTR_2$ input “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			
$t_{WL(CNTR)}$	$CNTR_0$–$CNTR_2$ input “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			
$t_{WH(INT)}$	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			
$t_{WL(INT)}$	INT_{00}, INT_{01}, INT_1, INT_2, INT_3, INT_{40}, INT_{41} input “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	48			ns
		4.0 ≤ V_{CC} < 4.5 V	64			
		2.7 ≤ V_{CC} < 4.0 V	115			
		2.2 ≤ V_{CC} < 2.7 V	230			
		2.0 ≤ V_{CC} < 2.2 V	460			

Table 20 Switching characteristics (1)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = 0V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$ $t_{WH}(S_{CLK3})$	Serial I/O1, serial I/O3 clock output “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	Fig.87	$t_C(S_{CLK1})$/2-30, $t_C(S_{CLK3})$/2-30			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK1})$/2-35, $t_C(S_{CLK3})$/2-35			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK1})$/2-40, $t_C(S_{CLK3})$/2-40			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK1})$/2-45, $t_C(S_{CLK3})$/2-45			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK1})$/2-50, $t_C(S_{CLK3})$/2-50			
$t_{WL}(S_{CLK1})$ $t_{WL}(S_{CLK3})$	Serial I/O1, serial I/O3 clock output “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK1})$/2-30, $t_C(S_{CLK3})$/2-30			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK1})$/2-35, $t_C(S_{CLK3})$/2-35			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK1})$/2-40, $t_C(S_{CLK3})$/2-40			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK1})$/2-45, $t_C(S_{CLK3})$/2-45			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK1})$/2-50, $t_C(S_{CLK3})$/2-50			
$t_d(S_{CLK1}\text{-}T_xD_1)$ $t_d(S_{CLK3}\text{-}T_xD_3)$	Serial I/O1, serial I/O3 output delay time(1)	4.5 ≤ V_{CC} ≤ 5.5 V				140	ns
		4.0 ≤ V_{CC} < 4.5 V				200	
		2.7 ≤ V_{CC} < 4.0 V				350	
		2.2 ≤ V_{CC} < 2.7 V				400	
		2.0 ≤ V_{CC} < 2.2 V				420	
$t_v(S_{CLK1}\text{-}T_xD_1)$ $t_v(S_{CLK3}\text{-}T_xD_3)$	Serial I/O1, serial I/O3 output valid time(1)	4.5 ≤ V_{CC} ≤ 5.5 V		−30			ns
		4.0 ≤ V_{CC} < 4.5 V		−30			
		2.7 ≤ V_{CC} < 4.0 V		−30			
		2.2 ≤ V_{CC} < 2.7 V		−30			
		2.0 ≤ V_{CC} < 2.2 V		−30			
$t_r(S_{CLK1})$ $t_r(S_{CLK3})$	Serial I/O1, serial I/O3 rise time of clock output	4.5 ≤ V_{CC} ≤ 5.5 V				30	ns
		4.0 ≤ V_{CC} < 4.5 V				35	
		2.7 ≤ V_{CC} < 4.0 V				40	
		2.2 ≤ V_{CC} < 2.7 V				45	
		2.0 ≤ V_{CC} < 2.2 V				50	
$t_f(S_{CLK1})$ $t_f(S_{CLK3})$	Serial I/O1, serial I/O3 fall time of clock output	4.5 ≤ V_{CC} ≤ 5.5 V				30	ns
		4.0 ≤ V_{CC} < 4.5 V				35	
		2.7 ≤ V_{CC} < 4.0 V				40	
		2.2 ≤ V_{CC} < 2.7 V				45	
		2.0 ≤ V_{CC} < 2.2 V				50	
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK2})$/2-160			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK2})$/2-200			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK2})$/2-240			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK2})$/2-260			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK2})$/2-280			
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK2})$/2-160			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK2})$/2-200			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK2})$/2-240			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK2})$/2-260			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK2})$/2-280			
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time	4.5 ≤ V_{CC} ≤ 5.5 V				200	ns
		4.0 ≤ V_{CC} < 4.5 V				250	
		2.7 ≤ V_{CC} < 4.0 V				300	
		2.2 ≤ V_{CC} < 2.7 V				350	
		2.0 ≤ V_{CC} < 2.2 V				400	
$t_v(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	4.5 ≤ V_{CC} ≤ 5.5 V			0		ns
		4.0 ≤ V_{CC} < 4.5 V			0		
		2.7 ≤ V_{CC} < 4.0 V			0		
		2.2 ≤ V_{CC} < 2.7 V			0		
		2.0 ≤ V_{CC} < 2.2 V			0		

NOTES:
1. When the $P4_5/T_xD_1$ P-channel output disable bit of the UART1 control register (bit 4 of address $001B_{16}$) is “0”.