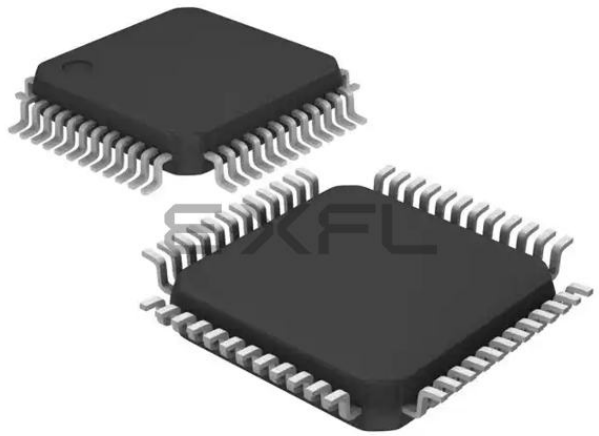
Nuvoton Technology Corporation - NUC140LC1CN Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc140lc1cn

- Timer
  - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Support event counting function
  - Support input capture function
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time out period from 1.6ms ~ 26.0sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable on watchdog time-out
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Support wake-up function
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
  - Support Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Support IrDA (SIR) and LIN function
  - Support RS-485 9-bit mode and direction control.
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode
- SPI
  - Up to four sets of SPI controller
  - Master up to 32 MHz, and Slave up to 10 MHz (chip working @ 5V)
  - Support SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Support byte suspend mode in 32-bit transmission
  - Support PDMA mode
  - Support three wire, no slave select signal, bi-direction interface

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC140 Products Selection Guide

3.1.1 NuMicro™ NUC140 Connectivity Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I^2C	USB	LIN	CAN								
NUC140LC1CN	32 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140LD2CN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140LE3CN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140RC1CN	32 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140RD2CN	64 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140RE3CN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140VE3CN	128 KB	16 KB	Definable	4 KB	up to 76	4x32-bit	3	4	2	1	2	1	1	2	8	8x12-bit	v	v	v	LQFP100

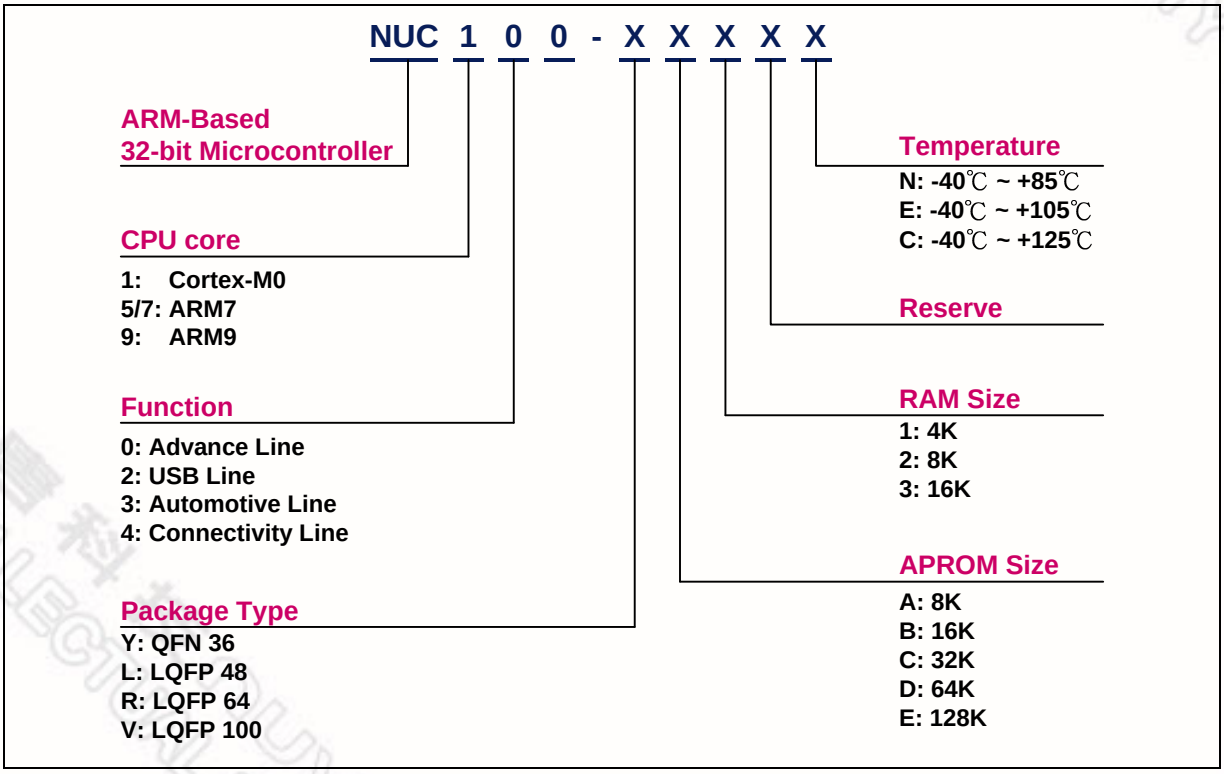


Figure 3-1 NuMicro™ NUC100 Series selection code

- Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC that features:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input.
  - Support for both level-sensitive and pulse-sensitive interrupt lines
  - Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 2.5 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and V_{DD33}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 5-2 shows the power distribution of NuMicro™ NUC140.

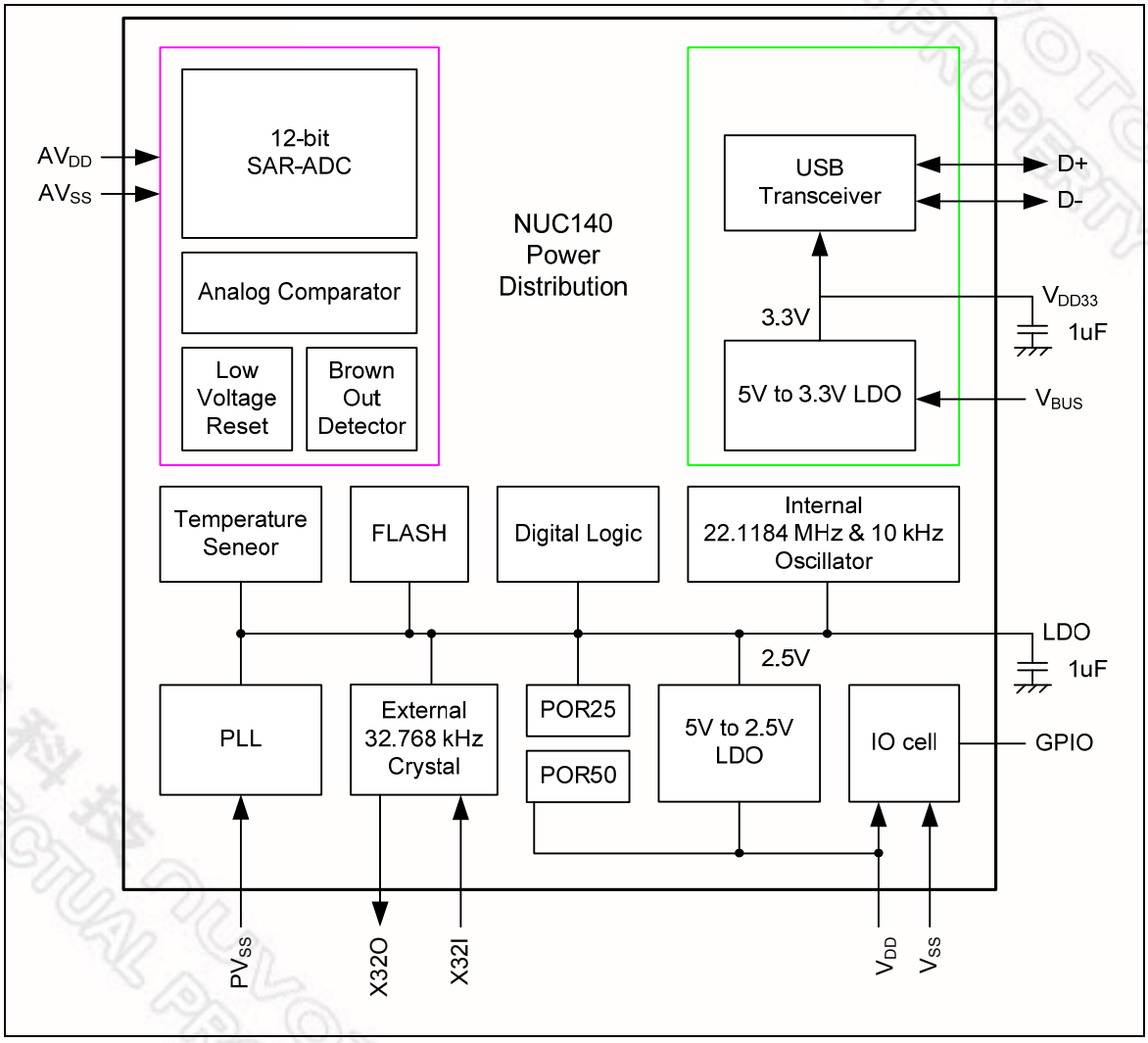


Figure 5-2 NuMicro™ NUC140 Power Distribution Diagram

5.2.5 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART02_INT**	UART0/2	UART0 and UART2 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt
30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**SPI2_INT**	SPI2	SPI2 interrupt
33	17	**SPI3_INT**	SPI3	SPI3 interrupt
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**CAN0_INT**	CAN0	CAN0 interrupt
37	21	**Reserved**	Reserved	Reserved
38	22	**Reserved**	Reserved	Reserved
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**ACMP_INT**	ACMP	Analog Comparator-0 or Comaprator-1 interrupt
42	26	**PDMA_INT**	PDMA	PDMA interrupt
43	27	**I2S_INT**	I^2S	I^2S interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from power down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**Reserved**	Reserved	Reserved
47	31	**RTC_INT**	RTC	Real time clock interrupt

Table 5-3 System Interrupt Map

5.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting which depends on the different peripheral. Please refer the CLKSEL1 and CLKSEL2 register description in 5.3.7.

5.3.5 Power Down Mode Clock

When chip enters into power down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in power down mode.

For theses clocks which still keep active list below:

- Clock Generator
  - Internal 10 kHz low speed oscillator clock
  - External 32.768 kHz low speed crystal clock
- Peripherals Clock (When these IP adopt external 32.768 kHz low speed crystal or 10 kHz low speed oscillator as clock source)

5.4 USB Device Controller (USB)

5.4.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. Users need to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (USB_BUFSEGx)”.

There are 6 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

Reference: Universal Serial Bus Specification Revision 1.1

5.4.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature listing of this USB.

- Compliant with USB 2.0 Full-Speed specification
- Provide 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Support Control/Bulk/Interrupt/Isochronous transfer type
- Support suspend function when no bus activity existing for 3 ms
- Provide 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provide remote wake-up capability

5.6.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows.
- External pull-up are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- I^2C-bus controllers support multiple address recognition (Four slave address with mask option)

5.7 PWM Generator and Capture Timer (PWM)

5.7.1 Overview

NuMicro™ NUC130/NUC140 has 2 sets of PWM group supports total 4 sets of PWM Generators which can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable dead-zone generators.

Each PWM Generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read

5.12.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake-up function (UART0 and UART1 support)
- Support 7-bit receiver buffer time out detection function
- UART0/UART1 can be served by the DMA controller
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Support IrDA SIR function mode
  - Support for 3-/16-bit duration for normal mode
- Support LIN function mode
  - Support LIN master/slave mode
  - Support programmable break generation function for transmitter
  - Support break detect function for receiver
- Support RS-485 function mode.
  - Support RS-485 9-bit mode
  - Support hardware or software direct enable control provided by RTS pin

5.15 I²S Controller (I²S)

5.15.1 Overview

The I²S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word deep FIFO for read path and write path respectively and is capable of handling 8 ~ 32 bit word sizes. DMA controller handles the data movement between FIFO and memory.

5.15.2 Features

- I²S can operate as either master or slave
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Mono and stereo audio data supported
- I²S and MSB justified data format supported
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two DMA requests, one for transmit and one for receive

5.17 Analog Comparator (CMP)

5.17.1 Overview

NuMicro™ NUC100 Series contains two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **Error! Reference source not found.**.

5.17.2 Features

- Analog input voltage range: 0~5.0 V
- Hysteresis function supported
- Two analog comparators with optional internal reference voltage input at negative end
- One interrupt vector for both comparators

5.19 External Bus Interface (EBI)

5.19.1 Overview

The NuMicro™ NUC130/NUC140 LQFP-64 and LQFP-100 package equips an external bus interface (EBI) for external device used.

To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

5.19.2 Features

External Bus Interface has the following functions:

- External devices with max. 64K-byte size (8-bit data width)/128K-byte (16-bit data width) supported
- Variable external bus base clock (MCLK) supported
- 8-bit or 16-bit data width supported
- Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

7 ELECTRICAL CHARACTERISTICS

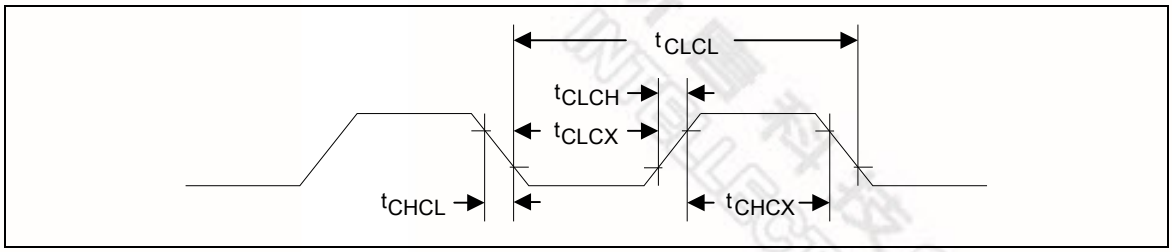
7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.3 AC Electrical Characteristics

7.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

7.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz@ V_{DD} = 5V	-	1	-	mA

7.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

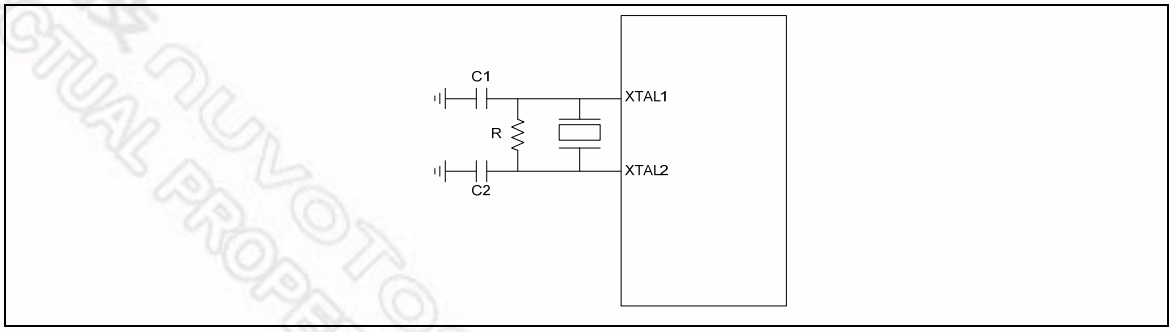


Figure 7-1 Typical Crystal Application Circuit

7.3.3 External 32.768 kHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	-	5.5	V

7.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	uA

7.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD}=5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25℃	1.7	2.0	2.3	V
	Temperature=-40℃	-	2.4	-	V
	Temperature=85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD}=5.5 V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.4.8 Specification of USB PHY

7.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

7.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	V_{DDD} and V_{DDREG} Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA