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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                                               |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Last Time Buy                                                                                                                                                                                 |
| Core Processor             | ARM® Cortex®-M0                                                                                                                                                                               |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                                            |
| Speed                      | 50MHz                                                                                                                                                                                         |
| Connectivity               | CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB                                                                                                                         |
| Peripherals                | Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT                                                                                                                                  |
| Number of I/O              | 45                                                                                                                                                                                            |
| Program Memory Size        | 64KB (64K x 8)                                                                                                                                                                                |
| Program Memory Type        | FLASH                                                                                                                                                                                         |
| EEPROM Size                | -                                                                                                                                                                                             |
| RAM Size                   | 8K x 8                                                                                                                                                                                        |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V                                                                                                                                                                                   |
| Data Converters            | A/D 8x12b                                                                                                                                                                                     |
| Oscillator Type            | Internal                                                                                                                                                                                      |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                                                                                                 |
| Package / Case             | 64-LQFP                                                                                                                                                                                       |
| Supplier Device Package    | -                                                                                                                                                                                             |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc140rd2cn">https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc140rd2cn</a> |

|      |        |                                                            |    |
|------|--------|------------------------------------------------------------|----|
|      | 5.8.1  | Overview .....                                             | 40 |
|      | 5.8.2  | Features .....                                             | 40 |
| 5.9  |        | Serial Peripheral Interface (SPI) .....                    | 41 |
|      | 5.9.1  | Overview .....                                             | 41 |
|      | 5.9.2  | Features .....                                             | 41 |
| 5.10 |        | Timer Controller (TMR) .....                               | 42 |
|      | 5.10.1 | Overview .....                                             | 42 |
|      | 5.10.2 | Features .....                                             | 42 |
| 5.11 |        | Watchdog Timer (WDT) .....                                 | 43 |
|      | 5.11.1 | Overview .....                                             | 43 |
|      | 5.11.2 | Features .....                                             | 45 |
| 5.12 |        | UART Interface Controller (UART) .....                     | 46 |
|      | 5.12.1 | Overview .....                                             | 46 |
|      | 5.12.2 | Features .....                                             | 48 |
| 5.13 |        | Controller Area Network (CAN) .....                        | 49 |
|      | 5.13.1 | Overview .....                                             | 49 |
|      | 5.13.2 | Features .....                                             | 49 |
| 5.14 |        | PS/2 Device Controller (PS2D) .....                        | 50 |
|      | 5.14.1 | Overview .....                                             | 50 |
|      | 5.14.2 | Features .....                                             | 50 |
| 5.15 |        | I <sup>2</sup> S Controller (I <sup>2</sup> S) .....       | 51 |
|      | 5.15.1 | Overview .....                                             | 51 |
|      | 5.15.2 | Features .....                                             | 51 |
| 5.16 |        | Analog-to-Digital Converter (ADC) .....                    | 52 |
|      | 5.16.1 | Overview .....                                             | 52 |
|      | 5.16.2 | Features .....                                             | 52 |
| 5.17 |        | Analog Comparator (CMP) .....                              | 53 |
|      | 5.17.1 | Overview .....                                             | 53 |
|      | 5.17.2 | Features .....                                             | 53 |
| 5.18 |        | PDMA Controller (PDMA) .....                               | 54 |
|      | 5.18.1 | Overview .....                                             | 54 |
|      | 5.18.2 | Features .....                                             | 54 |
| 5.19 |        | External Bus Interface (EBI) .....                         | 55 |
|      | 5.19.1 | Overview .....                                             | 55 |
|      | 5.19.2 | Features .....                                             | 55 |
| 6    |        | FLASH MEMORY CONTROLLER (FMC) .....                        | 56 |
|      | 6.1    | Overview .....                                             | 56 |
|      | 6.2    | Features .....                                             | 56 |
| 7    |        | ELECTRICAL CHARACTERISTICS .....                           | 57 |
|      | 7.1    | Absolute Maximum Ratings .....                             | 57 |
|      | 7.2    | DC Electrical Characteristics .....                        | 58 |
|      | 7.2.1  | NuMicro™ NUC130/NUC140 DC Electrical Characteristics ..... | 58 |

- Support byte write in 16-bit data width mode
- ADC
  - 12-bit SAR ADC with 700K SPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Support PDMA Mode
- Analog Comparator
  - Up to two analog comparators
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake-up
- One built-in temperature sensor with 1°C resolution
- Brown-Out detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brown-Out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40°C~85°C
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin

### 3.2 Pin Configuration

#### 3.2.1 NuMicro™ NUC140 Pin Diagram

##### 3.2.1.1 NuMicro™ NUC140 LQFP 100 pin

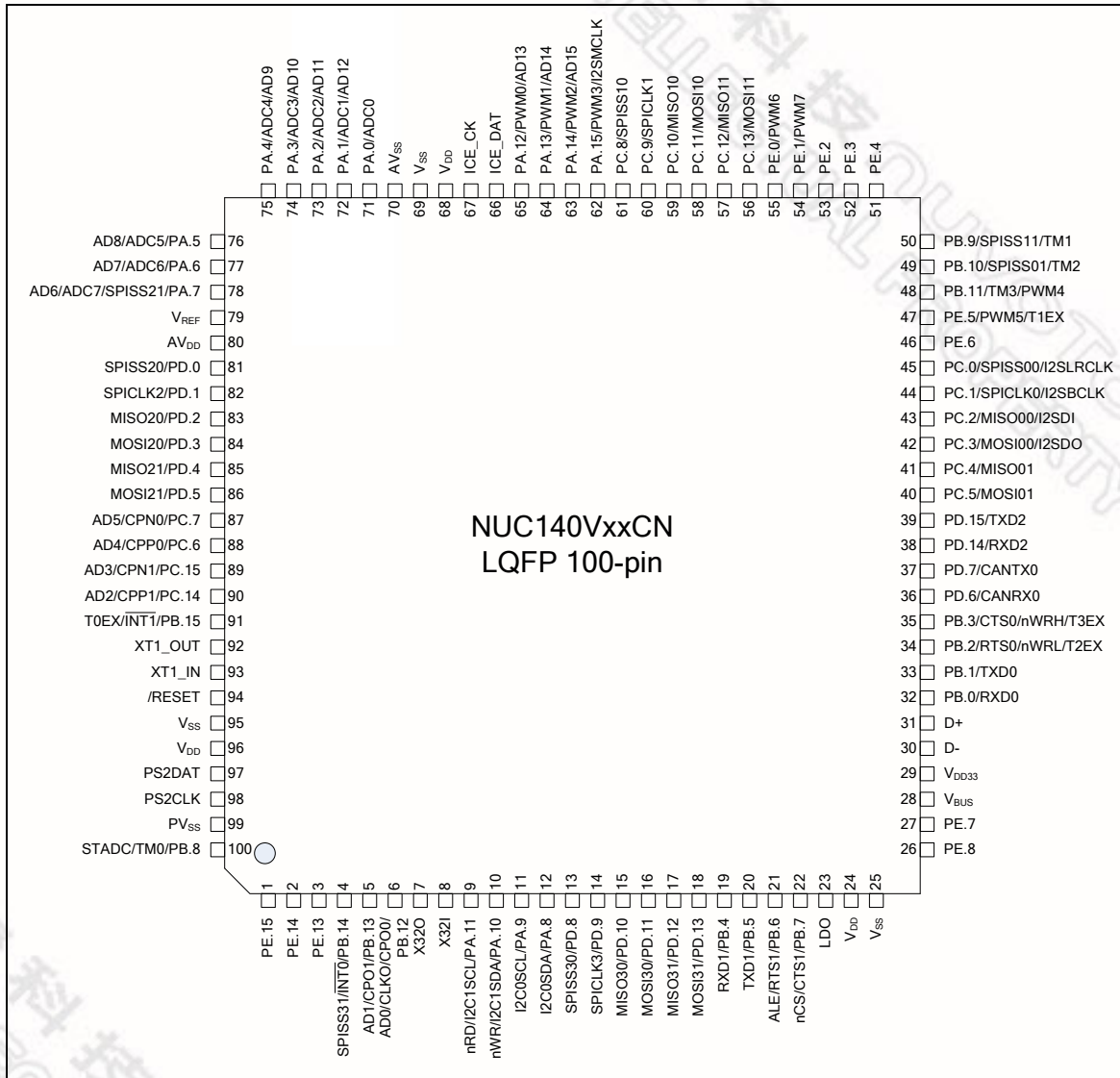


Figure 3-2 NuMicro™ NUC140 LQFP 100-pin Pin Diagram

## 3.2.1.2 NuMicro™ NUC140 LQFP 64 pin

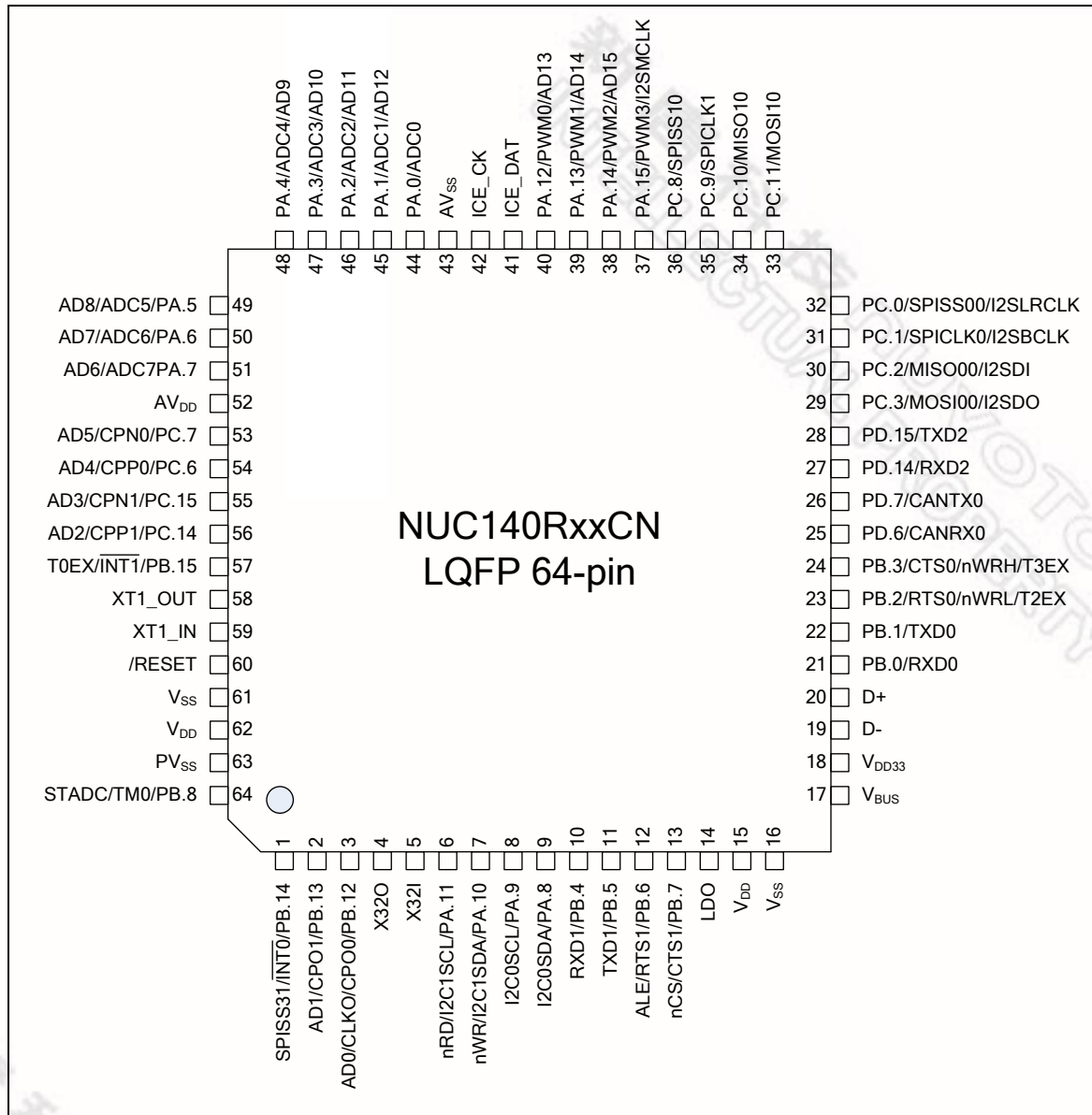


Figure 3-3 NuMicro™ NUC140 LQFP 64-pin Pin Diagram

## 3.2.1.3 NuMicro™ NUC140 LQFP 48 pin

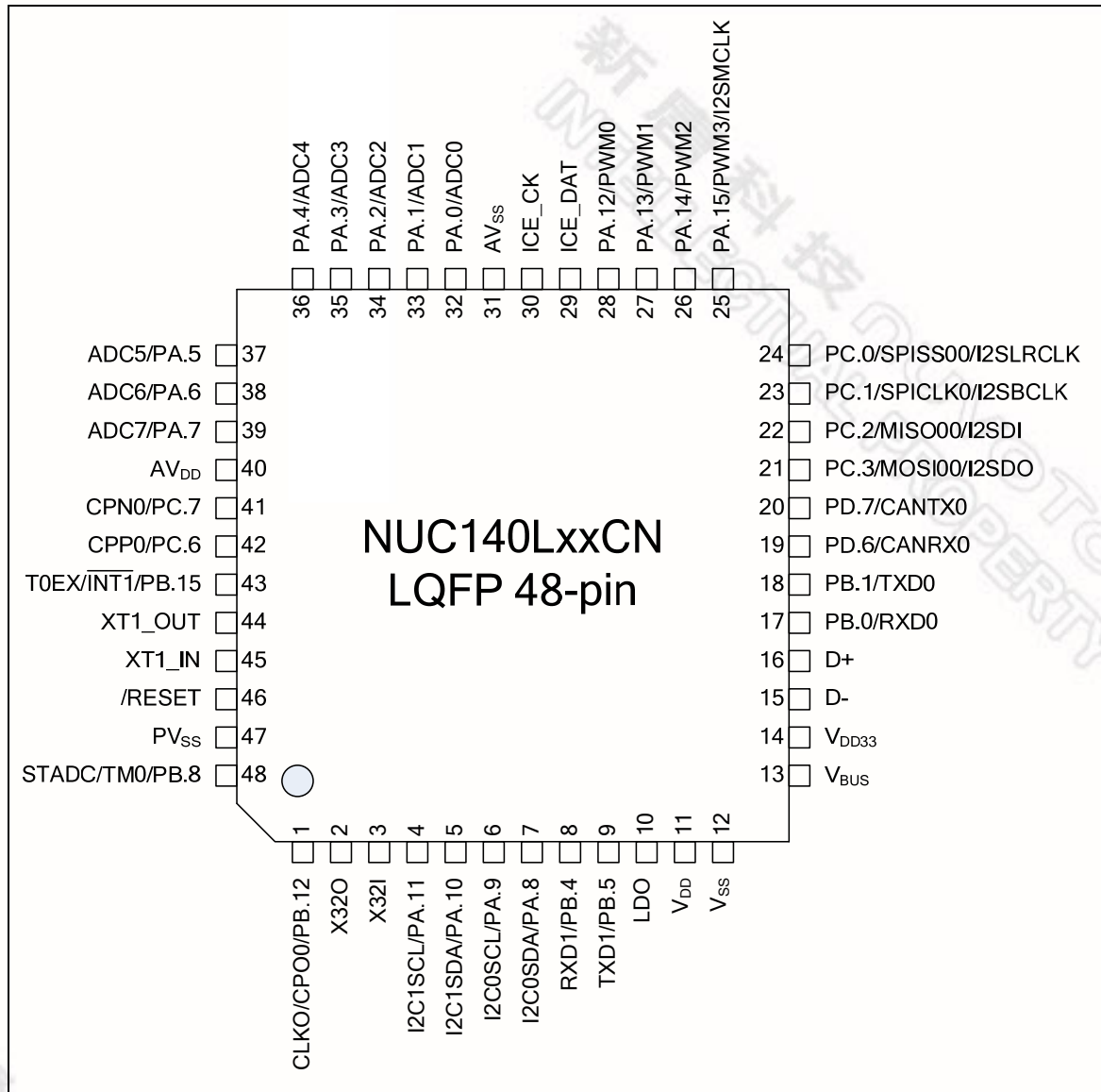


Figure 3-4 NuMicro™ NUC140 LQFP 48-pin Pin Diagram

## 4 BLOCK DIAGRAM

### 4.1 NuMicro™NUC140 Block Diagram

#### 4.1.1 NuMicro™ NUC140 Block Diagram

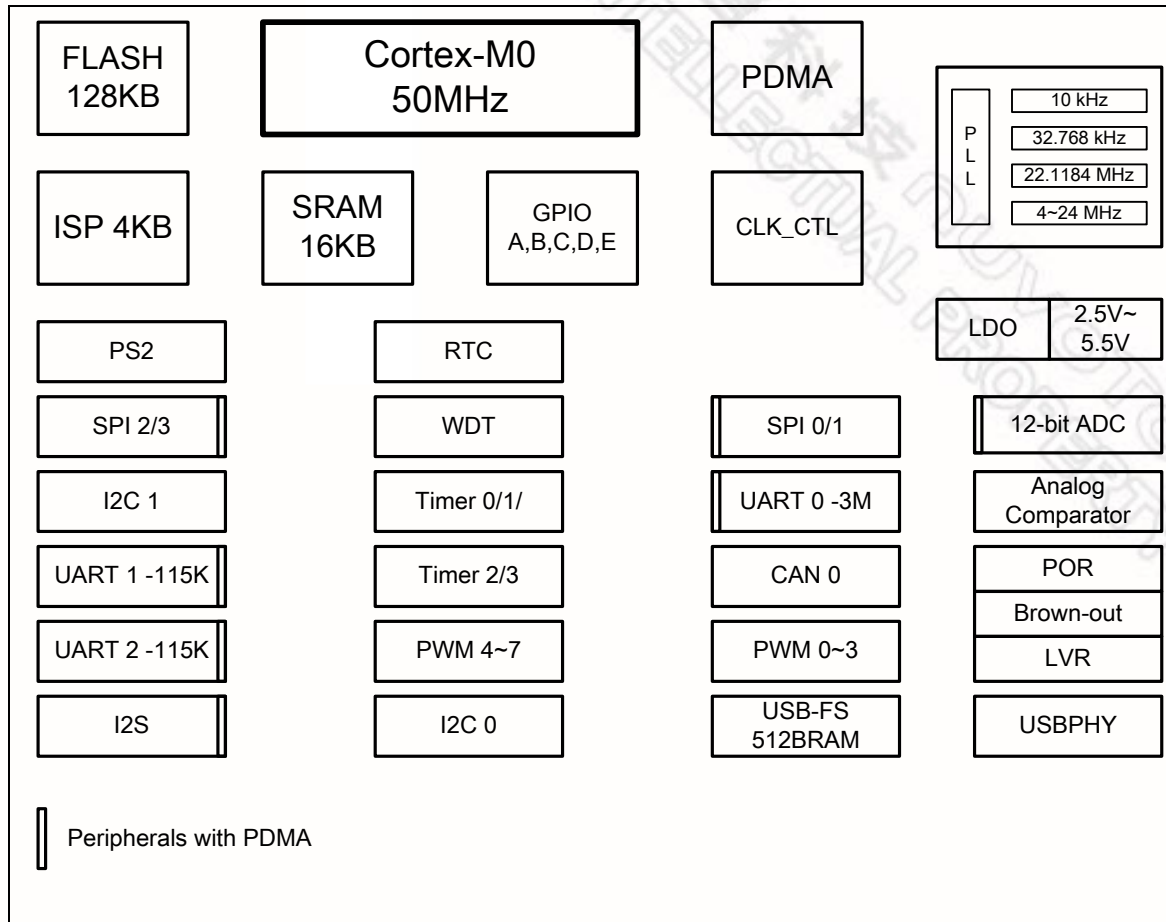


Figure 4-1 NuMicro™ NUC140 Block Diagram

- ◆ Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
  - ◆ 32 external interrupt inputs, each with four levels of priority
  - ◆ Dedicated Non-Maskable Interrupt (NMI) input.
  - ◆ Support for both level-sensitive and pulse-sensitive interrupt lines
  - ◆ Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
  - ◆ Four hardware breakpoints.
  - ◆ Two watchpoints.
  - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - ◆ Single step and vector catch capabilities.
- Bus interfaces:
  - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port).

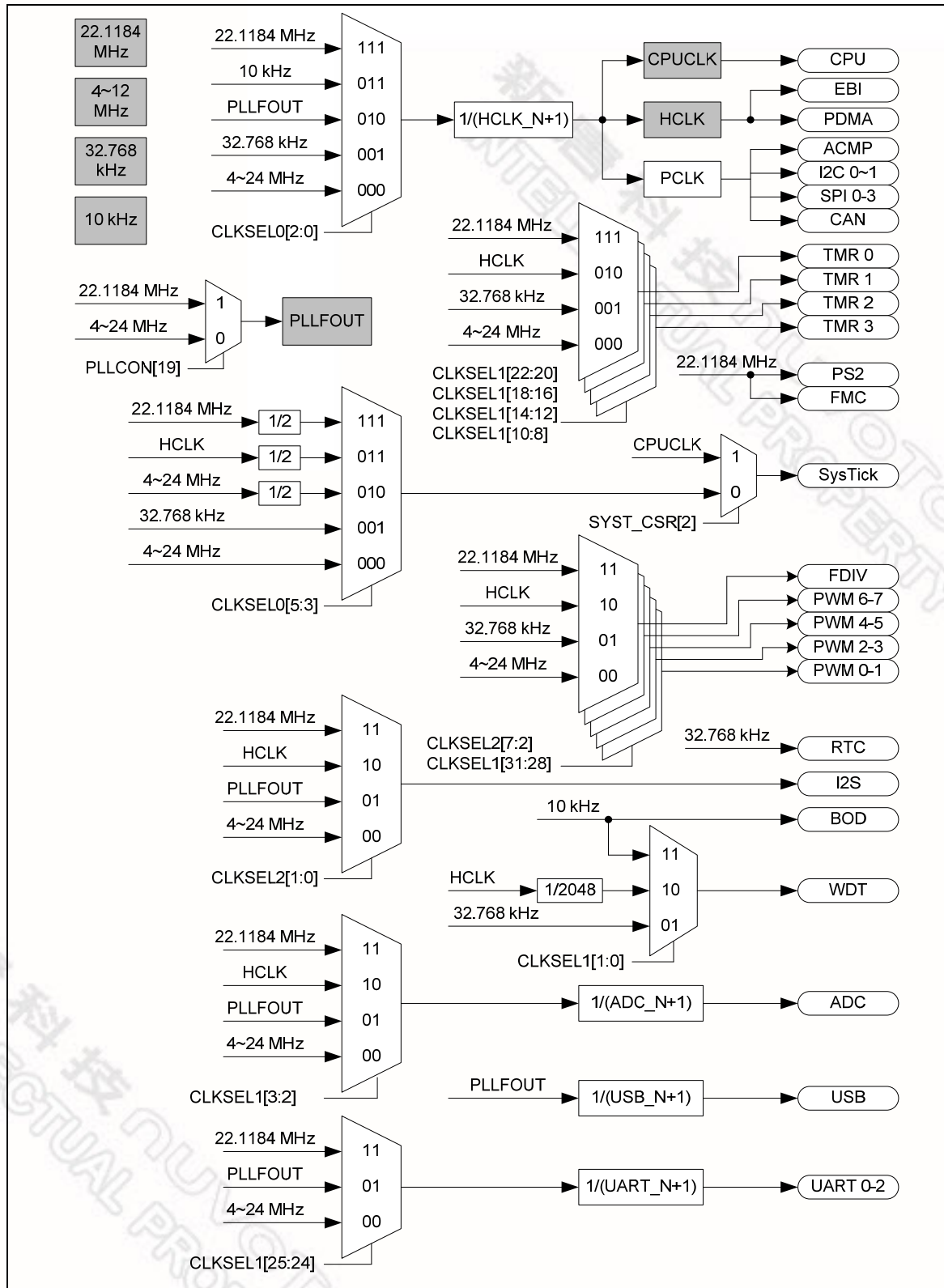


Figure 5-3 Clock generator global view diagram

## 5.6 I<sup>2</sup>C Serial Interface Controller (Master/Slave) (I<sup>2</sup>C)

### 5.6.1 Overview

I<sup>2</sup>C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I<sup>2</sup>C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 5-9 for more detail I<sup>2</sup>C BUS Timing.

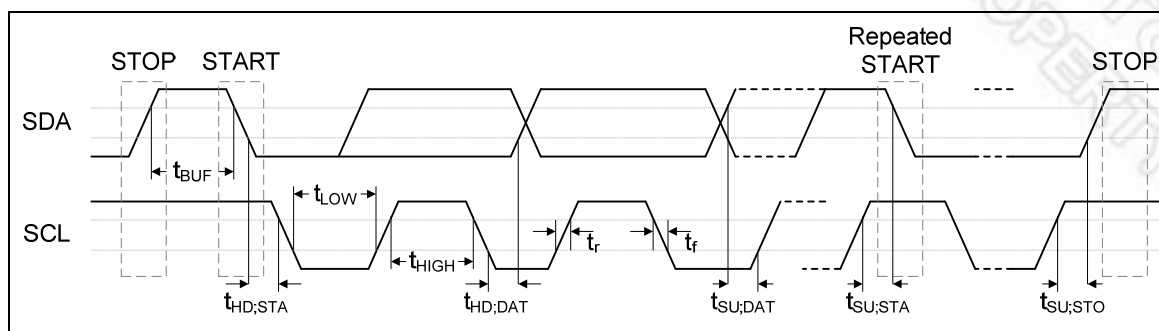


Figure 5-9 I<sup>2</sup>C Bus Timing

The device's on-chip I<sup>2</sup>C logic provides the serial interface that meets the I<sup>2</sup>C bus standard mode specification. The I<sup>2</sup>C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I<sup>2</sup>C H/W interfaces to the I<sup>2</sup>C bus via two pins: SDA and SCL. Pull up resistor is needed for I<sup>2</sup>C operation as these are open drain pins. When the I/O pins are used as I<sup>2</sup>C port, user must set the pins function to I<sup>2</sup>C in advance.

## 5.11 Watchdog Timer (WDT)

### 5.11.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wake-up chip from power down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals. Table 5-5 show the watchdog timeout interval selection and Figure 5-64 shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time ( $1024 * T_{WDT}$ ) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks ( $T_{RST}$ ) then chip restarts executing program from reset vector (0x0000\_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wake-up function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]), the chip is waken up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to wake up from power down state is  $2^4 * T_{WDT}$ . When power down command is set by software, then, chip enters power down state. After  $2^4 * T_{WDT}$  time is elapsed, chip is waken up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to wake up from power down state is  $2^{18} * T_{WDT}$ . If power down command is set by software, then, chip enters power down state. After  $2^{18} * T_{WDT}$  time is elapsed, chip is waken up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is waken up, software should clear the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over  $1024 * T_{WDT}$ , the chip is reset by Watchdog Timer.

### 5.11.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval ( $2^4 \sim 2^{18}$ ) and the time out interval is 104 ms ~ 26.3168 s (if WDT\_CLK = 10 kHz).
- Reset period =  $(1 / 10 \text{ kHz}) * 63$ , if WDT\_CLK = 10 kHz.

## 5.14 PS/2 Device Controller (PS2D)

### 5.14.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

### 5.14.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

## 5.16 Analog-to-Digital Converter (ADC)

### 5.16.1 Overview

NuMicro™ NUC100 Series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converters can be started by software and external STADC pin.

### 5.16.2 Features

- Analog input voltage range:  $0 \sim V_{REF}$
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Maximum ADC clock frequency is 16 MHz
- Up to 700K SPS conversion rate
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by
  - Software write 1 to ADST bit
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting
- Channel 7 supports 3 input sources: external analog voltage, internal bandgap voltage, and internal temperature sensor output
- Support Self-calibration to minimize conversion error

## 5.17 Analog Comparator (CMP)

### 5.17.1 Overview

NuMicro™ NUC100 Series contains two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **Error! Reference source not found.**

### 5.17.2 Features

- Analog input voltage range: 0~5.0 V
- Hysteresis function supported
- Two analog comparators with optional internal reference voltage input at negative end
- One interrupt vector for both comparators

## 5.19 External Bus Interface (EBI)

### 5.19.1 Overview

The NuMicro™ NUC130/NUC140 LQFP-64 and LQFP-100 package equips an external bus interface (EBI) for external device used.

To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

### 5.19.2 Features

External Bus Interface has the following functions:

- External devices with max. 64K-byte size (8-bit data width)/128K-byte (16-bit data width) supported
- Variable external bus base clock (MCLK) supported
- 8-bit or 16-bit data width supported
- Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

## 6 FLASH MEMORY CONTROLLER (FMC)

### 6.1 Overview

NuMicro™ NUC100 Series equips with 128/64/32K bytes on chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on, Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro™ NUC100 Series also provides additional DATA Flash for user, to store some application dependent data before chip power off. For 128K bytes APROM device, the data flash is shared with original 128K program memory and its start address is configurable and defined by user application request in Config1. For 64K/32K bytes APROM device, the data flash is fixed at 4K.

### 6.2 Features

- Run up to 50 MHz with zero wait state for continuous address read access
- 128/64/32KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Configurable or fixed 4KB data flash with 512 bytes page erase unit
- Programmable data flash start address for 128K APROM device
- In System Program (ISP) to update on chip Flash

| PARAMETER                                                                | SYM.               | SPECIFICATION       |                     |                      |      | TEST CONDITIONS                                  |
|--------------------------------------------------------------------------|--------------------|---------------------|---------------------|----------------------|------|--------------------------------------------------|
|                                                                          |                    | MIN.                | TYP.                | MAX.                 | UNIT |                                                  |
| Input High Voltage PA, PB, PC, PD, PE (Schmitt input)                    | V <sub>IH2</sub>   | 0.7 V <sub>DD</sub> | -                   | V <sub>DD</sub> +0.5 | V    |                                                  |
| Hysteresis voltage of PA~PE (Schmitt input)                              | V <sub>HY</sub>    |                     | 0.2 V <sub>DD</sub> |                      | V    |                                                  |
| Input Low Voltage XT1 <sup>[*2]</sup>                                    | V <sub>IL3</sub>   | 0                   | -                   | 0.8                  | V    | V <sub>DD</sub> = 4.5 V                          |
|                                                                          |                    | 0                   | -                   | 0.4                  |      | V <sub>DD</sub> = 3.0 V                          |
| Input High Voltage XT1 <sup>[*2]</sup>                                   | V <sub>IH3</sub>   | 3.5                 | -                   | V <sub>DD</sub> +0.2 | V    | V <sub>DD</sub> = 5.5 V                          |
|                                                                          |                    | 2.4                 | -                   | V <sub>DD</sub> +0.2 |      | V <sub>DD</sub> = 3.0 V                          |
| Input Low Voltage X32I <sup>[*2]</sup>                                   | V <sub>IL4</sub>   | 0                   | -                   | 0.4                  | v    |                                                  |
| Input High Voltage X32I <sup>[*2]</sup>                                  | V <sub>IH4</sub>   | 1.7                 |                     | 2.5                  | V    |                                                  |
| Negative going threshold (Schmitt input), /RESET                         | V <sub>ILS</sub>   | -0.5                | -                   | 0.3 V <sub>DD</sub>  | V    |                                                  |
| Positive going threshold (Schmitt input), /RESET                         | V <sub>IHS</sub>   | 0.7 V <sub>DD</sub> | -                   | V <sub>DD</sub> +0.5 | V    |                                                  |
| Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)             | I <sub>SR11</sub>  | -300                | -370                | -450                 | μA   | V <sub>DD</sub> = 4.5 V, V <sub>S</sub> = 2.4 V  |
|                                                                          | I <sub>SR12</sub>  | -50                 | -70                 | -90                  | μA   | V <sub>DD</sub> = 2.7 V, V <sub>S</sub> = 2.2 V  |
|                                                                          | I <sub>SR13</sub>  | -40                 | -60                 | -80                  | μA   | V <sub>DD</sub> = 2.5 V, V <sub>S</sub> = 2.0 V  |
| Source Current PA, PB, PC, PD, PE (Push-pull Mode)                       | I <sub>SR21</sub>  | -20                 | -24                 | -28                  | mA   | V <sub>DD</sub> = 4.5 V, V <sub>S</sub> = 2.4 V  |
|                                                                          | I <sub>SR22</sub>  | -4                  | -6                  | -8                   | mA   | V <sub>DD</sub> = 2.7 V, V <sub>S</sub> = 2.2 V  |
|                                                                          | I <sub>SR23</sub>  | -3                  | -5                  | -7                   | mA   | V <sub>DD</sub> = 2.5 V, V <sub>S</sub> = 2.0 V  |
| Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode) | I <sub>SK11</sub>  | 10                  | 16                  | 20                   | mA   | V <sub>DD</sub> = 4.5 V, V <sub>S</sub> = 0.45 V |
|                                                                          | I <sub>SK12</sub>  | 7                   | 10                  | 13                   | mA   | V <sub>DD</sub> = 2.7 V, V <sub>S</sub> = 0.45 V |
|                                                                          | I <sub>SK13</sub>  | 6                   | 9                   | 12                   | mA   | V <sub>DD</sub> = 2.5 V, V <sub>S</sub> = 0.45 V |
| Brown-Out voltage with BOV_VL [1:0] = 00b                                | V <sub>BO2.2</sub> | 2.1                 | 2.2                 | 2.3                  | V    |                                                  |
| Brown-Out voltage with BOV_VL [1:0] = 01b                                | V <sub>BO2.7</sub> | 2.6                 | 2.7                 | 2.8                  | V    |                                                  |
| Brown-Out voltage with BOV_VL [1:0] = 10b                                | V <sub>BO3.8</sub> | 3.6                 | 3.8                 | 4.0                  | V    |                                                  |
| Brown-Out voltage with BOV_VL [1:0] = 11b                                | V <sub>BO4.5</sub> | 4.3                 | 4.5                 | 4.7                  | V    |                                                  |
| Hysteresis range of BOD voltage                                          | V <sub>BH</sub>    | 30                  | -                   | 150                  | mV   | V <sub>DD</sub> = 2.5 V~5.5 V                    |

## 7.4 Analog Characteristics

### 7.4.1 Specification of 12-bit SARADC

| SYMBOL    | PARAMETER                               | MIN.       | TYP.      | MAX.      | UNIT  |
|-----------|-----------------------------------------|------------|-----------|-----------|-------|
| -         | Resolution                              | -          | -         | 12        | Bit   |
| DNL       | Differential nonlinearity error         | -          | ±3        | -         | LSB   |
| INL       | Integral nonlinearity error             | -          | ±4        | -         | LSB   |
| EO        | Offset error                            | -          | ±1        | 10        | LSB   |
| EG        | Gain error (Transfer gain)              | -          | 1         | 1.005     | -     |
| -         | Monotonic                               | Guaranteed |           |           |       |
| FADC      | ADC clock frequency ( $AV_{DD}=5V/3V$ ) | -          | -         | 16/8      | MHz   |
| FS        | Sample rate                             | -          | -         | 700       | K SPS |
| $V_{DDA}$ | Supply voltage                          | 3          | -         | 5.5       | V     |
| $I_{DD}$  | Supply current (Avg.)                   | -          | 0.5       | -         | mA    |
| $I_{DDA}$ |                                         | -          | 1.5       | -         | mA    |
| $V_{REF}$ | Reference voltage                       | -          | $V_{DDA}$ | -         | V     |
| $I_{REF}$ | Reference current (Avg.)                | -          | 1         | -         | mA    |
| $V_{IN}$  | Input voltage                           | 0          | -         | $V_{REF}$ | V     |

## 7.5 Flash DC Electrical Characteristics

| SYMBOL             | PARAMETER             | CONDITIONS | MIN.  | TYP. | MAX. | UNIT                  |
|--------------------|-----------------------|------------|-------|------|------|-----------------------|
| N <sub>endu</sub>  | Endurance             |            | 10000 |      |      | cycles <sup>[1]</sup> |
| T <sub>ret</sub>   | Retention time        | Temp=25 °C | 100   |      |      | year                  |
| T <sub>erase</sub> | Page erase time       |            | 20    |      | 40   | ms                    |
| T <sub>mass</sub>  | Mass erase time       |            | 40    | 50   | 60   | ms                    |
| T <sub>prog</sub>  | Program time          |            | 35    | 40   | 55   | us                    |
| V <sub>dd</sub>    | Supply voltage        |            | 2.25  | 2.5  | 2.75 | V <sup>[2]</sup>      |
| I <sub>dd1</sub>   | Read current          |            |       |      | 14   | mA                    |
| I <sub>dd2</sub>   | Program/Erase current |            |       |      | 7    | mA                    |
| I <sub>pd</sub>    | Power down current    |            |       |      | 10   | uA                    |

1. Number of program/erase cycles.
2. V<sub>dd</sub> is source from chip LDO output voltage.
3. This table is guaranteed by design, not test in production.

## 7.6 SPI Dynamic Characteristics

| SYMBOL                                                                | PARAMETER              | MIN.               | TYP.                | MAX.                | UNIT |
|-----------------------------------------------------------------------|------------------------|--------------------|---------------------|---------------------|------|
| SPI master mode ( $V_{DD} = 4.5V \sim 5.5V$ , 30pF loading Capacitor) |                        |                    |                     |                     |      |
| $t_{DS}$                                                              | Data setup time        | 4                  | 2                   | -                   | ns   |
| $t_{DH}$                                                              | Data hold time         | 0                  | -                   | -                   | ns   |
| $t_V$                                                                 | Data output valid time | -                  | 7                   | 11                  | ns   |
| SPI master mode ( $V_{DD} = 3.0V \sim 3.6V$ , 30pF loading Capacitor) |                        |                    |                     |                     |      |
| $t_{DS}$                                                              | Data setup time        | 5                  | 3                   | -                   | ns   |
| $t_{DH}$                                                              | Data hold time         | 0                  | -                   | -                   | ns   |
| $t_V$                                                                 | Data output valid time | -                  | 13                  | 18                  | ns   |
| SPI slave mode ( $V_{DD} = 4.5V \sim 5.5V$ , 30pF loading Capacitor)  |                        |                    |                     |                     |      |
| $t_{DS}$                                                              | Data setup time        | 0                  | -                   | -                   | ns   |
| $t_{DH}$                                                              | Data hold time         | $2 \cdot PCLK + 4$ | -                   | -                   | ns   |
| $t_V$                                                                 | Data output valid time | -                  | $2 \cdot PCLK + 11$ | $2 \cdot PCLK + 19$ | ns   |
| SPI slave mode ( $V_{DD} = 3.0V \sim 3.6V$ , 30pF loading Capacitor)  |                        |                    |                     |                     |      |
| $t_{DS}$                                                              | Data setup time        | 0                  | -                   | -                   | ns   |
| $t_{DH}$                                                              | Data hold time         | $2 \cdot PCLK + 6$ | -                   | -                   | ns   |
| $t_V$                                                                 | Data output valid time | -                  | $2 \cdot PCLK + 19$ | $2 \cdot PCLK + 25$ | ns   |