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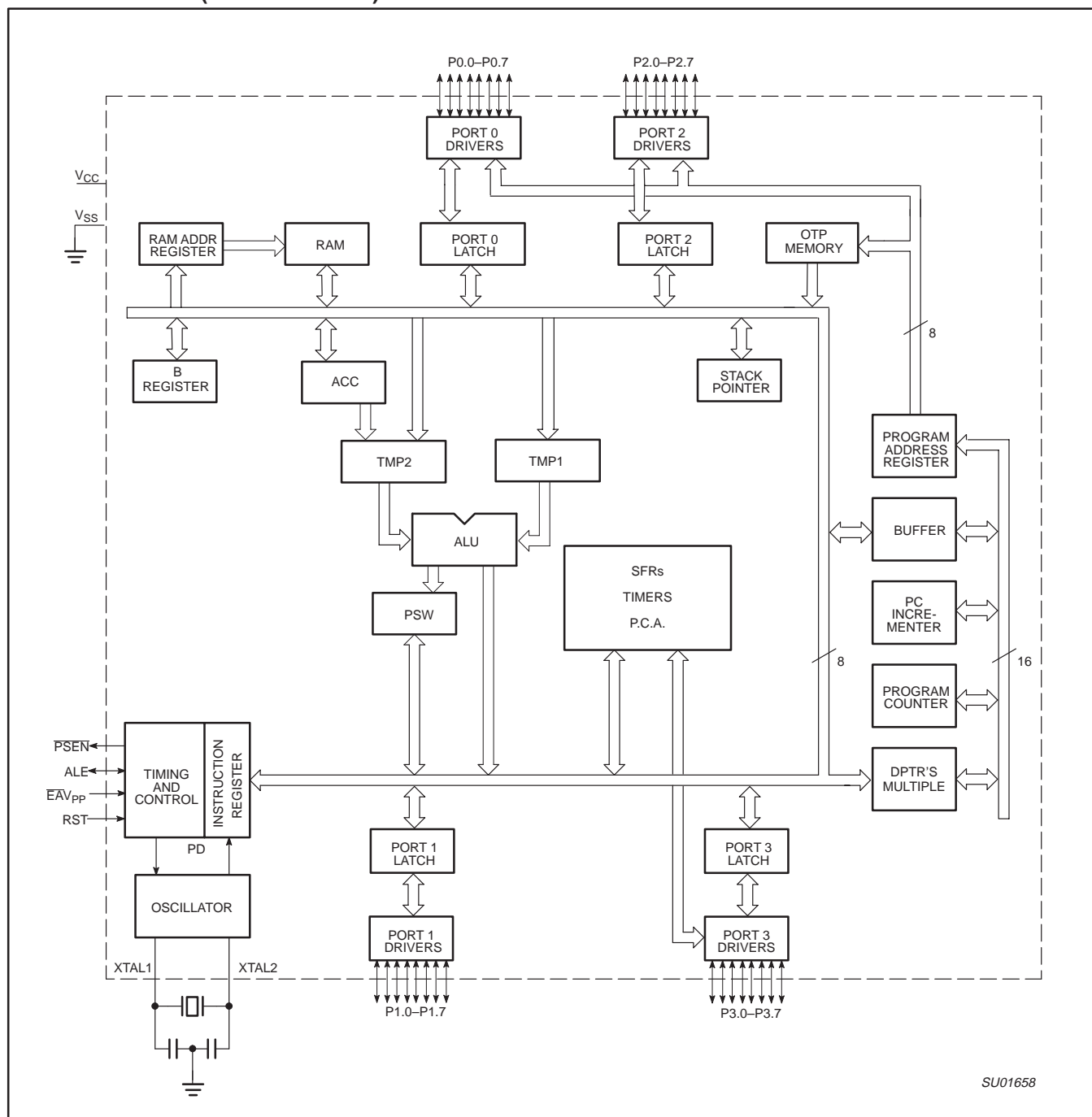
Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51ra2ba-512

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

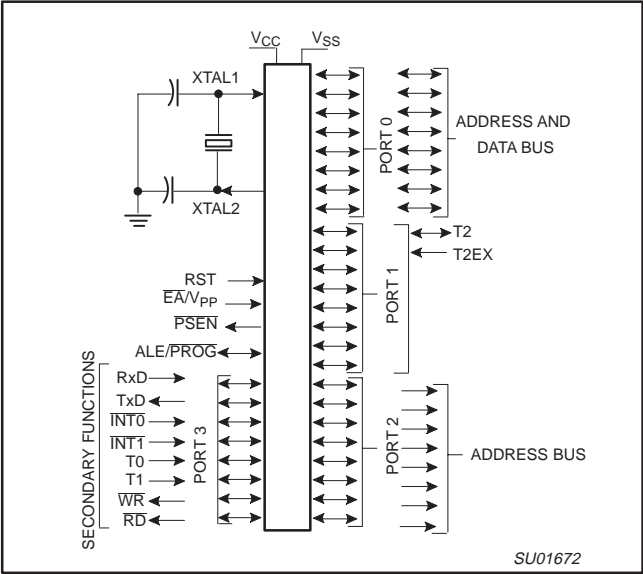
BLOCK DIAGRAM (CPU-ORIENTED)



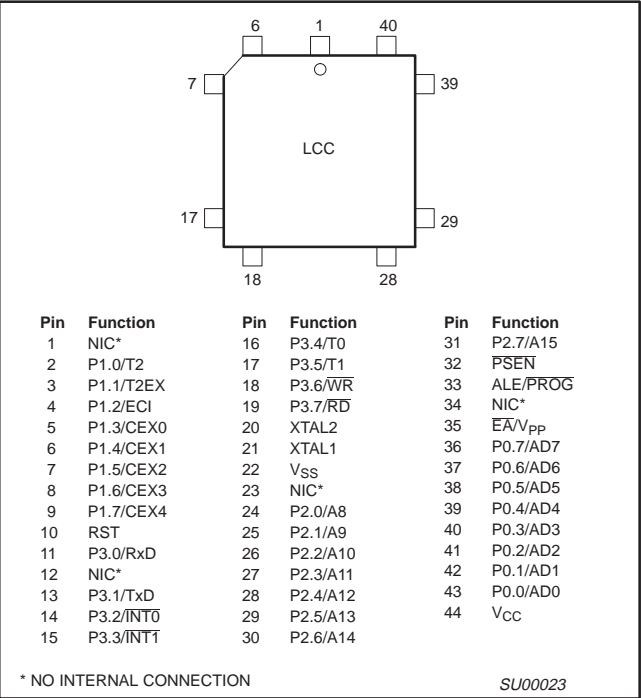
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LOGIC SYMBOL

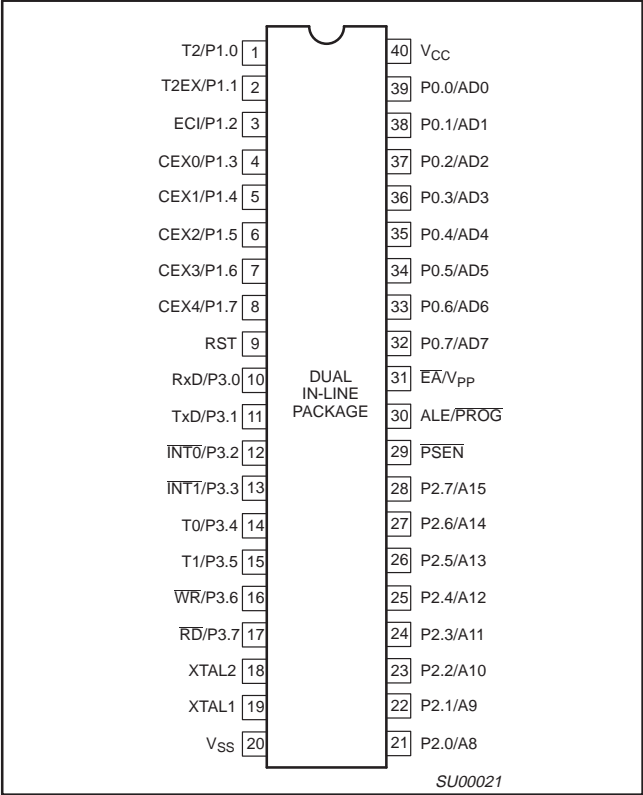


Plastic Leaded Chip Carrier

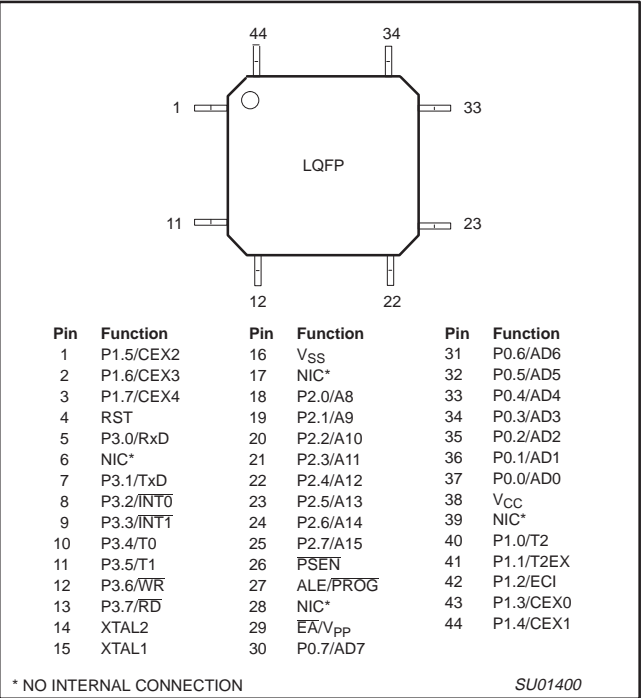


PINNING

Plastic Dual In-Line Package



Plastic Quad Flat Pack



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LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

POWER-ON FLAG

The Power-On Flag (POF) is set by on-chip circuitry when the V_{CC} level on the P87C51RA2/RB2/RC2/RD2 rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3 V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and \overline{PSEN} is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and \overline{PSEN} are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency in 12-clock mode (122 Hz to 8 MHz in 6-clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$n \times \frac{\text{Oscillator Frequency}}{(65536 - \text{RCAP2H, RCAP2L})}$$

n = 2 in 6-clock mode
4 in 12-clock mode

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	\overline{PSEN}	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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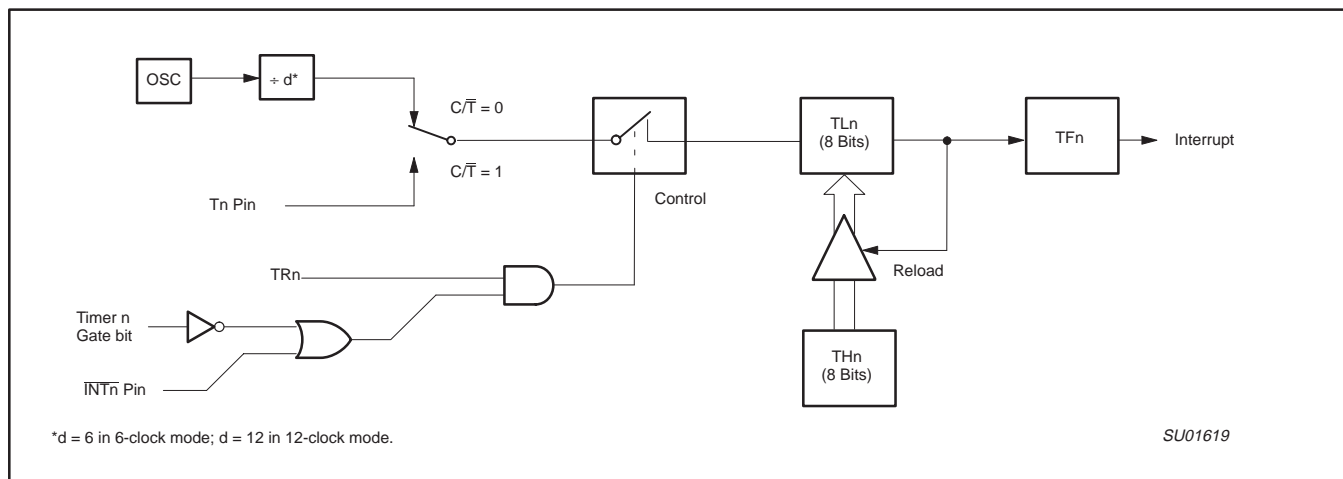


Figure 5. Timer/Counter 0/1 Mode 2: 8-Bit Auto-Reload

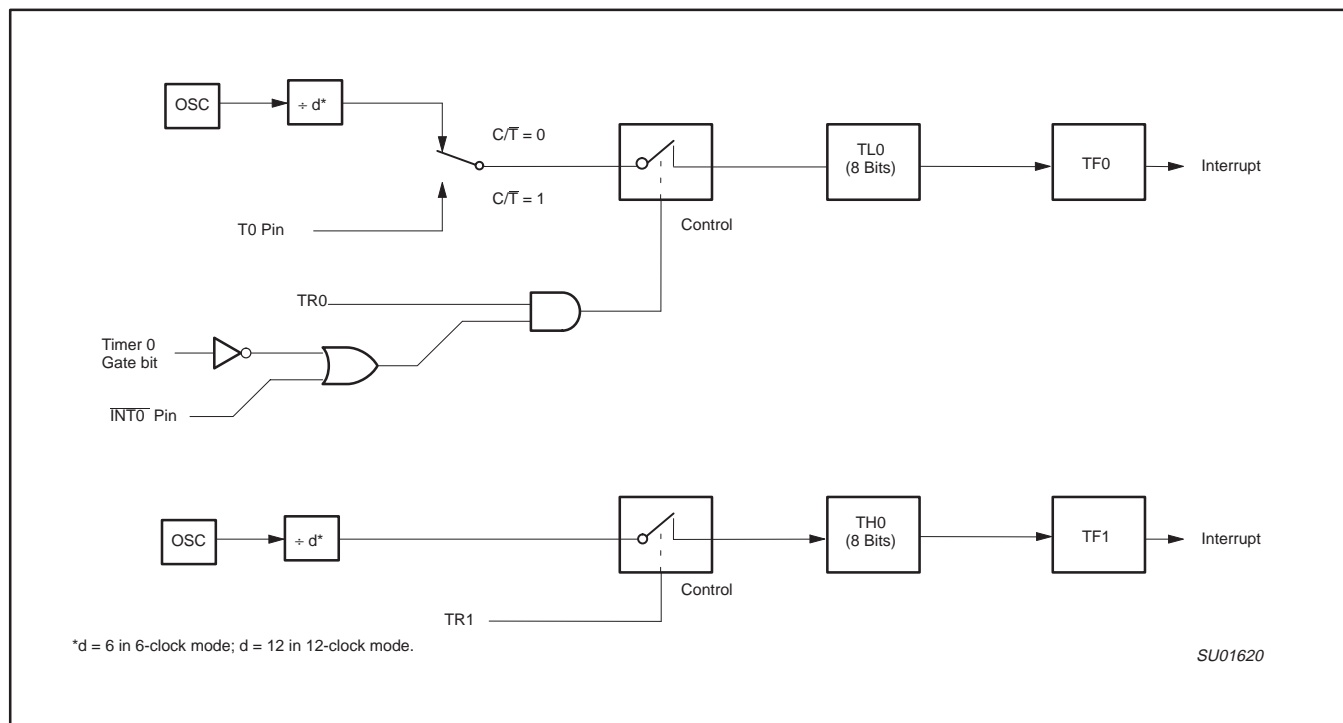


Figure 6. Timer/Counter 0 Mode 3: Two 8-Bit Counters

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TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2 in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2 in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/6 pulses (osc/12 in 12-clock mode)).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter [C/T2 in T2CON]) then programmed to count up or down. The counting direction is determined by bit DCEN (Down

Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

		(MSB)						(LSB)	
		TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Symbol	Position	Name and Significance							
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.							
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).							
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.							
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.							
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.							
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.							
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/6 in 6-clock mode or OSC/12 in 12-clock mode) 1 = External event counter (falling edge triggered).							
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.							

SU01251

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Figure 1. Timer/Counter 2 (T2CON) Control Register

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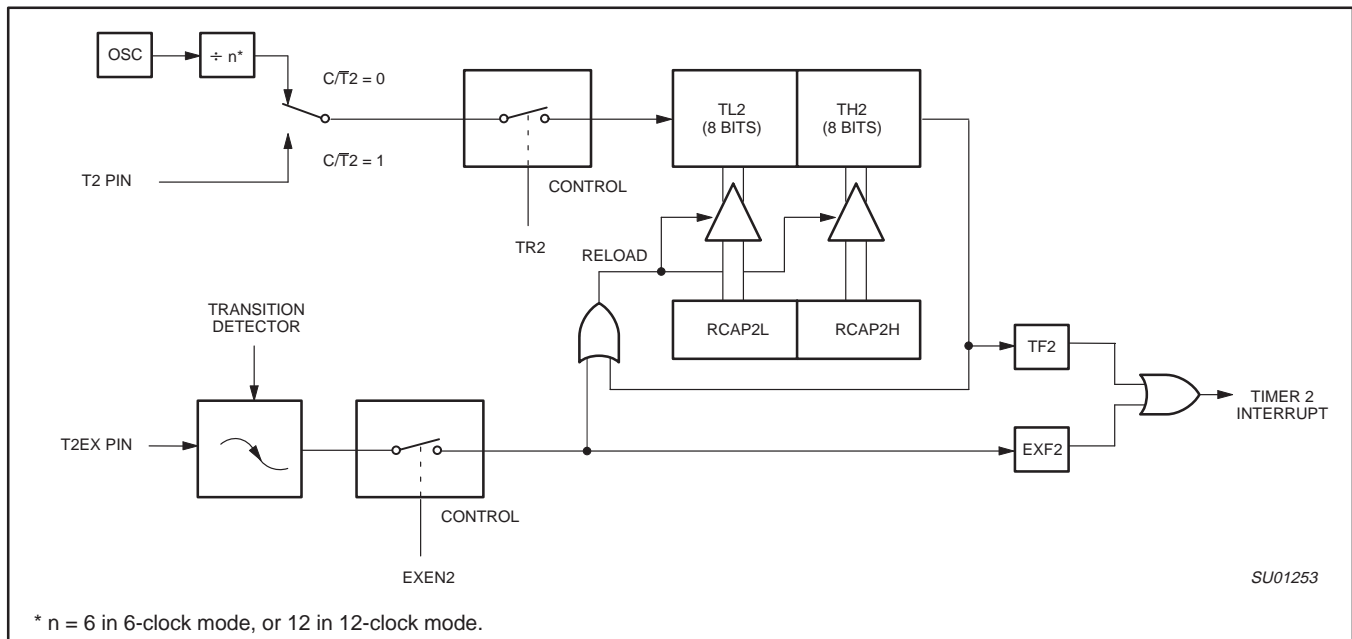


Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)

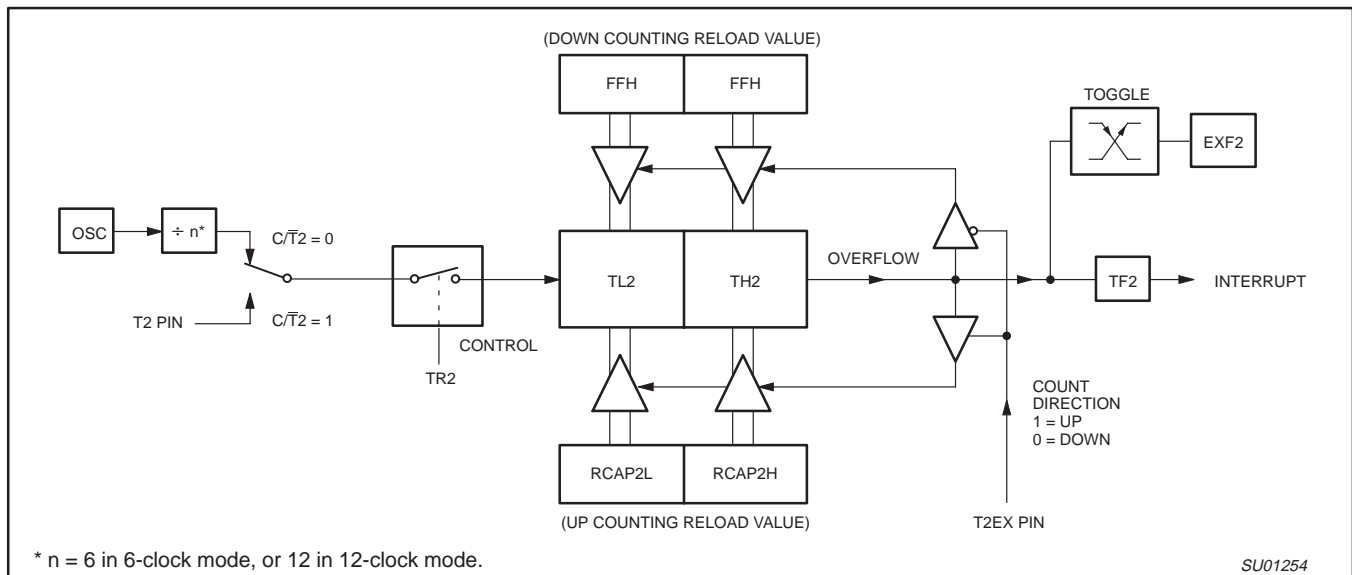


Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)

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shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 80C51 the baud rate is determined by the Timer 1 or Timer 2 overflow rate.

Figure 10 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.:

1. RI = 0, and
2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time,

whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

More About Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 (12-clock mode) or 1/16 or 1/32 the oscillator frequency (6-clock mode) the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1 or Timer 2.

Figures 11 and 12 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R-D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1. RI = 0, and
2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

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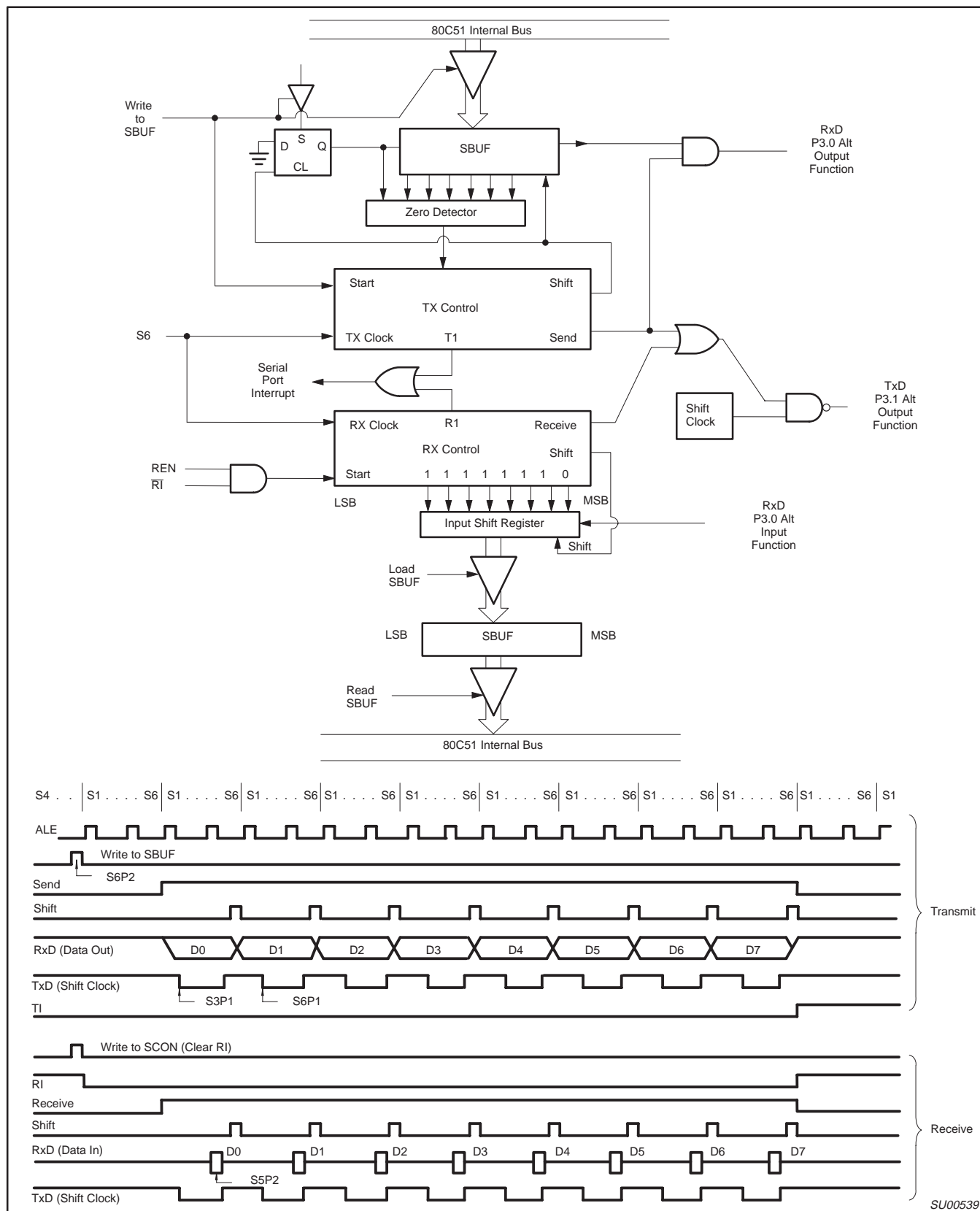


Figure 9. Serial Port Mode 0

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Enhanced Features

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 13.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 14.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1101
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	1111 1110
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1001
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	1111 1010
	Given =	1110 0XX0
Slave 2	SADDR =	1110 0000
	SADEN =	1111 1100
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

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		7	6	5	4	3	2	1	0
IP (0B8H)		–	PPC	PT2	PS	PT1	PX1	PT0	PX0
		Priority Bit = 1 assigns high priority Priority Bit = 0 assigns low priority							
BIT	SYMBOL	FUNCTION							
IP.7	–	–							
IP.6	PPC	PCA interrupt priority bit							
IP.5	PT2	Timer 2 interrupt priority bit.							
IP.4	PS	Serial Port interrupt priority bit.							
IP.3	PT1	Timer 1 interrupt priority bit.							
IP.2	PX1	External interrupt 1 priority bit.							
IP.1	PT0	Timer 0 interrupt priority bit.							
IP.0	PX0	External interrupt 0 priority bit.							

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Figure 16. IP Registers

		7	6	5	4	3	2	1	0
IPH (B7H)		–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Priority Bit = 1 assigns higher priority Priority Bit = 0 assigns lower priority							
BIT	SYMBOL	FUNCTION							
IPH.7	–	–							
IPH.6	PPCH	PCA interrupt priority bit							
IPH.5	PT2H	Timer 2 interrupt priority bit high.							
IPH.4	PSH	Serial Port interrupt priority bit high.							
IPH.3	PT1H	Timer 1 interrupt priority bit high.							
IPH.2	PX1H	External interrupt 1 priority bit high.							
IPH.1	PT0H	Timer 0 interrupt priority bit high.							
IPH.0	PX0H	External interrupt 0 priority bit high.							

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Figure 17. IPH Registers

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speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

Programmable Counter Array (PCA)

The Programmable Counter Array available on the P87C51RA2/RB2/RC2/RD2 is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1.4 (CEX1), etc. The basic PCA configuration is shown in Figure 19.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 22):

CPS1 CPS0 PCA Timer Count Source

0	0	1/6 oscillator frequency (6-clock mode); 1/12 oscillator frequency (12-clock mode)
0	1	1/2 oscillator frequency (6-clock mode); 1/4 oscillator frequency (12-clock mode)
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 20.

The watchdog timer function is implemented in module 4 (see Figure 29).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 23). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when

the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 21.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 24). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 25 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

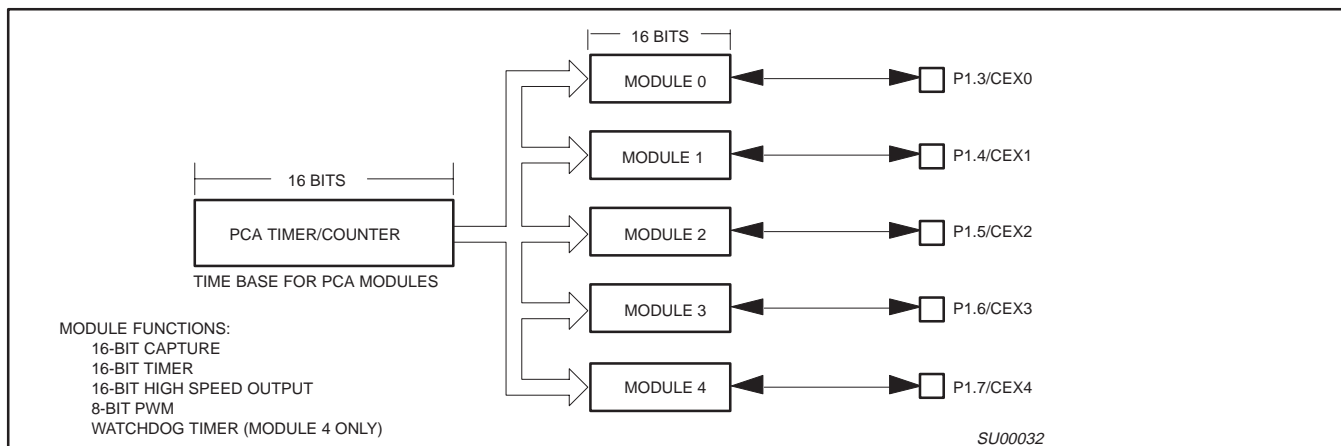


Figure 19. Programmable Counter Array (PCA)

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speed (30/33 MHz)

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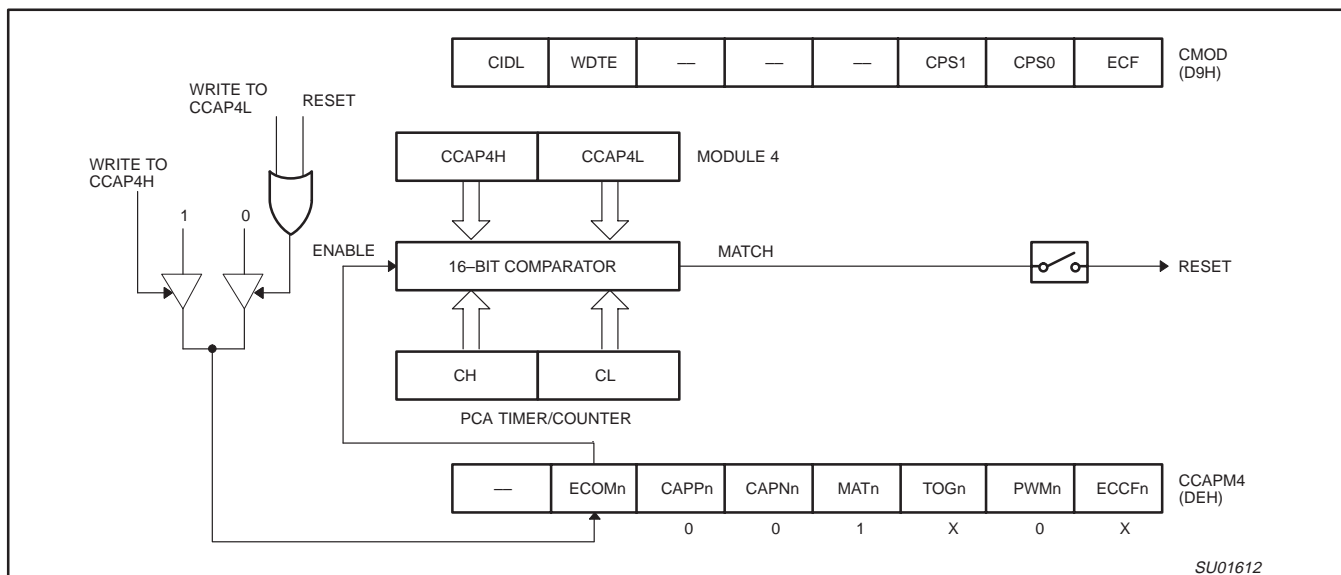


Figure 30. PCA Watchdog Timer mode (Module 4 only)

PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 30 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 31 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine in Figure 31.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

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P87C51RA2/RB2/RC2/RD2

Expanded Data RAM Addressing

The P87C51RA2/RB2/RC2/RD2 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes expanded RAM (ERAM) (768 bytes for the RD2).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256/768-bytes expanded RAM (ERAM, 00H – 1FFH/2FFH) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared, see Figure 32.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

```
MOV 0A0H,#data
```

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 bytes of data RAM.

For example:

```
MOV @R0,acc
```

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The ERAM can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 256/768 bytes of external data memory in the P87C51RA2/RB2/RC2/RD2.

With EXTRAM = 0, the ERAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ERAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is output during external addressing. For example, with EXTRAM = 0,

```
MOVX @R0,acc
```

where R0 contains 0A0H, accesses the ERAM at address 0A0H rather than external memory. An access to external data memory locations higher than the ERAM will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 33.

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high-order eight address bits (the contents of DPH) while Port 0 multiplexes the low-order eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 (WR) and P3.7 (RD).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the ERAM.

AUXR Address = 8EH		Reset Value = xxxx xx00B							
Not Bit Addressable									
		—	—	—	—	—	—	EXTRAM	AO
Bit:		7	6	5	4	3	2	1	0
Symbol	Function								
AO	Disable/Enable ALE								
	AO								
	0	ALE is emitted at a constant rate of $\frac{1}{6}$ the oscillator frequency (12-clock mode; $\frac{1}{3} f_{OSC}$ in 6-clock mode).							
	1	ALE is active only during off-chip memory access.							
EXTRAM	Internal/External RAM access using MOVX @Ri/@DPTR								
	EXTRAM								
	0	Internal ERAM access using MOVX @Ri/@DPTR							
	1	External data memory access.							
—	Not implemented, reserved for future use*.								
NOTE:									
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.									

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Figure 32. AUXR: Auxiliary Register

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P87C51RA2/RB2/RC2/RD2

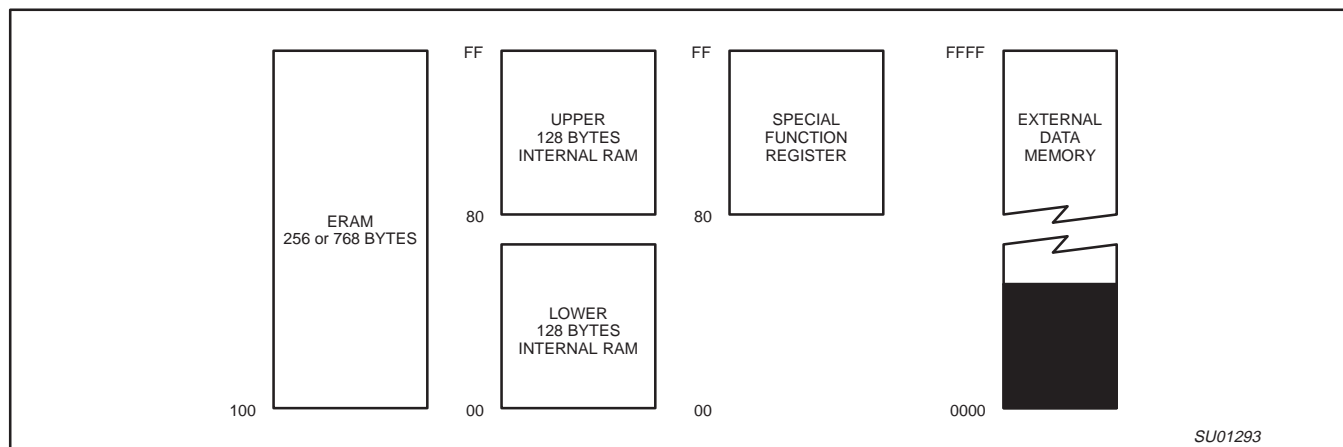


Figure 33. Internal and External Data Memory Address Space with EXTRAM = 0

HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT FOR P87C51RA2/RB2/RC2/RD2)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, the user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When the WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When the WDT overflows, it will drive an output reset HIGH pulse at the RST-pin (see the note below).

Using the WDT

To enable the WDT, the user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When the WDT overflows, it will generate an output RESET pulse at the reset pin (see note below). The RESET pulse duration is $98 \times T_{OSC}$ (6-clock mode; 196 in 12-clock mode), where $T_{OSC} = 1/f_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

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with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C or }-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$ (30/33 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage ¹¹	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, EA)		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ¹¹		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{ V}$; $I_{OL} = 1.6\text{ mA}^2$	-		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{7, 8}	$V_{CC} = 4.5\text{ V}$; $I_{OL} = 3.2\text{ mA}^2$	-		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{ V}$; $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		-	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 4.5\text{ V}$; $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		-	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$; See note 4	-		-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	-		± 10	μA
I_{CC}	Power supply current Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 46 for conditions)	$T_{amb} = 0\text{ }^{\circ}\text{C to }70\text{ }^{\circ}\text{C}$		2	30	μA
		$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$		3	50	μA
V_{RAM}	RAM keep-alive voltage		1.2			V
R_{RST}	Internal reset pull-down resistor		40		225	$\text{k}\Omega$
C_{IO}	Pin capacitance ¹⁰ (except EA)		-		15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 43 through 46 for I_{CC} test conditions and Figure 41 for I_{CC} vs. Frequency.
12-clock mode characteristics:
Active mode (operating): $I_{CC} = 1.0\text{ mA} + 1.1\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Active mode (reset): $I_{CC} = 7.0\text{ mA} + 0.6\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Idle mode: $I_{CC} = 1.0\text{ mA} + 0.22\text{ mA} \times \text{FREQ.}[\text{MHz}]$
- This value applies to $T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$. For $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$, $I_{TL} = -750\text{ }\mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 °C specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except EA is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.

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AC ELECTRICAL CHARACTERISTICS (12-CLOCK MODE, 5 V $\pm 10\%$ OPERATION)

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}^{1,2,3,4}$

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	38	Oscillator frequency	0	33			MHz
t_{LHLL}	34	ALE pulse width	$2 t_{CLCL} - 8$		117		ns
t_{AVLL}	34	Address valid to ALE low	$t_{CLCL} - 13$		49.5		ns
t_{LLAX}	34	Address hold after ALE low	$t_{CLCL} - 20$		42.5		ns
t_{LLIV}	34	ALE low to valid instruction in		$4 t_{CLCL} - 35$		215	ns
t_{LLPL}	34	ALE low to PSEN low	$t_{CLCL} - 10$		52.5		ns
t_{PLPH}	34	PSEN pulse width	$3 t_{CLCL} - 10$		177.5		ns
t_{PLIV}	34	PSEN low to valid instruction in		$3 t_{CLCL} - 35$		152.5	ns
t_{PXIX}	34	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	34	Input instruction float after PSEN		$t_{CLCL} - 10$		52.5	ns
t_{AVIV}	34	Address to valid instruction in		$5 t_{CLCL} - 35$		277.5	ns
t_{PLAZ}	34	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	35	\overline{RD} pulse width	$6 t_{CLCL} - 20$		355		ns
t_{WLWH}	36	\overline{WR} pulse width	$6 t_{CLCL} - 20$		355		ns
t_{RLDV}	35	\overline{RD} low to valid data in		$5 t_{CLCL} - 35$		277.5	ns
t_{RHDX}	35	Data hold after \overline{RD}	0		0		ns
t_{RHDZ}	35	Data float after \overline{RD}		$2 t_{CLCL} - 10$		115	ns
t_{LLDV}	35	ALE low to valid data in		$8 t_{CLCL} - 35$		465	ns
t_{AVDV}	35	Address to valid data in		$9 t_{CLCL} - 35$		527.5	ns
t_{LLWL}	35, 36	ALE low to \overline{RD} or \overline{WR} low	$3 t_{CLCL} - 15$	$3 t_{CLCL} + 15$	172.5	202.5	ns
t_{AVWL}	35, 36	Address valid to \overline{WR} low or \overline{RD} low	$4 t_{CLCL} - 15$		235		ns
t_{QVWX}	36	Data valid to \overline{WR} transition	$t_{CLCL} - 25$		37.5		ns
t_{WHQX}	36	Data hold after \overline{WR}	$t_{CLCL} - 15$		47.5		ns
t_{QVWH}	36	Data valid to \overline{WR} high	$7 t_{CLCL} - 5$		432.5		ns
t_{RLAZ}	35	\overline{RD} low to address float		0		0	ns
t_{WHLH}	35, 36	\overline{RD} or \overline{WR} high to ALE high	$t_{CLCL} - 10$	$t_{CLCL} + 10$	52.5	72.5	ns
External Clock							
t_{CHCX}	38	High time	$0.32 t_{CLCL}$	$t_{CLCL} - t_{CLCX}$			ns
t_{CLCX}	38	Low time	$0.32 t_{CLCL}$	$t_{CLCL} - t_{CHCX}$			ns
t_{CLCH}	38	Rise time		5			ns
t_{CHCL}	38	Fall time		5			ns
Shift register							
t_{XLXL}	37	Serial port clock cycle time	$12 t_{CLCL}$		750		ns
t_{QVXH}	37	Output data setup to clock rising edge	$10 t_{CLCL} - 25$		600		ns
t_{XHQX}	37	Output data hold after clock rising edge	$2 t_{CLCL} - 15$		110		ns
t_{XHDX}	37	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	37	Clock rising edge to input data valid ⁵		$10 t_{CLCL} - 133$		492	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all outputs = 80 pF
- Interfacing the microcontroller to devices with float time up to 45 ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
- Parts are guaranteed by design to operate down to 0 Hz.
- Below 16 MHz this parameter is $8 t_{CLCL} - 133$.

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AC ELECTRICAL CHARACTERISTICS (6-CLOCK MODE, 5 V $\pm 10\%$ OPERATION)

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ ^{1,2,3,4,5}

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	38	Oscillator frequency	0	30			MHz
t_{LHLL}	34	ALE pulse width	$t_{CLCL} - 8$		54.5		ns
t_{AVLL}	34	Address valid to ALE low	$0.5 t_{CLCL} - 13$		18.25		ns
t_{LLAX}	34	Address hold after ALE low	$0.5 t_{CLCL} - 20$		11.25		ns
t_{LLIV}	34	ALE low to valid instruction in		$2 t_{CLCL} - 35$		90	ns
t_{LLPL}	34	ALE low to PSEN low	$0.5 t_{CLCL} - 10$		21.25		ns
t_{PLPH}	34	PSEN pulse width	$1.5 t_{CLCL} - 10$		83.75		ns
t_{PLIV}	34	PSEN low to valid instruction in		$1.5 t_{CLCL} - 35$		58.75	ns
t_{PXIX}	34	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	34	Input instruction float after PSEN		$0.5 t_{CLCL} - 10$		21.25	ns
t_{AVIV}	34	Address to valid instruction in		$2.5 t_{CLCL} - 35$		121.25	ns
t_{PLAZ}	34	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	35	RD pulse width	$3 t_{CLCL} - 20$		167.5		ns
t_{WLWH}	36	WR pulse width	$3 t_{CLCL} - 20$		167.5		ns
t_{RLDV}	35	RD low to valid data in		$2.5 t_{CLCL} - 35$		121.25	ns
t_{RHDX}	35	Data hold after RD	0		0		ns
t_{RHDZ}	35	Data float after RD		$t_{CLCL} - 10$		52.5	ns
t_{LLDV}	35	ALE low to valid data in		$4 t_{CLCL} - 35$		215	ns
t_{AVDV}	35	Address to valid data in		$4.5 t_{CLCL} - 35$		246.25	ns
t_{LLWL}	35, 36	ALE low to RD or WR low	$1.5 t_{CLCL} - 15$	$1.5 t_{CLCL} + 15$	78.75	108.75	ns
t_{AVWL}	35, 36	Address valid to WR low or RD low	$2 t_{CLCL} - 15$		110		ns
t_{QVWX}	36	Data valid to WR transition	$0.5 t_{CLCL} - 25$		6.25		ns
t_{WHQX}	36	Data hold after WR	$0.5 t_{CLCL} - 15$		16.25		ns
t_{QVWH}	36	Data valid to WR high	$3.5 t_{CLCL} - 5$		213.75		ns
t_{RLAZ}	35	RD low to address float		0		0	ns
t_{WHLH}	35, 36	RD or WR high to ALE high	$0.5 t_{CLCL} - 10$	$0.5 t_{CLCL} + 10$	21.25	41.25	ns
External Clock							
t_{CHCX}	38	High time	$0.4 t_{CLCL}$	$t_{CLCL} - t_{CLCX}$			ns
t_{CLCX}	38	Low time	$0.4 t_{CLCL}$	$t_{CLCL} - t_{CHCX}$			ns
t_{CLCH}	38	Rise time		5			ns
t_{CHCL}	38	Fall time		5			ns
Shift register							
t_{XLXL}	37	Serial port clock cycle time	$6 t_{CLCL}$		375		ns
t_{QVXH}	37	Output data setup to clock rising edge	$5 t_{CLCL} - 25$		287.5		ns
t_{XHGX}	37	Output data hold after clock rising edge	$t_{CLCL} - 15$		47.5		ns
t_{XHDX}	37	Input data hold after clock rising edge	0		0		ns
t_{XHDX}	37	Clock rising edge to input data valid ⁶		$5 t_{CLCL} - 133$		179.5	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN=100 pF, load capacitance for all outputs = 80 pF
- Interfacing the microcontroller to devices with float time up to 45ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
- Parts are guaranteed by design to operate down to 0 Hz.
- Data shown in the table are the best mathematical models for the set of measured values obtained in tests. If a particular parameter calculated at a customer specified frequency has a negative value, it should be considered equal to zero.
- Below 16 MHz this parameter is $4 t_{CLCL} - 133$

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

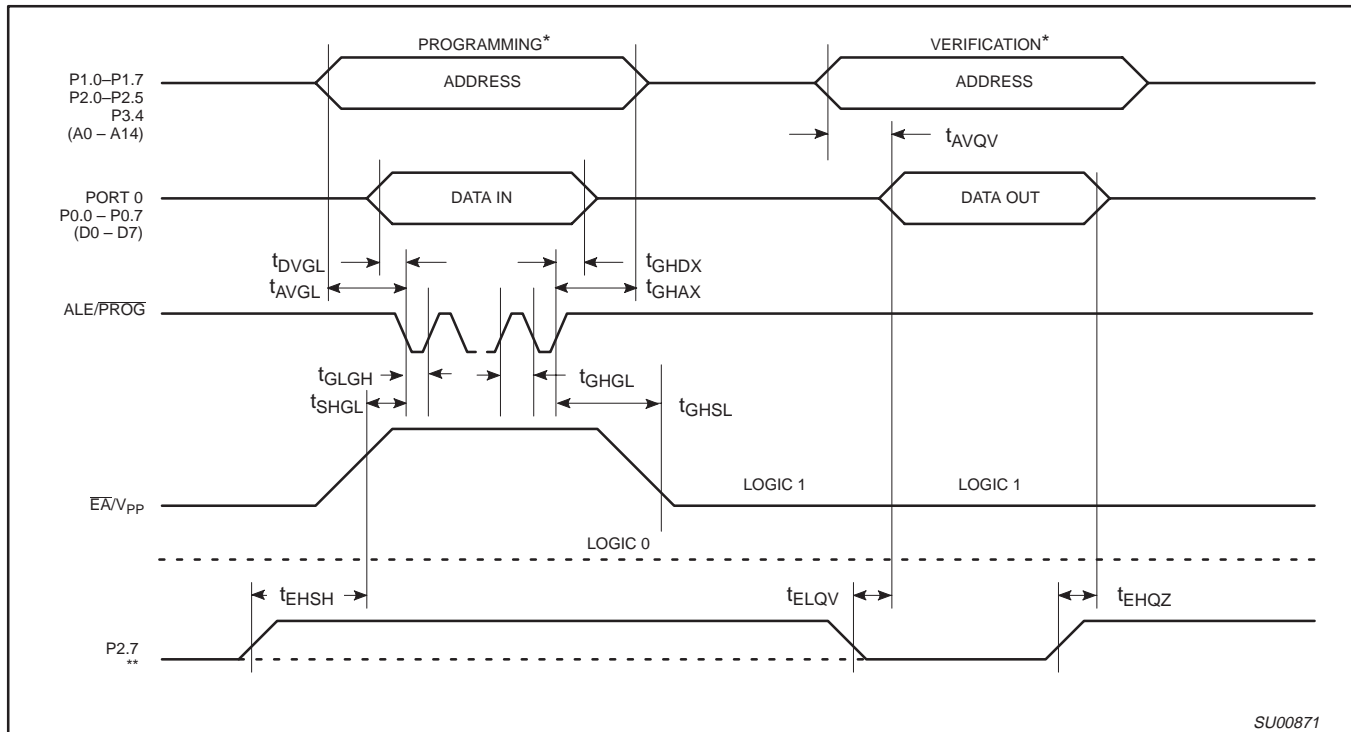
EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$ to $+27^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$ (See Figure 50)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50 ¹	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to \overline{PROG} low	$48t_{CLCL}$		
t_{GHAX}	Address hold after \overline{PROG}	$48t_{CLCL}$		
t_{DVGL}	Data setup to \overline{PROG} low	$48t_{CLCL}$		
t_{GHDX}	Data hold after \overline{PROG}	$48t_{CLCL}$		
t_{EHS}	P2.7 (\overline{ENABLE}) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to \overline{PROG} low	10		μs
t_{GHS}	V_{PP} hold after \overline{PROG}	10		μs
t_{GLGH}	\overline{PROG} width	90	110	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	\overline{ENABLE} low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after \overline{ENABLE}	0	$48t_{CLCL}$	
t_{GHGL}	\overline{PROG} high to \overline{PROG} low	10		μs

NOTE:

1. Not tested.



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NOTES:

* FOR PROGRAMMING CONFIGURATION SEE FIGURE 47.
FOR VERIFICATION CONDITIONS SEE FIGURE 49.

** SEE TABLE 8.

Figure 50. EPROM Programming and Verification

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

ROM CODE SUBMISSION FOR 32K ROM DEVICES (87C51RC2)

When submitting ROM code for the 32K ROM devices, the following must be specified:

1. 32 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 7FFFH	DATA	7:0	User ROM Data
8000H to 803FH	KEY	7:0	ROM Encryption Key FFH = no encryption
8040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
8040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOV_C is disabled, and
2. \overline{EA} is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

REVISION HISTORY

Rev	Date	Description
_3	20030124	Product data (9397 750 10994); ECN 853-2391 29335 dated 07 Jan 2003. Modifications: <ul style="list-style-type: none">• Updated ordering information table.
_2	20021028	Product data (9397 750 10393); ECN 853-2391 29117 dated 28 Oct 2002.