



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

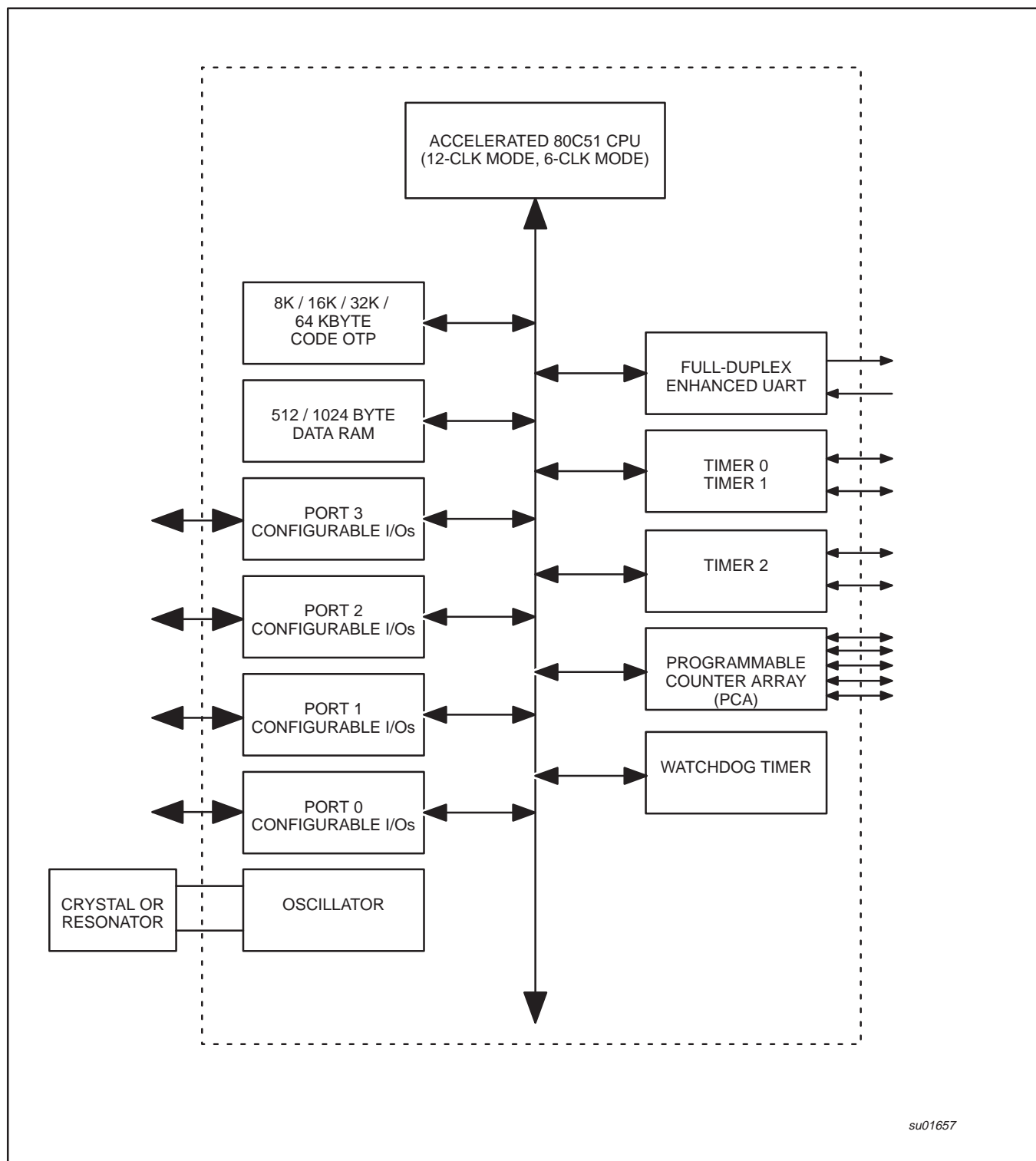
Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51rc2bn-112

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

BLOCK DIAGRAM 1



80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

POWER-ON FLAG

The Power-On Flag (POF) is set by on-chip circuitry when the V_{CC} level on the P87C51RA2/RB2/RC2/RD2 rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3 V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and \overline{PSEN} is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and \overline{PSEN} are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency in 12-clock mode (122 Hz to 8 MHz in 6-clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$n \times \frac{\text{Oscillator Frequency}}{(65536 - \text{RCAP2H, RCAP2L})}$$

n = 2 in 6-clock mode
4 in 12-clock mode

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	\overline{PSEN}	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

TIMER 0 AND TIMER 1 OPERATION

Timer 0 and Timer 1

The "Timer" or "Counter" function is selected by control bits C/\overline{T} in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 3 shows the Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF_n. The counted input is enabled to the Timer when TR_n = 1 and either GATE = 0 or \overline{INTn} = 1. (Setting GATE = 1 allows the Timer to be controlled by external input \overline{INTn} , to facilitate pulse width measurements). TR_n is a control bit in the Special Function Register TCON (Figure 4).

The 13-bit register consists of all 8 bits of TH_n and the lower 5 bits of TL_n. The upper 3 bits of TL_n are indeterminate and should be ignored. Setting the run flag (TR_n) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL_n) with automatic reload, as shown in Figure 5. Overflow from TL_n not only sets TF_n, but also reloads TL_n with the contents of TH_n, which is preset by software. The reload leaves TH_n unchanged.

Mode 2 operation is the same for Timer 0 as for Timer 1.

Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 6. TL0 uses the Timer 0 control bits: C/\overline{T} , GATE, TR0, and TF0 as well as pin $\overline{INT0}$. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. With Timer 0 in Mode 3, an 80C51 can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

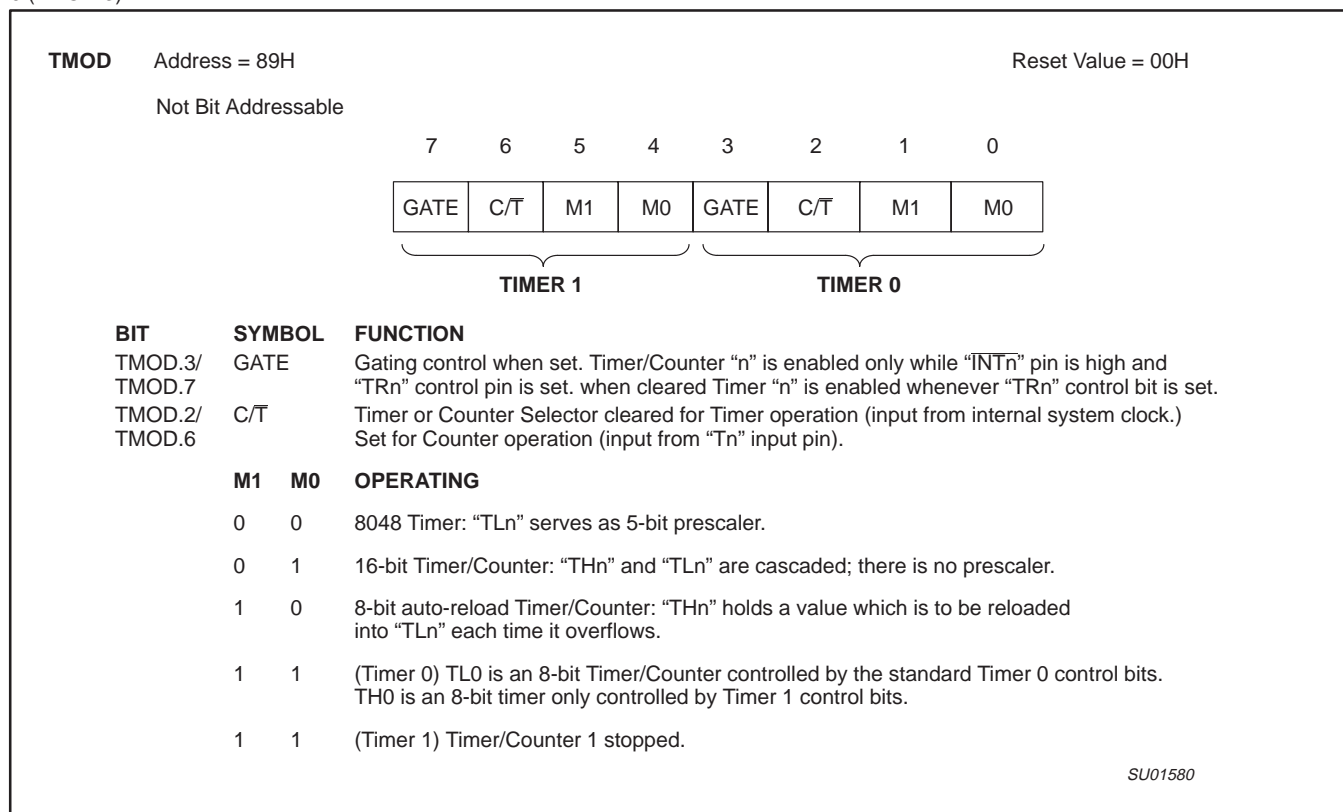


Figure 2. Timer/Counter 0/1 Mode Control (TMOD) Register

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2 in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2 in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/6 pulses (osc/12 in 12-clock mode)).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter [C/T2 in T2CON]) then programmed to count up or down. The counting direction is determined by bit DCEN (Down

Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

		(MSB)							(LSB)	
			TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/6 in 6-clock mode or OSC/12 in 12-clock mode) 1 = External event counter (falling edge triggered).
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

SU01251

SU01251

Figure 1. Timer/Counter 2 (T2CON) Control Register

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time ($f_{osc}/2$) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Summary of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{osc}}{[n * \times [65536 - (RCAP2H, RCAP2L)]]}$$

* n = 16 in 6-clock mode
 32 in 12-clock mode

Where f_{osc} = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$RCAP2H, RCAP2L = 65536 - \left(\frac{f_{osc}}{n * \times \text{Baud Rate}} \right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 80C51 the baud rate is determined by the Timer 1 or Timer 2 overflow rate.

Figure 10 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.:

1. RI = 0, and
2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time,

whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

More About Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 (12-clock mode) or 1/16 or 1/32 the oscillator frequency (6-clock mode) the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1 or Timer 2.

Figures 11 and 12 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R-D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

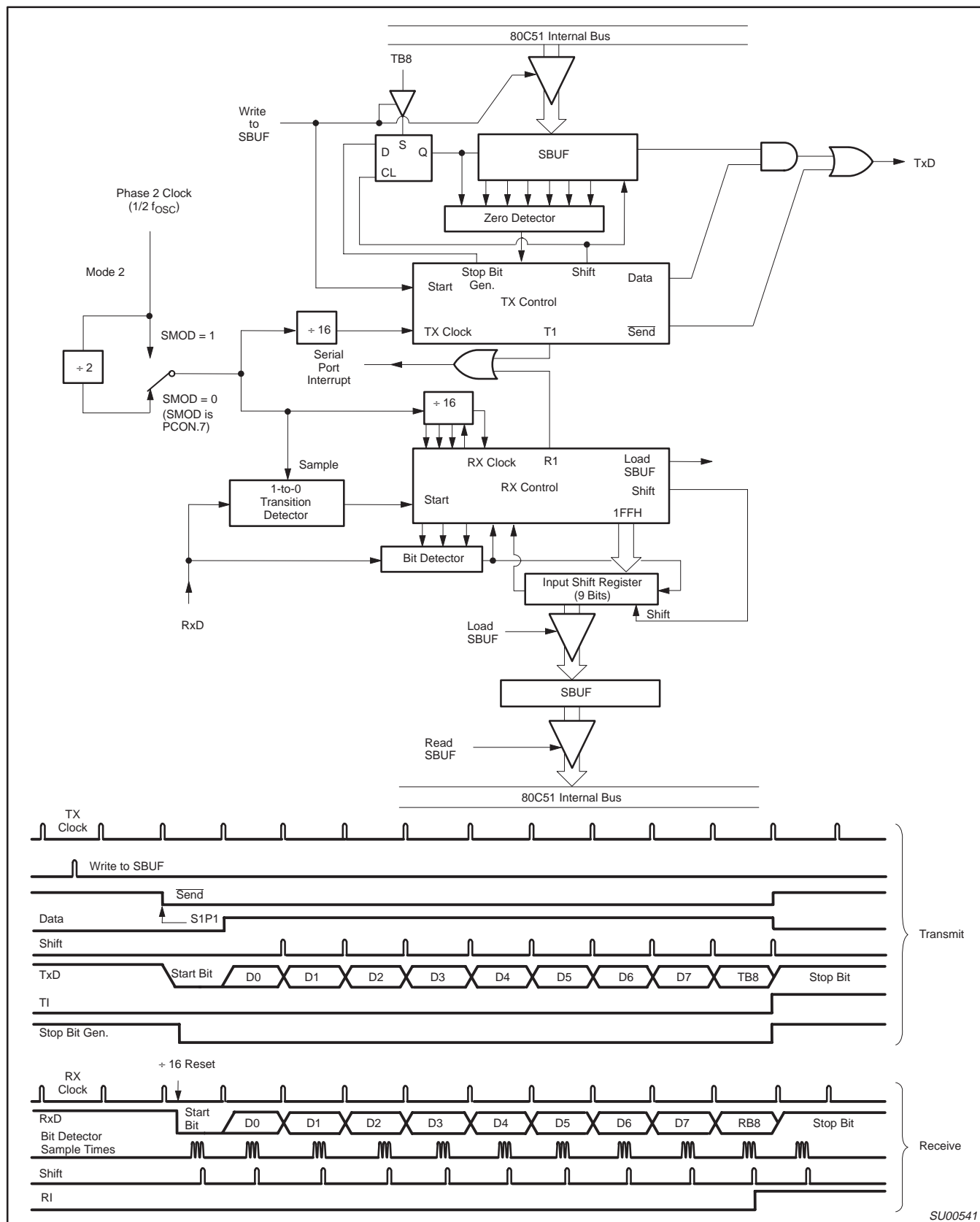
The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1. RI = 0, and
2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2



SU00541

Figure 11. Serial Port Mode 2

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

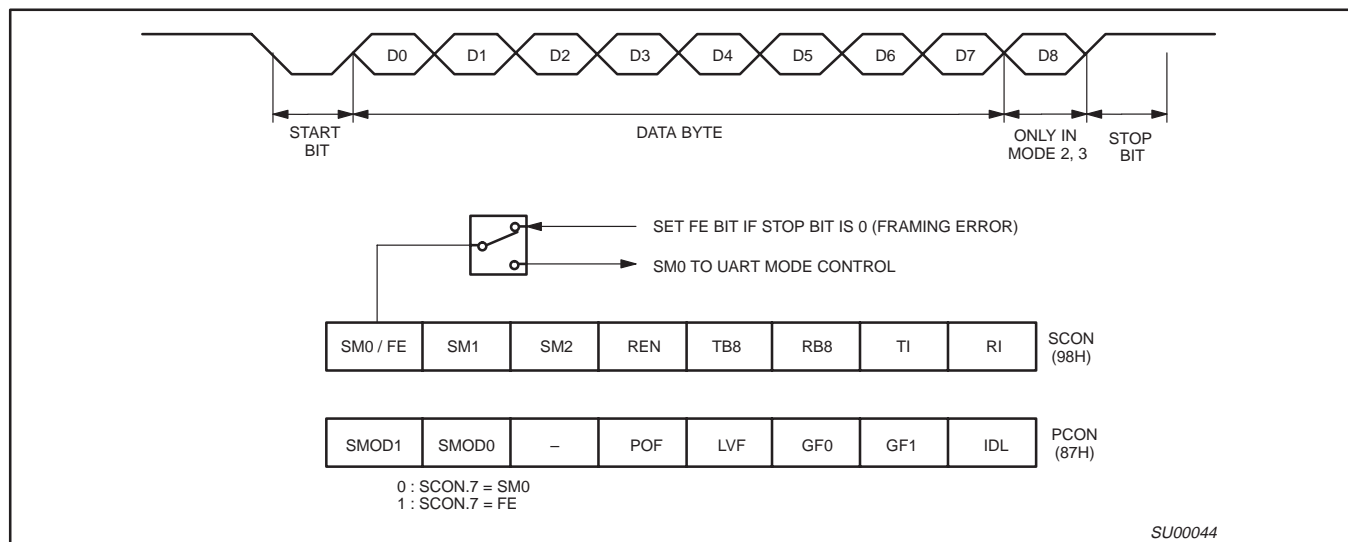


Figure 13. UART Framing Error Detection

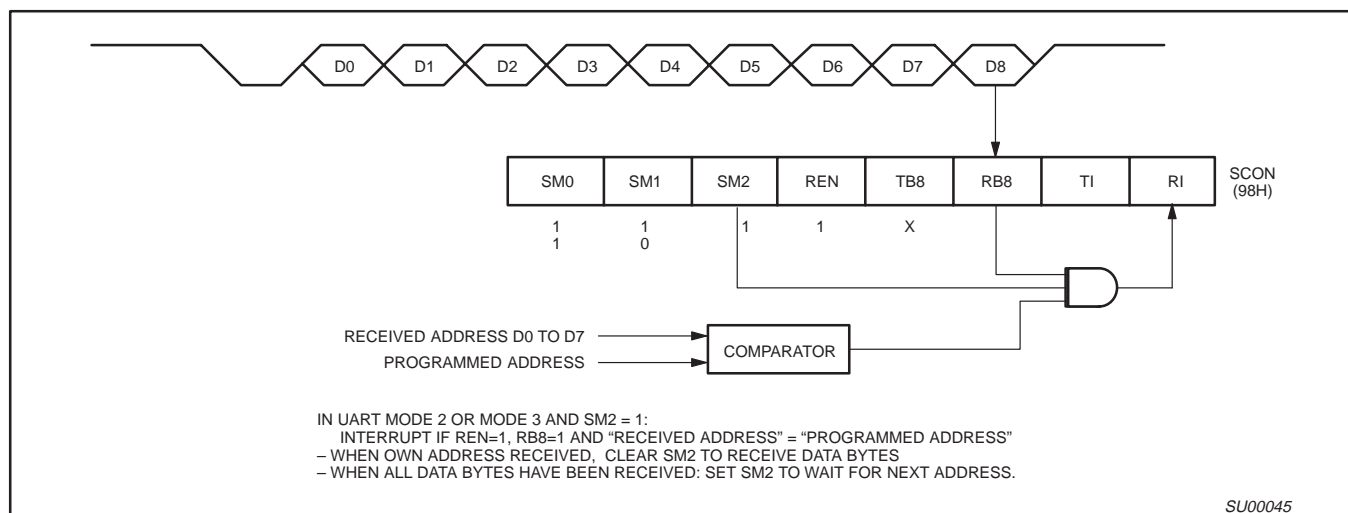


Figure 14. UART Multiprocessor Communication, Automatic Address Recognition

P87C51RA2/RB2/RC2/RD2



80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

CMOD Address = D9H					Reset Value = 00XX X000B			
	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF
Bit:	7	6	5	4	3	2	1	0
Symbol	Function							
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.							
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.							
–	Not implemented, reserved for future use.*							
CPS1	PCA Count Pulse Select bit 1.							
CPS0	PCA Count Pulse Select bit 0.							
	CPS1	CPS0	Selected PCA Input**					
	0	0	0	Internal clock, $f_{OSC}/6$ in 6-clock mode ($f_{OSC}/12$ in 12-clock mode)				
	0	1	1	Internal clock, $f_{OSC}/2$ in 6-clock mode ($f_{OSC}/4$ in 12-clock mode)				
	1	0	2	Timer 0 overflow				
	1	1	3	External clock at ECI/P1.2 pin (max. rate = $f_{OSC}/4$ in 6-clock mode, $f_{OSC}/8$ in 12-clock mode)				
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.							
NOTE:								
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.								
** f_{OSC} = oscillator frequency								

SU01318

SU01318

Figure 22. CMOD: PCA Counter Mode Register

CCON Address = D8H

Reset Value = 00X0 0000B

Bit Addressable

CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0

Bit:

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU01319

SU01319

Figure 23. CCON: PCA Counter Control Register

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

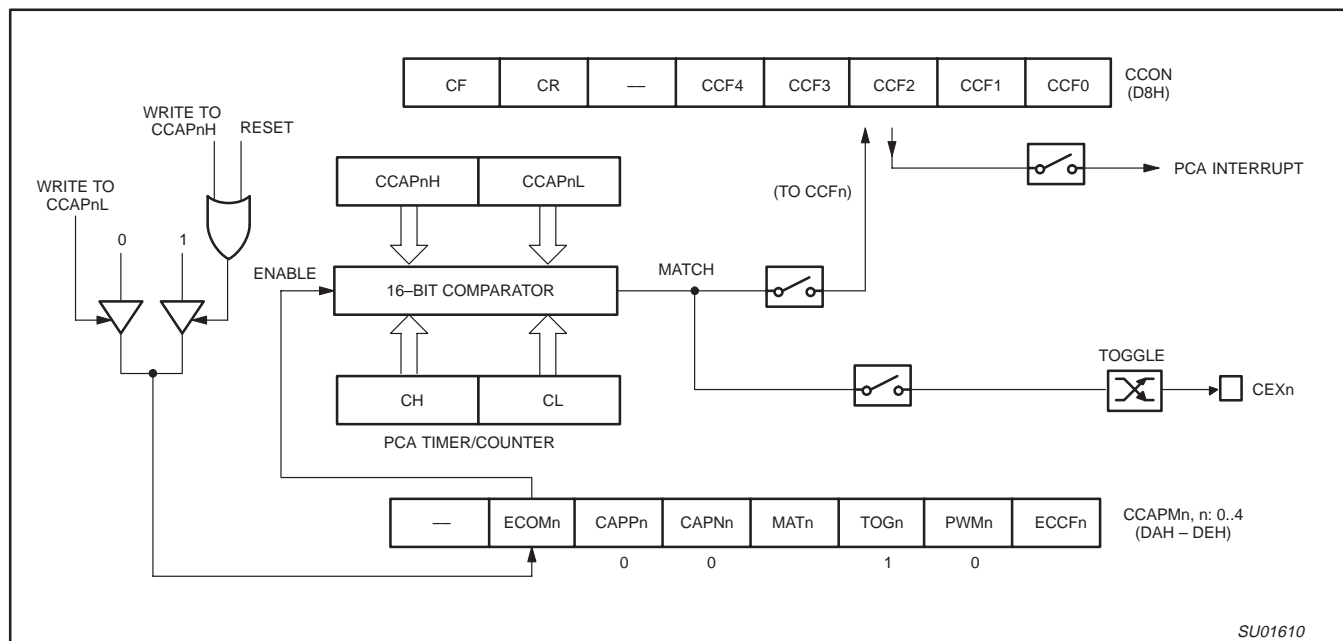


Figure 28. PCA High Speed Output Mode

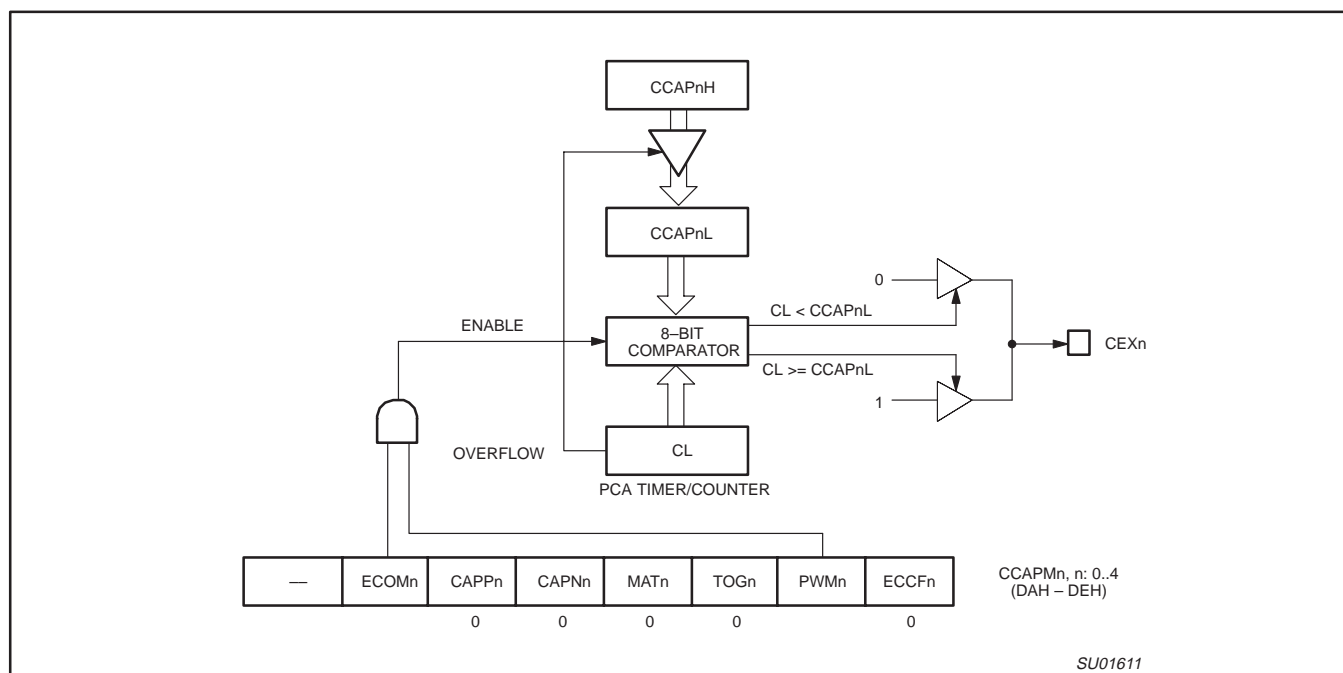


Figure 29. PCA PWM Mode

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

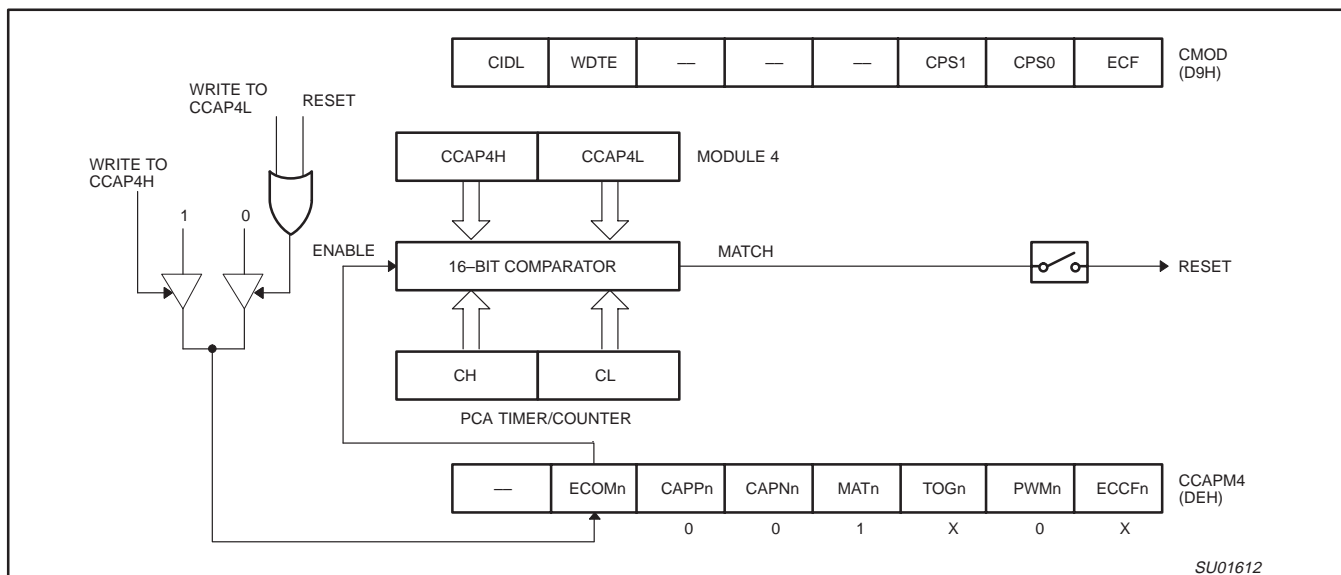


Figure 30. PCA Watchdog Timer mode (Module 4 only)

PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 30 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 31 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine in Figure 31.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on \overline{EA}/V_{PP} pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS} ⁴	–0.5 to +6.0	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
- Transient voltage only.

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$

SYMBOL	FIGURE	PARAMETER	OPERATING MODE	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY RANGE		UNIT
					MIN	MAX	
$1/t_{CLCL}$	38	Oscillator frequency	6-clock	5 V \pm 10%	0	30	MHz
			6-clock	2.7 V to 5.5 V	0	16	MHz
			12-clock	5 V \pm 10%	0	33	MHz
			12-clock	2.7 V to 5.5 V	0	16	MHz

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 2.7\text{ V}$ to 5.5 V ; $V_{SS} = 0\text{ V}$ (16 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage ¹¹	$4.0\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
		$2.7\text{ V} < V_{CC} < 4.0\text{ V}$	-0.5		$0.7 V_{CC}$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, \overline{EA})		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ¹¹		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, ⁸	$V_{CC} = 2.7\text{ V}$; $I_{OL} = 1.6\text{ mA}^2$	—		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{8, 7}	$V_{CC} = 2.7\text{ V}$; $I_{OL} = 3.2\text{ mA}^2$	—		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 2.7\text{ V}$; $I_{OH} = -20\text{ }\mu\text{A}$	$V_{CC} - 0.7$		—	V
		$V_{CC} = 4.5\text{ V}$; $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		—	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 2.7\text{ V}$; $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		—	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$; See note 4	—		-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	—		± 10	μA
I_{CC}	Power supply current (see Figure 41 and Source Code): Active mode @ 16 MHz Idle mode @ 16 MHz Power-down mode or clock stopped (see Figure 37 for conditions) ¹²	$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$				μA
						μA
				2	30	μA
				3	50	μA
V_{RAM}	RAM keep-alive voltage		1.2			V
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except \overline{EA})		—		15	pF

NOTES:

- Typical ratings are not guaranteed. Values listed are based on tests conducted on limited number of samples at room temperature.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{ pF}$), the noise pulse on the ALE pin may exceed 0.8 V . In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V .
- See Figures 43 through 46 for I_{CC} test conditions and Figure 41 for I_{CC} vs. Frequency
12-clock mode characteristics:
Active mode (operating): $I_{CC} = 1.0\text{ mA} + 1.1\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Active mode (reset): $I_{CC} = 7.0\text{ mA} + 0.6\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Idle mode: $I_{CC} = 1.0\text{ mA} + 0.22\text{ mA} \times \text{FREQ.}[\text{MHz}]$
- This value applies to $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$. For $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $I_{TL} = -750\text{ }\mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF , load capacitance for all other outputs = 80 pF .
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is $85\text{ }^{\circ}\text{C}$ specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF . Pin capacitance of ceramic package is less than 15 pF (except \overline{EA} is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.
- Power down mode for 3 V range: Commercial Temperature Range – typ. $0.5\text{ }\mu\text{A}$, max. $20\text{ }\mu\text{A}$; Industrial Temperature Range – typ. $1.0\text{ }\mu\text{A}$, max. $30\text{ }\mu\text{A}$;

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$ (30/33 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage ¹¹	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, EA)		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ¹¹		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{ V}$; $I_{OL} = 1.6\text{ mA}^2$	-		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{7, 8}	$V_{CC} = 4.5\text{ V}$; $I_{OL} = 3.2\text{ mA}^2$	-		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{ V}$; $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		-	V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 4.5\text{ V}$; $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		-	V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$; See note 4	-		-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	-		± 10	μA
I_{CC}	Power supply current Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 46 for conditions)	$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$		2	30	μA
		$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		3	50	μA
V_{RAM}	RAM keep-alive voltage		1.2			V
R_{RST}	Internal reset pull-down resistor		40		225	$\text{k}\Omega$
C_{IO}	Pin capacitance ¹⁰ (except EA)		-		15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{ pF}$), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 43 through 46 for I_{CC} test conditions and Figure 41 for I_{CC} vs. Frequency.
12-clock mode characteristics:
Active mode (operating): $I_{CC} = 1.0\text{ mA} + 1.1\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Active mode (reset): $I_{CC} = 7.0\text{ mA} + 0.6\text{ mA} \times \text{FREQ.}[\text{MHz}]$
Idle mode: $I_{CC} = 1.0\text{ mA} + 0.22\text{ mA} \times \text{FREQ.}[\text{MHz}]$
- This value applies to $T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$. For $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $I_{TL} = -750\text{ }\mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85 $^{\circ}\text{C}$ specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except EA is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

AC ELECTRICAL CHARACTERISTICS (6-CLOCK MODE, 2.7 V TO 5.5 V OPERATION)

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{CC}=2.7\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$ ^{1,2,3,4,5}

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	38	Oscillator frequency	0	16			MHz
t_{LHLL}	34	ALE pulse width	$t_{CLCL}-10$		52.5		ns
t_{AVLL}	34	Address valid to ALE low	$0.5\ t_{CLCL}-15$		16.25		ns
t_{LLAX}	34	Address hold after ALE low	$0.5\ t_{CLCL}-25$		6.25		ns
t_{LLIV}	34	ALE low to valid instruction in		$2\ t_{CLCL}-55$		70	ns
t_{LLPL}	34	ALE low to PSEN low	$0.5\ t_{CLCL}-15$		16.25		ns
t_{PLPH}	34	PSEN pulse width	$1.5\ t_{CLCL}-15$		78.75		ns
t_{PLIV}	34	PSEN low to valid instruction in		$1.5\ t_{CLCL}-55$		38.75	ns
t_{PXIX}	34	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	34	Input instruction float after PSEN		$0.5\ t_{CLCL}-10$		21.25	ns
t_{AVIV}	34	Address to valid instruction in		$2.5\ t_{CLCL}-50$		101.25	ns
t_{PLAZ}	34	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	35	RD pulse width	$3\ t_{CLCL}-25$		162.5		ns
t_{WLWH}	36	WR pulse width	$3\ t_{CLCL}-25$		162.5		ns
t_{RLDV}	35	RD low to valid data in		$2.5\ t_{CLCL}-50$		106.25	ns
t_{RHDX}	35	Data hold after RD	0		0		ns
t_{RHDZ}	35	Data float after RD		$t_{CLCL}-20$		42.5	ns
t_{LLDV}	35	ALE low to valid data in		$4\ t_{CLCL}-55$		195	ns
t_{AVDV}	35	Address to valid data in		$4.5\ t_{CLCL}-50$		231.25	ns
t_{LLWL}	35, 36	ALE low to RD or WR low	$1.5\ t_{CLCL}-20$	$1.5\ t_{CLCL}+20$	73.75	113.75	ns
t_{AVWL}	35, 36	Address valid to WR low or RD low	$2\ t_{CLCL}-20$		105		ns
t_{QVWX}	36	Data valid to WR transition	$0.5\ t_{CLCL}-30$		1.25		ns
t_{WHQX}	36	Data hold after WR	$0.5\ t_{CLCL}-20$		11.25		ns
t_{QVWH}	36	Data valid to WR high	$3.5\ t_{CLCL}-10$		208.75		ns
t_{RLAZ}	35	RD low to address float		0		0	ns
t_{WHLH}	35, 36	RD or WR high to ALE high	$0.5\ t_{CLCL}-15$	$0.5\ t_{CLCL}+15$	16.25	46.25	ns
External Clock							
t_{CHCX}	38	High time	$0.4\ t_{CLCL}$	$t_{CLCL}-t_{CLCX}$			ns
t_{CLCX}	38	Low time	$0.4\ t_{CLCL}$	$t_{CLCL}-t_{CHCX}$			ns
t_{CLCH}	38	Rise time		5			ns
t_{CHCL}	38	Fall time		5			ns
Shift register							
t_{XLXL}	37	Serial port clock cycle time	$6\ t_{CLCL}$		375		ns
t_{QVXH}	37	Output data setup to clock rising edge	$5\ t_{CLCL}-25$		287.5		ns
t_{XHGX}	37	Output data hold after clock rising edge	$t_{CLCL}-15$		47.5		ns
t_{XHDX}	37	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	37	Clock rising edge to input data valid ⁶		$5\ t_{CLCL}-133$		179.5	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN=100 pF, load capacitance for all outputs = 80 pF
- Interfacing the microcontroller to devices with float time up to 45ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
- Parts are guaranteed by design to operate down to 0 Hz.
- Data shown in the table are the best mathematical models for the set of measured values obtained in tests. If a particular parameter calculated at a customer specified frequency has a negative value, it should be considered equal to zero.
- Below 16 MHz this parameter is $4\ t_{CLCL}-133$

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

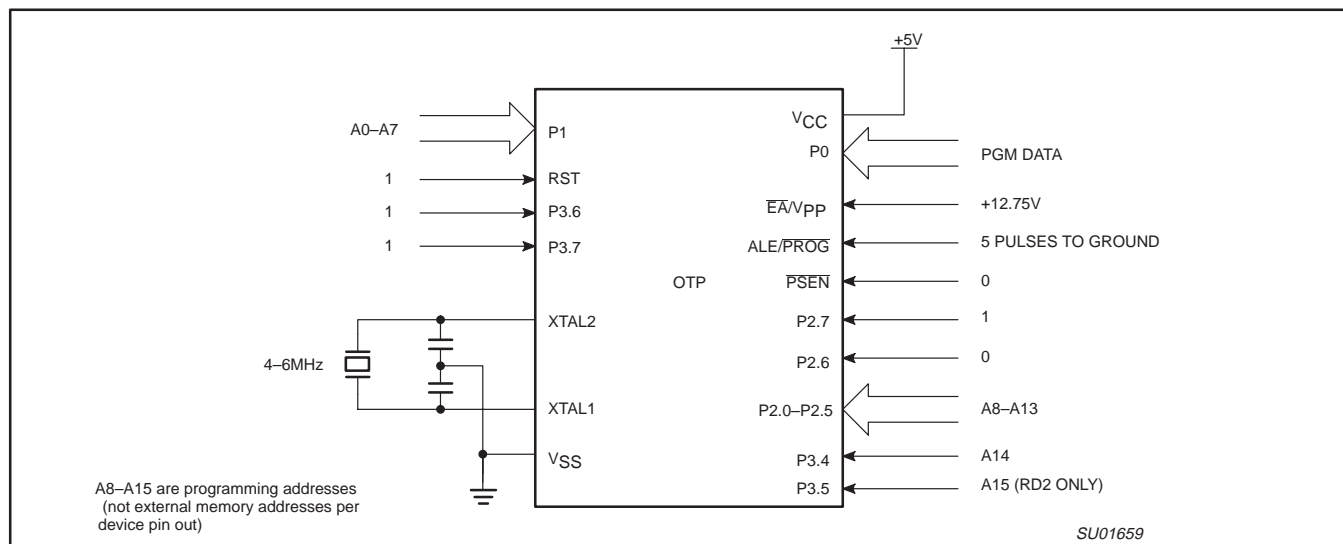


Figure 47. Programming Configuration

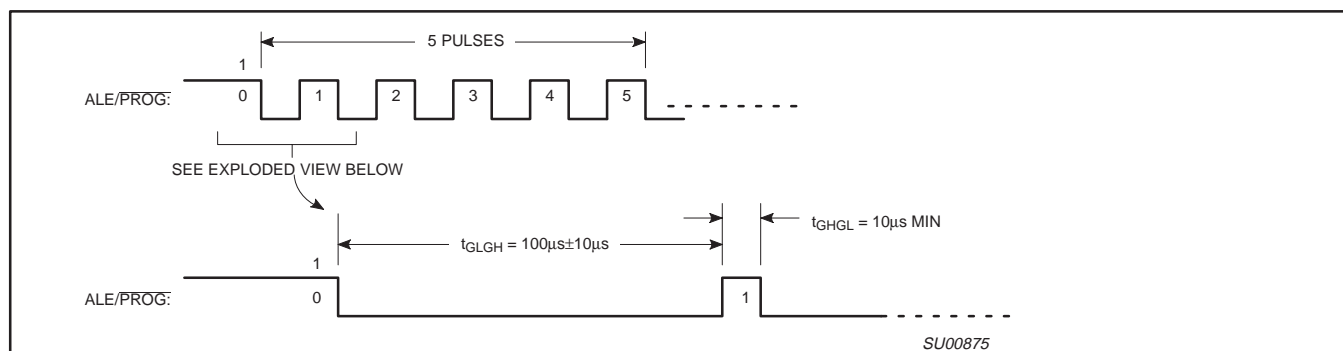


Figure 48. PROG Waveform

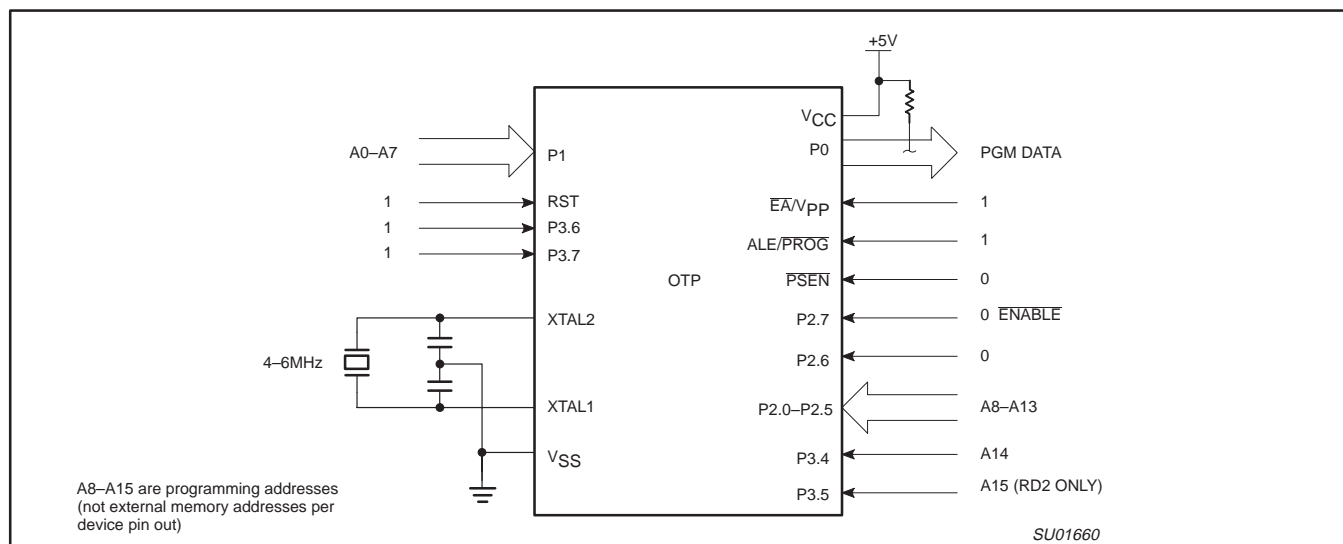


Figure 49. Program Verification

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

ROM CODE SUBMISSION FOR 16K ROM DEVICES (87C51RB2)

When submitting ROM code for the 16K ROM devices, the following must be specified:

1. 16 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 3FFFH	DATA	7:0	User ROM Data
4000H to 403FH	KEY	7:0	ROM Encryption Key FFH = no encryption
4040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
4040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOV_C is disabled, and
2. \overline{EA} is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

ROM CODE SUBMISSION FOR 32K ROM DEVICES (87C51RC2)

When submitting ROM code for the 32K ROM devices, the following must be specified:

1. 32 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 7FFFH	DATA	7:0	User ROM Data
8000H to 803FH	KEY	7:0	ROM Encryption Key FFH = no encryption
8040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
8040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOV_C is disabled, and
2. \overline{EA} is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

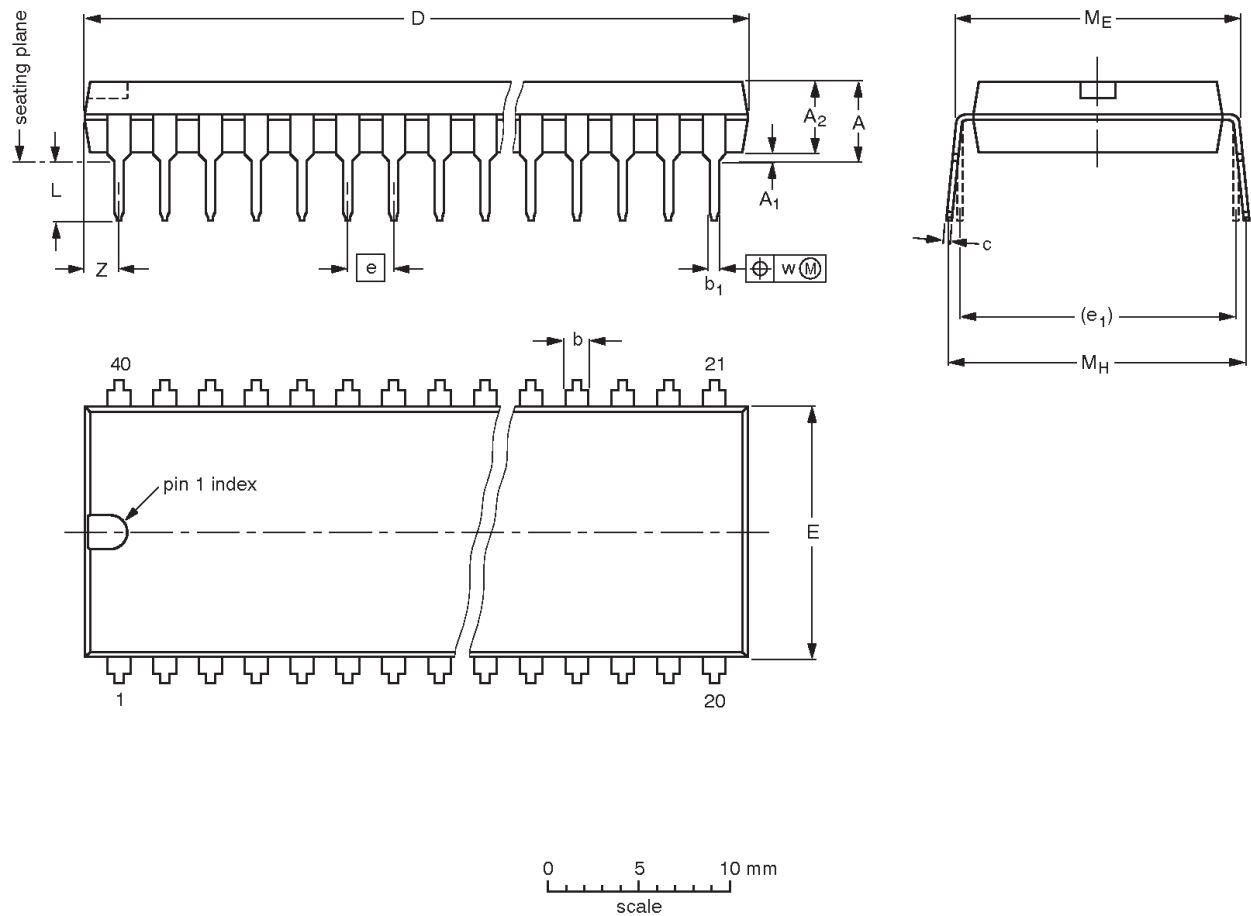
Encryption: ☐ No ☐ Yes If Yes, must send key file.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015	SC-511-40			95-01-14 99-12-27