

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

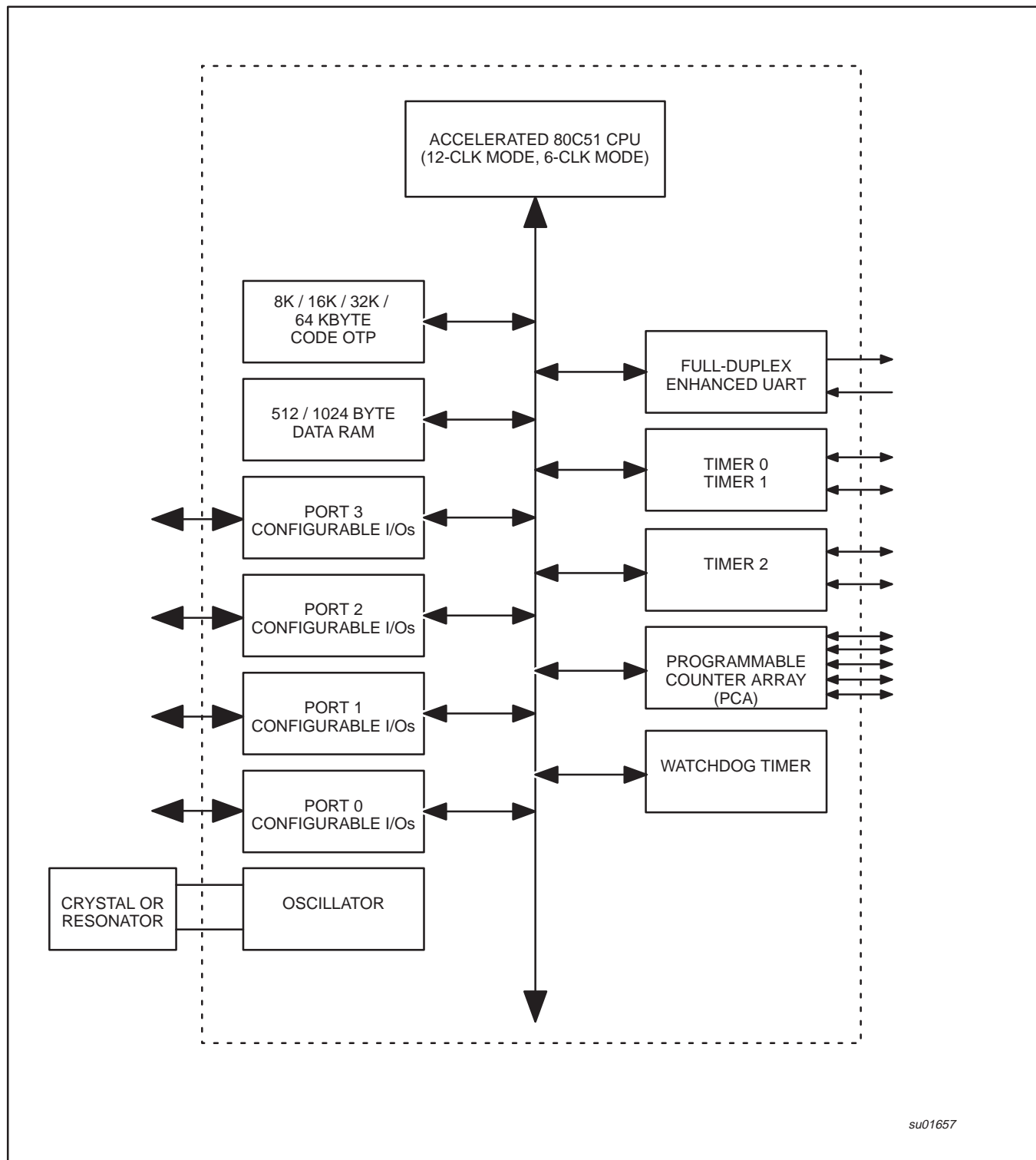
#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51rd2bbd-157">https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51rd2bbd-157</a>

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

**BLOCK DIAGRAM 1**



80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

## SPECIAL FUNCTION REGISTERS

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	EXTRAM	AO	xxxxxx00B
AUXR1#	Auxiliary 1	A2H	–	–	–	–	GF2	0	–	DPS	xxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxB
CCAPM0#	Module 0 Mode	DAH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM3#	Module 3 Mode	DDH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM4#	Module 4 Mode	DEH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCON*#	PCA Counter Control	D8H	DF	DE	DD	DC	DB	DA	D9	D8	00x00000B
			CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	
CH#	PCA Counter High	F9H									00H
CKCON#	Clock control	8FH	–	–	–	–	–	–	–	X2	x0000000B
											00H
CL#	PCA Counter Low	E9H									00H
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00xxx000B
DPTR:	Data Pointer (2 bytes)	83H									00H
			82H								
IE*	Interrupt Enable 0	A8H	AF	AE	AD	AC	AB	AA	A9	A8	00H
			EA	EC	ET2	ES	ET1	EX1	ET0	EX0	
IP*	Interrupt Priority	B8H	BF	BE	BD	BC	BB	BA	B9	B8	x0000000B
			–	PPC	PT2	PS	PT1	PX1	PT0	PX0	
IPH#	Interrupt Priority High	B7H	B7	B6	B5	B4	B3	B2	B1	B0	x0000000B
			–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	
P0*	Port 0	80H	87	86	85	84	83	82	81	80	FFH
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
P1*	Port 1	90H	97	96	95	94	93	92	91	90	FFH
			CEX4	CEX3	CEX2	CEX1	CEX0	ECI	T2EX	T2	
P2*	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
			AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
			R $\overline{D}$	W $\overline{R}$	T1	T0	INT1	INT0	TxD	RxD	
PCON# <sup>1</sup>	Power Control	87H									00xxx000B
			SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL	

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

– Reserved bits.

1. Reset value depends on reset source.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

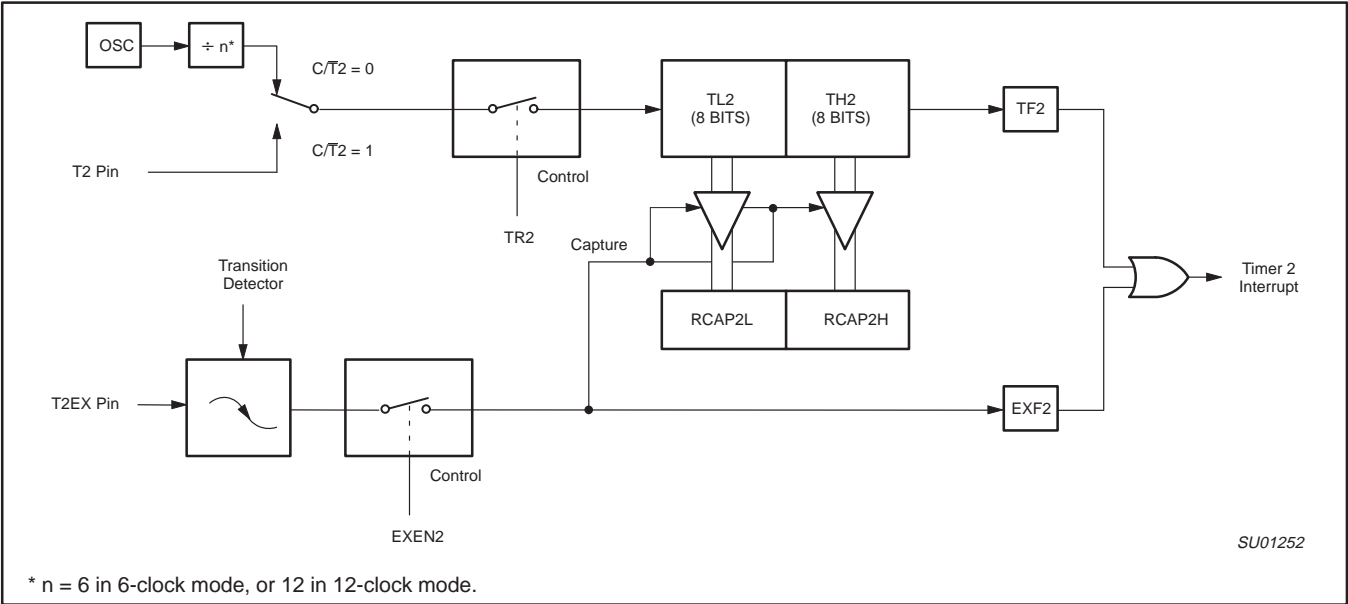


Figure 2. Timer 2 in Capture Mode

<b>T2MOD</b>	Address = 0C9H	Reset Value = XXXX XX00B																
Not Bit Addressable																		
	<table><tr><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>T2OE</td><td>DCEN</td></tr><tr><td>Bit 7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr></table>	—	—	—	—	—	—	T2OE	DCEN	Bit 7	6	5	4	3	2	1	0	
—	—	—	—	—	—	T2OE	DCEN											
Bit 7	6	5	4	3	2	1	0											
<b>Symbol</b>	<b>Function</b>																	
—	Not implemented, reserved for future use.*																	
T2OE	Timer 2 Output Enable bit.																	
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.																	
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.																		

SU00729

Figure 3. Timer 2 Mode (T2MOD) Control Register

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

SCON

Address = 98H

Reset Value = 00H

Bit Addressable

7

6

5

4

3

2

1

0

SM0

SM1

SM2

REN

TB8

RB8

TI

RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0

SM1

Mode

Description

Baud Rate

0

0

0

shift register

$f_{OSC}/12$  (12-clock mode) or  $f_{OSC}/6$  (6-clock mode)

0

1

1

8-bit UART

variable

1

0

2

9-bit UART

$f_{OSC}/64$  or  $f_{OSC}/32$  (12-clock mode) or  $f_{OSC}/32$  or  $f_{OSC}/16$  (6-clock mode)

1

1

3

9-bit UART

variable

SM2

Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.

REN

Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8

The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8

In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, if SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI

Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

RI

Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

SU01626

SU01626

Figure 7. Serial Port Control (SCON) Register

Baud Rate			$f_{osc}$	SMOD	Timer 1		
Mode	12-clock mode	6-clock mode			C/T	Mode	Reload Value
Mode 0 Max	1.67 MHz	3.34 MHz	20 MHz	X	X	X	X
Mode 2 Max	625 k	1250 k	20 MHz	1	X	X	X
Mode 1, 3 Max	104.2 k	208.4 k	20 MHz	1	0	2	FFH
Mode 1, 3	19.2 k	38.4 k	11.059 MHz	1	0	2	FDH
	9.6 k	19.2 k	11.059 MHz	0	0	2	FDH
	4.8 k	9.6 k	11.059 MHz	0	0	2	FAH
	2.4 k	4.8 k	11.059 MHz	0	0	2	F4H
	1.2 k	2.4 k	11.059 MHz	0	0	2	E8H
	137.5	275	11.986 MHz	0	0	2	1DH
	110	220	6 MHz	0	0	2	72H
	110	220	12 MHz	0	0	1	FEEDH

Figure 8. Timer 1 Generated Commonly Used Baud Rates

#### More About Mode 0

Serial data enters and exits through Rx/D. Tx/D outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed a 1/12 the oscillator frequency (12-clock mode) or 1/6 the oscillator frequency (6-clock mode).

Figure 9 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF" and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At

S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF."

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

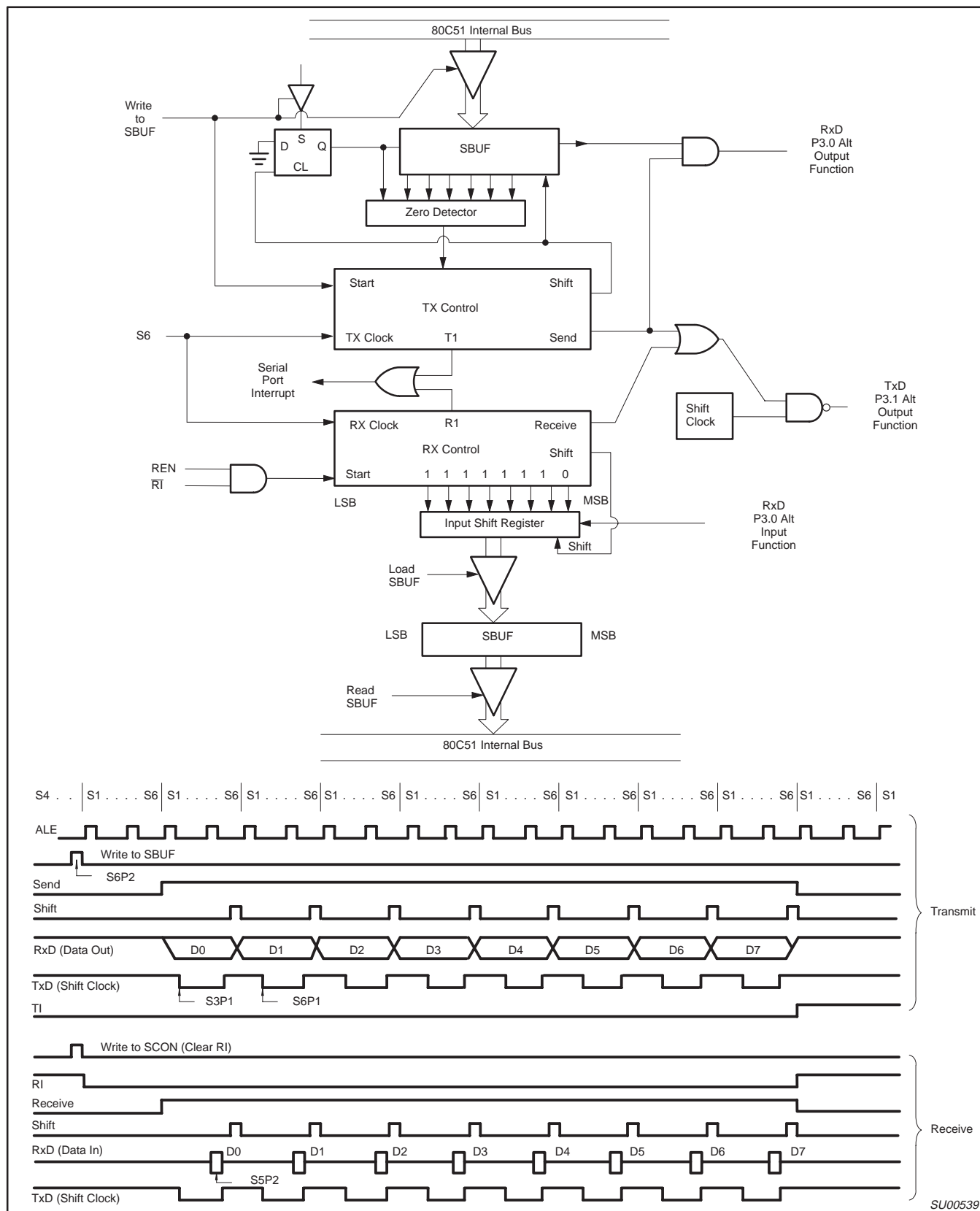
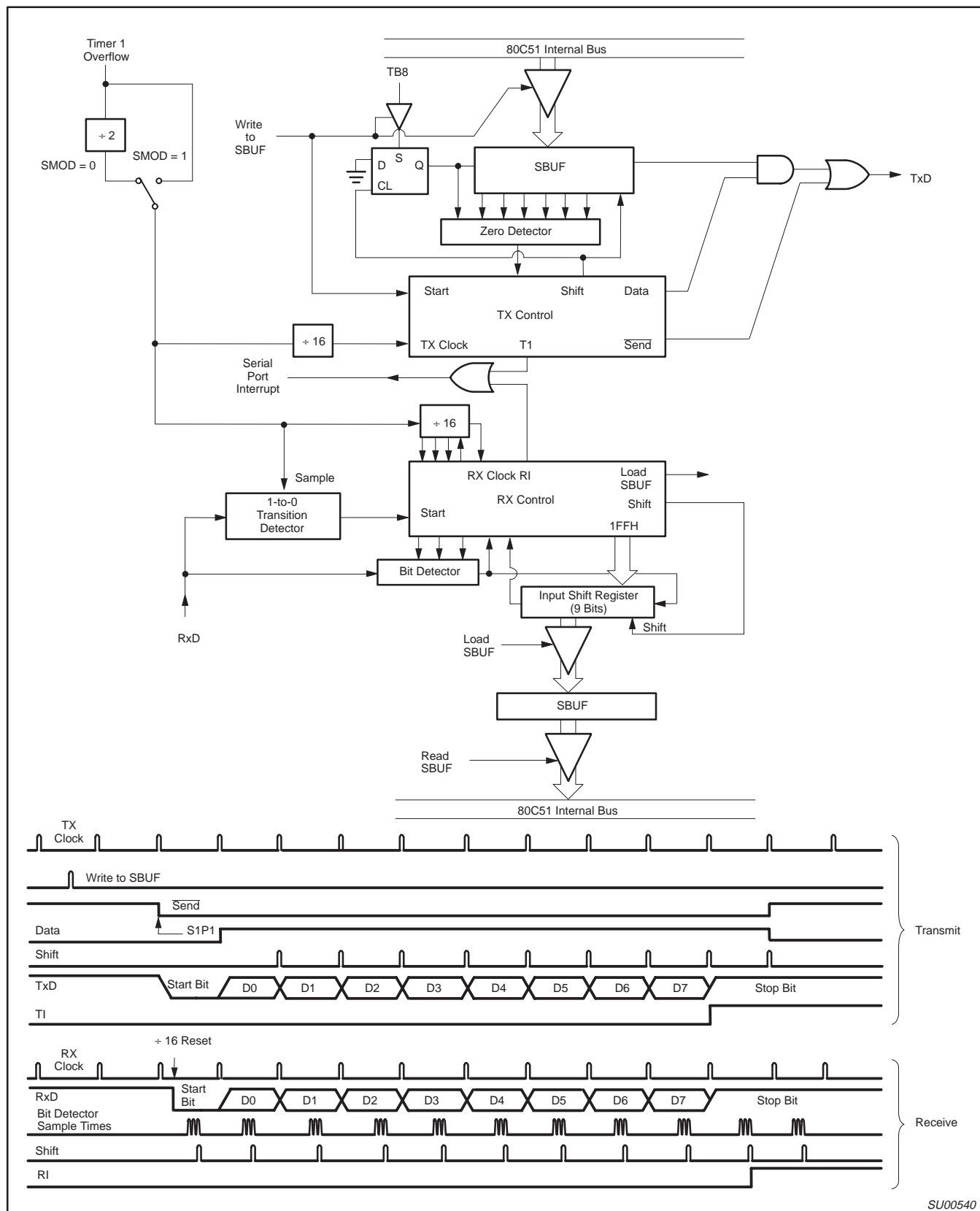


Figure 9. Serial Port Mode 0

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2



SU00540

Figure 10. Serial Port Mode 1

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

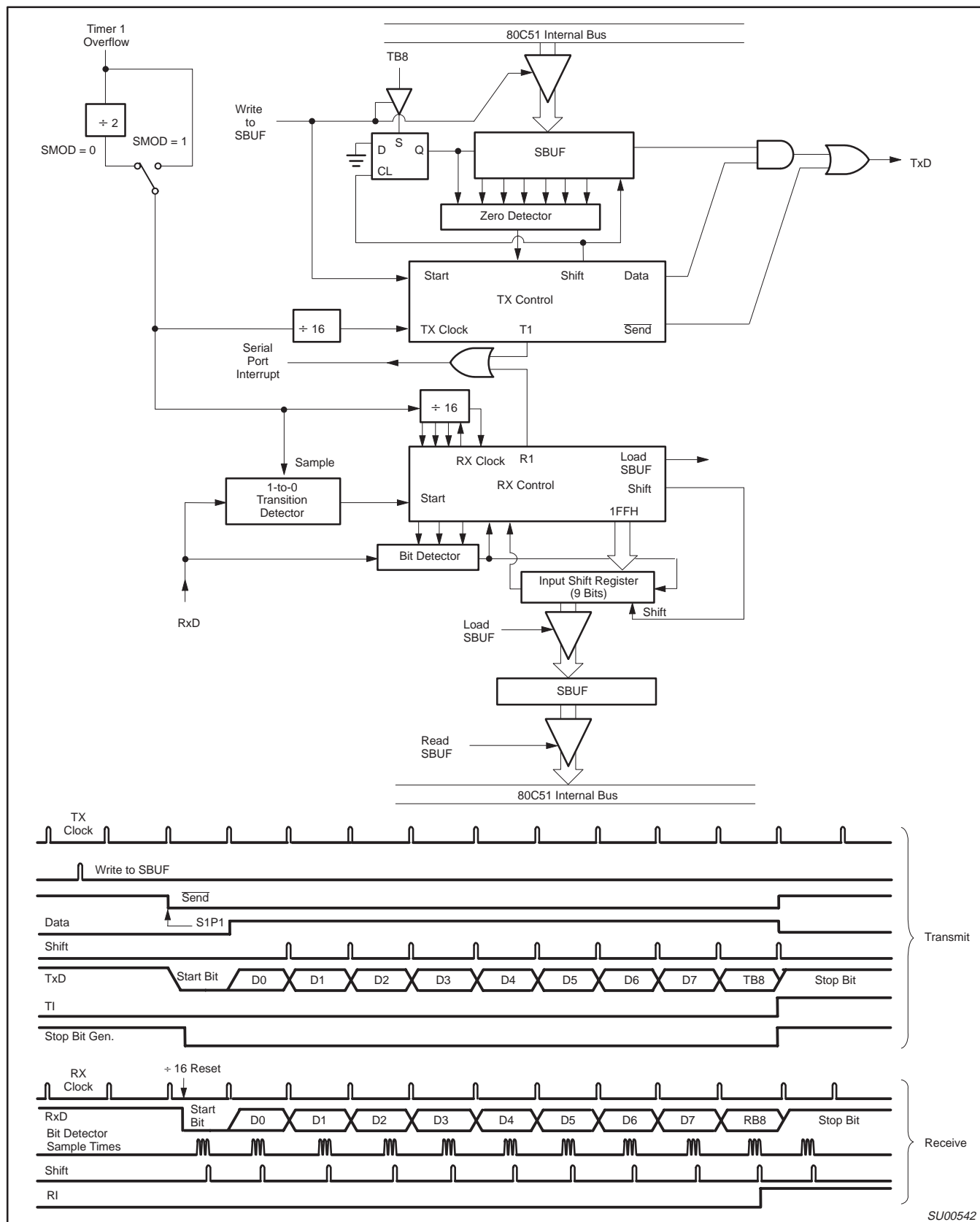


Figure 12. Serial Port Mode 3



80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

## P87C51RA2/RB2/RC2/RD2

### Enhanced Features

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 13.

### Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 14.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1101
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	1111 1110
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1001
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	1111 1010
	Given =	1110 0XX0
Slave 2	SADDR =	1110 0000
	SADEN =	1111 1100
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

		7	6	5	4	3	2	1	0
IP (0B8H)		–	PPC	PT2	PS	PT1	PX1	PT0	PX0
		Priority Bit = 1 assigns high priority Priority Bit = 0 assigns low priority							
BIT	SYMBOL	FUNCTION							
IP.7	–	–							
IP.6	PPC	PCA interrupt priority bit							
IP.5	PT2	Timer 2 interrupt priority bit.							
IP.4	PS	Serial Port interrupt priority bit.							
IP.3	PT1	Timer 1 interrupt priority bit.							
IP.2	PX1	External interrupt 1 priority bit.							
IP.1	PT0	Timer 0 interrupt priority bit.							
IP.0	PX0	External interrupt 0 priority bit.							

SU01291

Figure 16. IP Registers

		7	6	5	4	3	2	1	0
IPH (B7H)		–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Priority Bit = 1 assigns higher priority Priority Bit = 0 assigns lower priority							
BIT	SYMBOL	FUNCTION							
IPH.7	–	–							
IPH.6	PPCH	PCA interrupt priority bit							
IPH.5	PT2H	Timer 2 interrupt priority bit high.							
IPH.4	PSH	Serial Port interrupt priority bit high.							
IPH.3	PT1H	Timer 1 interrupt priority bit high.							
IPH.2	PX1H	External interrupt 1 priority bit high.							
IPH.1	PT0H	Timer 0 interrupt priority bit high.							
IPH.0	PX0H	External interrupt 0 priority bit high.							

SU01292

Figure 17. IPH Registers

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

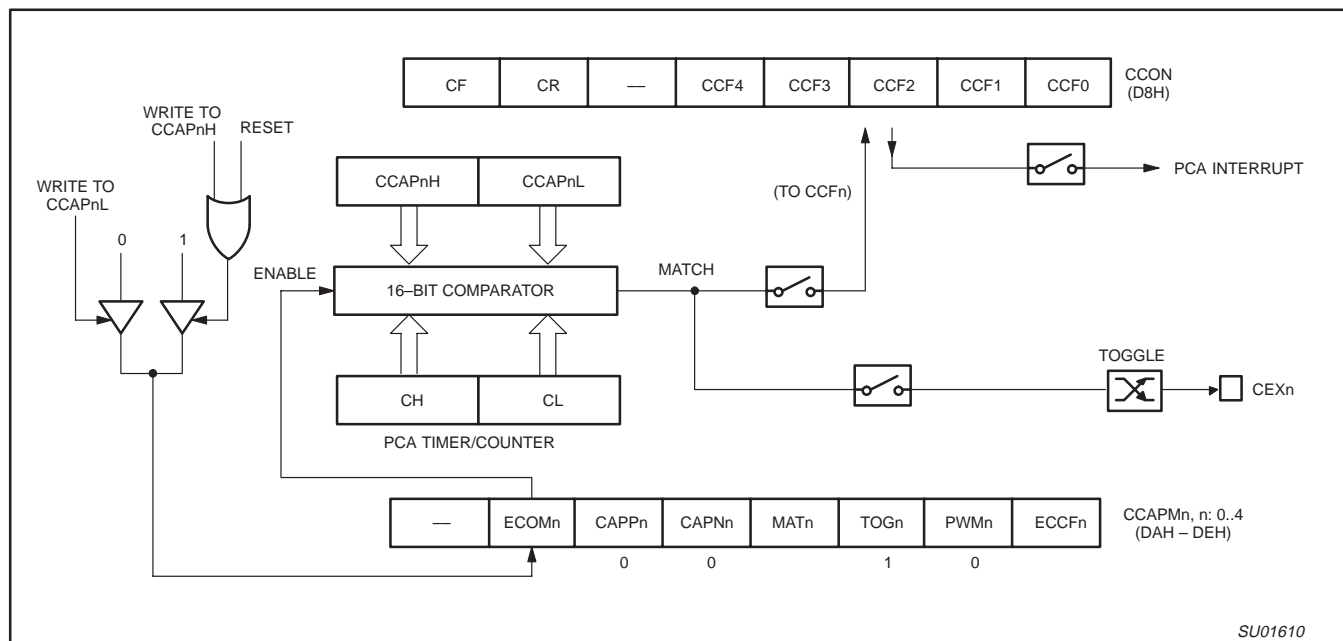


Figure 28. PCA High Speed Output Mode

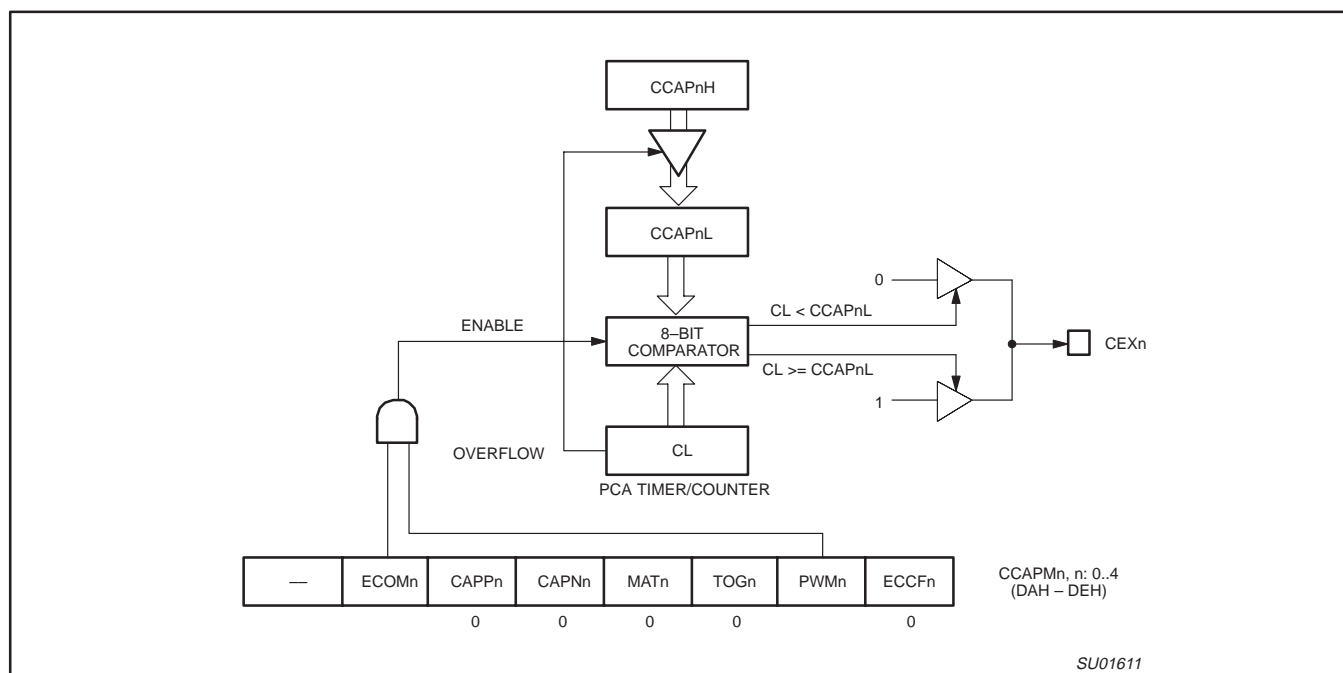


Figure 29. PCA PWM Mode

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

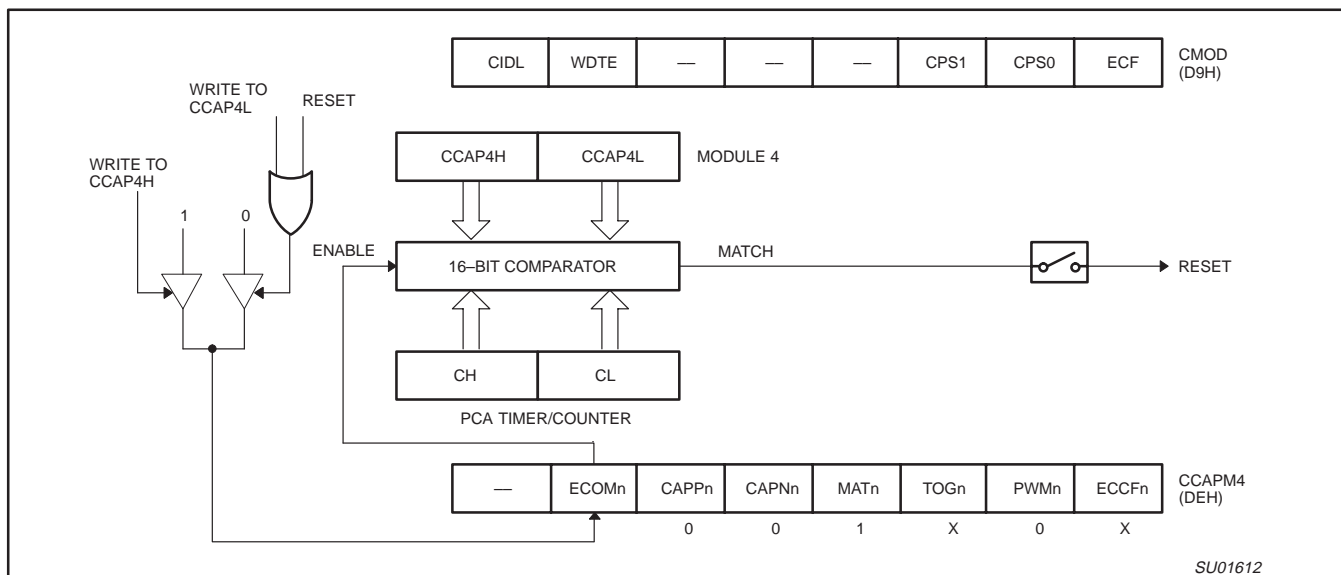


Figure 30. PCA Watchdog Timer mode (Module 4 only)

### PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 30 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 31 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine in Figure 31.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within  $2^{16}$  count of the PCA timer.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

## P87C51RA2/RB2/RC2/RD2

### Expanded Data RAM Addressing

The P87C51RA2/RB2/RC2/RD2 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes expanded RAM (ERAM) (768 bytes for the RD2).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256/768-bytes expanded RAM (ERAM, 00H – 1FFH/2FFH) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared, see Figure 32.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

```
MOV 0A0H,#data
```

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 bytes of data RAM.

For example:

```
MOV @R0,acc
```

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The ERAM can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 256/768 bytes of external data memory in the P87C51RA2/RB2/RC2/RD2.

With EXTRAM = 0, the ERAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ERAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is output during external addressing. For example, with EXTRAM = 0,

```
MOVX @R0,acc
```

where R0 contains 0A0H, accesses the ERAM at address 0A0H rather than external memory. An access to external data memory locations higher than the ERAM will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 33.

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high-order eight address bits (the contents of DPH) while Port 0 multiplexes the low-order eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 (WR) and P3.7 (RD).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the ERAM.

<b>AUXR</b> Address = 8EH		Reset Value = xxxx xx00B							
Not Bit Addressable									
		—	—	—	—	—	—	<b>EXTRAM</b>	<b>AO</b>
Bit:		7	6	5	4	3	2	1	0
<b>Symbol</b>	<b>Function</b>								
<b>AO</b>	Disable/Enable ALE								
	<b>AO</b>								
	0	ALE is emitted at a constant rate of $\frac{1}{6}$ the oscillator frequency (12-clock mode; $\frac{1}{3} f_{OSC}$ in 6-clock mode).							
	1	ALE is active only during off-chip memory access.							
<b>EXTRAM</b>	Internal/External RAM access using MOVX @Ri/@DPTR								
	<b>EXTRAM</b>								
	0	Internal ERAM access using MOVX @Ri/@DPTR							
	1	External data memory access.							
—	Not implemented, reserved for future use*.								
<b>NOTE:</b>									
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.									

SU01613

Figure 32. AUXR: Auxiliary Register

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

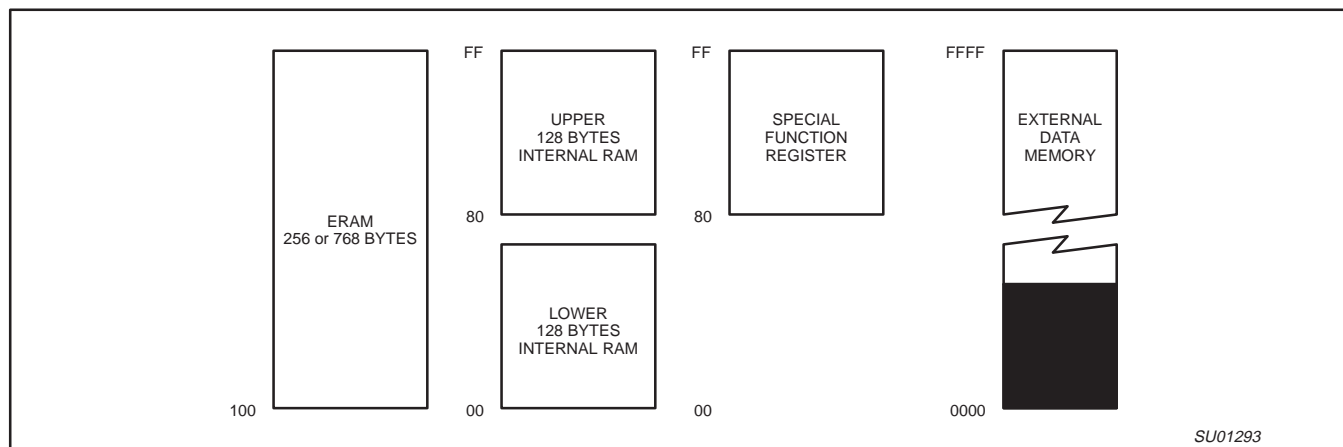


Figure 33. Internal and External Data Memory Address Space with EXTRAM = 0

### HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT FOR P87C51RA2/RB2/RC2/RD2)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, the user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When the WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When the WDT overflows, it will drive an output reset HIGH pulse at the RST-pin (see the note below).

### Using the WDT

To enable the WDT, the user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When the WDT overflows, it will generate an output RESET pulse at the reset pin (see note below). The RESET pulse duration is  $98 \times T_{OSC}$  (6-clock mode; 196 in 12-clock mode), where  $T_{OSC} = 1/f_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

## DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$  or  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $V_{SS} = 0\text{ V}$  (30/33 MHz max. CPU clock)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>1</sup>	MAX	
$V_{IL}$	Input low voltage <sup>11</sup>	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
$V_{IH}$	Input high voltage (ports 0, 1, 2, 3, EA)		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
$V_{IH1}$	Input high voltage, XTAL1, RST <sup>11</sup>		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
$V_{OL}$	Output low voltage, ports 1, 2, 3 <sup>8</sup>	$V_{CC} = 4.5\text{ V}$ ; $I_{OL} = 1.6\text{ mA}^2$	-		0.4	V
$V_{OL1}$	Output low voltage, port 0, ALE, PSEN <sup>7, 8</sup>	$V_{CC} = 4.5\text{ V}$ ; $I_{OL} = 3.2\text{ mA}^2$	-		0.4	V
$V_{OH}$	Output high voltage, ports 1, 2, 3 <sup>3</sup>	$V_{CC} = 4.5\text{ V}$ ; $I_{OH} = -30\text{ }\mu\text{A}$	$V_{CC} - 0.7$		-	V
$V_{OH1}$	Output high voltage (port 0 in external bus mode), ALE <sup>9</sup> , PSEN <sup>3</sup>	$V_{CC} = 4.5\text{ V}$ ; $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$		-	V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-50	$\mu\text{A}$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3 <sup>6</sup>	$V_{IN} = 2.0\text{ V}$ ; See note 4	-		-650	$\mu\text{A}$
$I_{LI}$	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$	-		$\pm 10$	$\mu\text{A}$
$I_{CC}$	Power supply current Active mode (see Note 5) Idle mode (see Note 5)  Power-down mode or clock stopped (see Figure 46 for conditions)	$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$		2	30	$\mu\text{A}$
		$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		3	50	$\mu\text{A}$
$V_{RAM}$	RAM keep-alive voltage		1.2			V
$R_{RST}$	Internal reset pull-down resistor		40		225	$\text{k}\Omega$
$C_{IO}$	Pin capacitance <sup>10</sup> (except EA)		-		15	pF

### NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the  $V_{OL}$ s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading  $> 100\text{ pF}$ ), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.  $I_{OL}$  can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and PSEN to momentarily fall below the  $V_{CC} - 0.7$  specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when  $V_{IN}$  is approximately 2 V.
- See Figures 43 through 46 for  $I_{CC}$  test conditions and Figure 41 for  $I_{CC}$  vs. Frequency.  
12-clock mode characteristics:  
Active mode (operating):  $I_{CC} = 1.0\text{ mA} + 1.1\text{ mA} \times \text{FREQ.}[\text{MHz}]$   
Active mode (reset):  $I_{CC} = 7.0\text{ mA} + 0.6\text{ mA} \times \text{FREQ.}[\text{MHz}]$   
Idle mode:  $I_{CC} = 1.0\text{ mA} + 0.22\text{ mA} \times \text{FREQ.}[\text{MHz}]$
- This value applies to  $T_{amb} = 0\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ . For  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $I_{TL} = -750\text{ }\mu\text{A}$ .
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
Maximum  $I_{OL}$  per port pin: 15 mA (\*NOTE: This is 85  $^{\circ}\text{C}$  specification.)  
Maximum  $I_{OL}$  per 8-bit port: 26 mA  
Maximum total  $I_{OL}$  for all outputs: 71 mA  
If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to  $V_{OH1}$ , except when ALE is off then  $V_{OH}$  is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except EA is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

## AC ELECTRICAL CHARACTERISTICS (12-CLOCK MODE, 2.7 V TO 5.5 V OPERATION)

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C or }-40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ <sup>1,2,3,4</sup>

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	38	Oscillator frequency	0	16			MHz
$t_{LHLL}$	34	ALE pulse width	$2t_{CLCL}-10$		115		ns
$t_{AVLL}$	34	Address valid to ALE low	$t_{CLCL}-15$		47.5		ns
$t_{LLAX}$	34	Address hold after ALE low	$t_{CLCL}-25$		37.5		ns
$t_{LLIV}$	34	ALE low to valid instruction in		$4t_{CLCL}-55$		195	ns
$t_{LLPL}$	34	ALE low to PSEN low	$t_{CLCL}-15$		47.5		ns
$t_{PLPH}$	34	PSEN pulse width	$3t_{CLCL}-15$		172.5		ns
$t_{PLIV}$	34	PSEN low to valid instruction in		$3t_{CLCL}-55$		132.5	ns
$t_{PXIX}$	34	Input instruction hold after PSEN	0		0		ns
$t_{PXIZ}$	34	Input instruction float after PSEN		$t_{CLCL}-10$		52.5	ns
$t_{AVIV}$	34	Address to valid instruction in		$5t_{CLCL}-50$		262.5	ns
$t_{PLAZ}$	34	PSEN low to address float		10		10	ns
<b>Data Memory</b>							
$t_{RLRH}$	35	$\overline{RD}$ pulse width	$6t_{CLCL}-25$		350		ns
$t_{WLWH}$	36	$\overline{WR}$ pulse width	$6t_{CLCL}-25$		350		ns
$t_{RLDV}$	35	$\overline{RD}$ low to valid data in		$5t_{CLCL}-50$		262.5	ns
$t_{RHDX}$	35	Data hold after $\overline{RD}$	0		0		ns
$t_{RHDZ}$	35	Data float after $\overline{RD}$		$2t_{CLCL}-20$		105	ns
$t_{LLDV}$	35	ALE low to valid data in		$8t_{CLCL}-55$		445	ns
$t_{AVDV}$	35	Address to valid data in		$9t_{CLCL}-50$		512.5	ns
$t_{LLWL}$	35, 36	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}-20$	$3t_{CLCL}+20$	167.5	207.5	ns
$t_{AVWL}$	35, 36	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}-20$		230		ns
$t_{QVWX}$	36	Data valid to $\overline{WR}$ transition	$t_{CLCL}-30$		32.5		ns
$t_{WHQX}$	36	Data hold after $\overline{WR}$	$t_{CLCL}-20$		42.5		ns
$t_{QVWH}$	36	Data valid to $\overline{WR}$ high	$7t_{CLCL}-10$		427.5		ns
$t_{RLAZ}$	35	$\overline{RD}$ low to address float		0		0	ns
$t_{WHLH}$	35, 36	$\overline{RD}$ or $\overline{WR}$ high to ALE high	$t_{CLCL}-15$	$t_{CLCL}+15$	47.5	77.5	ns
<b>External Clock</b>							
$t_{CHCX}$	38	High time	$0.32t_{CLCL}$	$t_{CLCL}-t_{CLCX}$			ns
$t_{CLCX}$	38	Low time	$0.32t_{CLCL}$	$t_{CLCL}-t_{CHCX}$			ns
$t_{CLCH}$	38	Rise time		5			ns
$t_{CHCL}$	38	Fall time		5			ns
<b>Shift register</b>							
$t_{XLXL}$	37	Serial port clock cycle time	$12t_{CLCL}$		750		ns
$t_{QVXH}$	37	Output data setup to clock rising edge	$10t_{CLCL}-25$		600		ns
$t_{XHQX}$	37	Output data hold after clock rising edge	$2t_{CLCL}-15$		110		ns
$t_{XHDX}$	37	Input data hold after clock rising edge	0		0		ns
$t_{XHDV}$	37	Clock rising edge to input data valid <sup>5</sup>		$10t_{CLCL}-133$		492	ns

### NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all outputs = 80 pF
- Interfacing the microcontroller to devices with float time up to 45 ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
- Parts are guaranteed by design to operate down to 0 Hz.
- Below 16 MHz this parameter is  $8t_{CLCL}-133$ .



80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

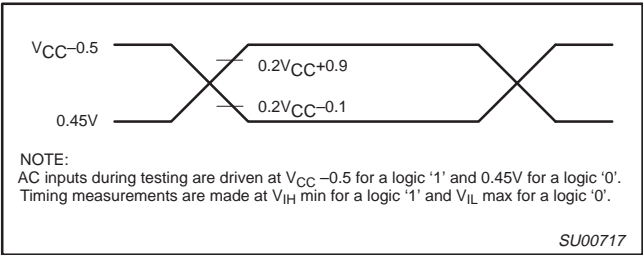


Figure 39. AC Testing Input/Output

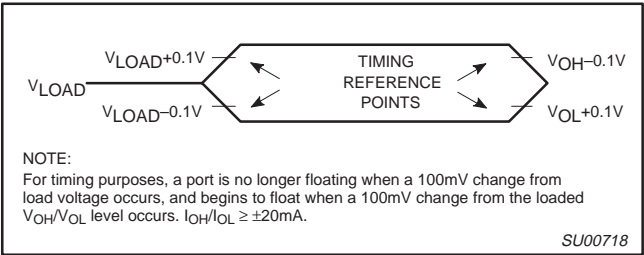


Figure 40. Float Waveform

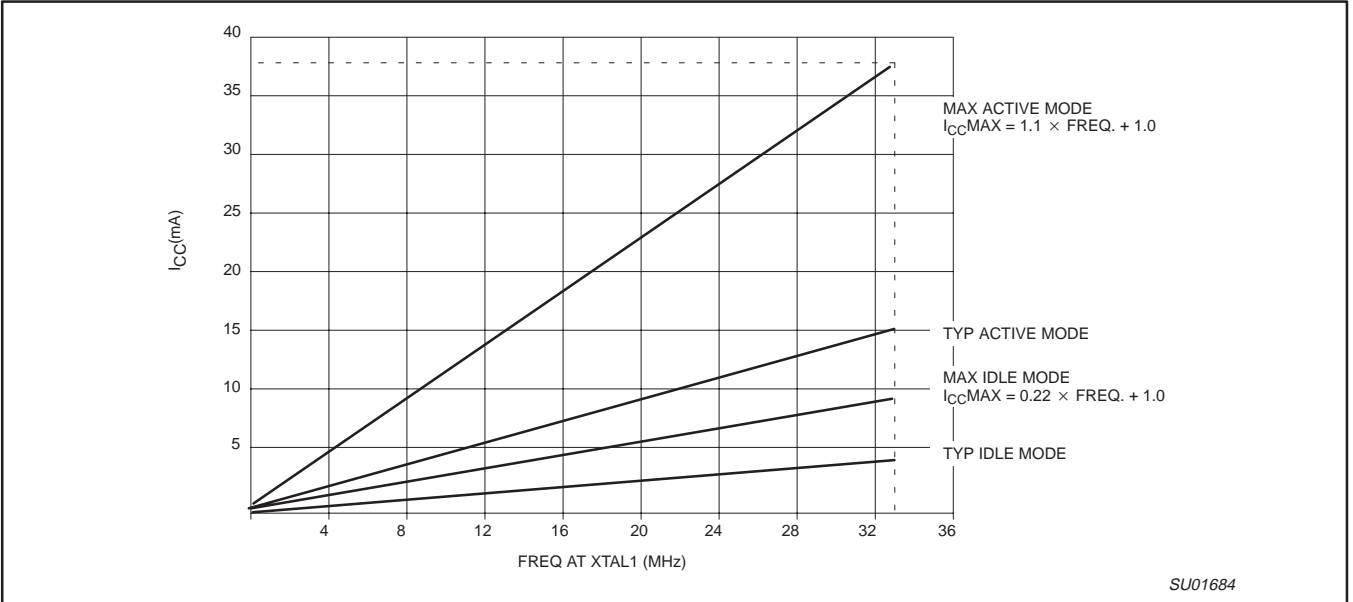


Figure 41.  $I_{CC}$  vs. FREQ for 12-clock operation  
Valid only within frequency specifications of the specified operating voltage

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

### ROM CODE SUBMISSION FOR 16K ROM DEVICES (87C51RB2)

When submitting ROM code for the 16K ROM devices, the following must be specified:

1. 16 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 3FFFH	DATA	7:0	User ROM Data
4000H to 403FH	KEY	7:0	ROM Encryption Key FFH = no encryption
4040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
4040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOV<sub>C</sub> is disabled, and
2.  $\overline{EA}$  is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1:    ☐ Enabled        ☐ Disabled

Security Bit #2:    ☐ Enabled        ☐ Disabled

Encryption:        ☐ No                ☐ Yes    If Yes, must send key file.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

### ROM CODE SUBMISSION FOR 32K ROM DEVICES (87C51RC2)

When submitting ROM code for the 32K ROM devices, the following must be specified:

1. 32 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 7FFFH	DATA	7:0	User ROM Data
8000H to 803FH	KEY	7:0	ROM Encryption Key FFH = no encryption
8040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
8040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOV<sub>C</sub> is disabled, and
2.  $\overline{EA}$  is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1:    ☐ Enabled        ☐ Disabled

Security Bit #2:    ☐ Enabled        ☐ Disabled

Encryption:        ☐ No                ☐ Yes    If Yes, must send key file.

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

**P87C51RA2/RB2/RC2/RD2**

## REVISION HISTORY

Rev	Date	Description
_3	20030124	<b>Product data (9397 750 10994); ECN 853-2391 29335 dated 07 Jan 2003.</b> Modifications: <ul style="list-style-type: none"><li>• Updated ordering information table.</li></ul>
_2	20021028	<b>Product data (9397 750 10393); ECN 853-2391 29117 dated 28 Oct 2002.</b>

80C51 8-bit microcontroller family 8KB/16KB/32KB/64KB OTP  
with 512B/1KB RAM, low voltage (2.7 to 5.5 V), low power, high  
speed (30/33 MHz)

P87C51RA2/RB2/RC2/RD2

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## Contact information

For additional information please visit  
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

© Koninklijke Philips Electronics N.V. 2003  
All rights reserved. Printed in U.S.A.

For sales offices addresses send e-mail to:  
[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

Date of release: 01-03

Document order number: 9397 750 10994

*Let's make things better.*