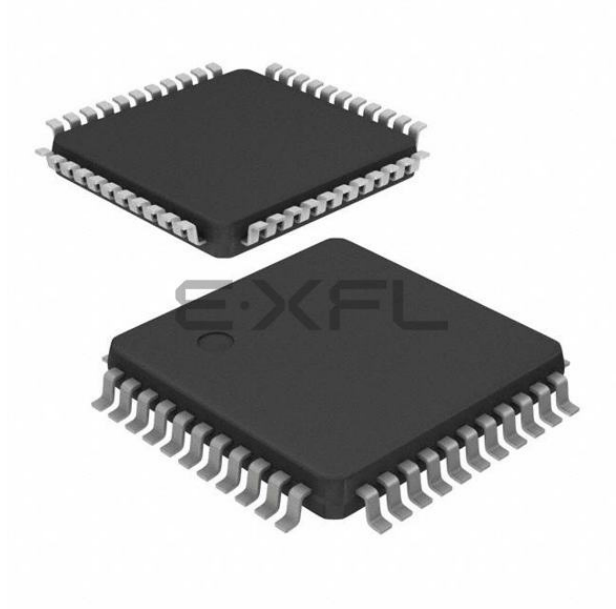

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 33MHz |
| Connectivity | EBI/EMI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51rd2fbd-01-15 |

## SELECTION TABLE

| Type | Memory | | | | Timers | | | | Serial Interfaces | | | | ADC bits/ch. | I/O Pins | Interrupts (Ext.)/Levels | Program Security | Default Clock Rate | Optional Clock Rate | Reset active low/high? | Max. Freq. at 6-clk / 12-clk (MHz) | Freq. Range at 3V (MHz) | Freq. Range at 5V (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RAM | ROM | OTP | Flash | # of Timers | PWM | PCA | WD | UART | I2C | CAN | SPI | | | | | | | | | | |
| P87C51RD2 | 1K | – | 64K | – | 4 | √ | √ | √ | √ | – | – | – | – | 32 | 7(2)/4 | √ | 12-clk | 6-clk | H | 30/33 | 0-16 | 0-30/33 |
| P87C51RC2 | 512B | – | 32K | – | 4 | √ | √ | √ | √ | – | – | – | – | 32 | 7(2)/4 | √ | 12-clk | 6-clk | H | 30/33 | 0-16 | 0-30/33 |
| P87C51RB2 | 512B | – | 16K | – | 4 | √ | √ | √ | √ | – | – | – | – | 32 | 7(2)/4 | √ | 12-clk | 6-clk | H | 30/33 | 0-16 | 0-30/33 |
| P87C51RA2 | 512B | – | 8K | – | 4 | √ | √ | √ | √ | – | – | – | – | 32 | 7(2)/4 | √ | 12-clk | 6-clk | H | 30/33 | 0-16 | 0-30/33 |

## ORDERING INFORMATION

| PHILIPS (EXCEPT NORTH AMERICA) PART ORDER NUMBER PART MARKING | MEMORY | | TEMPERATURE RANGE (°C) AND PACKAGE | VOLTAGE RANGE | DWG # |
|---|---|---|---|---|---|
| | OTP | RAM | | | |
| P87C51RA2BA | 8 KB | 512B | 0 to +70, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RA2FA | 8 KB | 512B | –40 to +85, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RA2BBD | 8 KB | 512B | 0 to +70, LQFP | 2.7 to 5.5 V | SOT389-1 |
| P87C51RB2BA | 16 KB | 512B | 0 to +70, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RB2FA | 16 KB | 512B | –40 to +85, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RB2BBD | 16 KB | 512B | 0 to +70, LQFP | 2.7 to 5.5 V | SOT389-1 |
| P87C51RB2BN | 16 KB | 512B | 0 to +70, DIP40 | 2.7 to 5.5 V | SOT129-1 |
| P87C51RB2FN | 16 KB | 512B | –40 to +85, DIP40 | 2.7 to 5.5 V | SOT129-1 |
| P87C51RC2BA | 32 KB | 512B | 0 to +70, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RC2FA | 32 KB | 512B | –40 to +85, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RC2BBD | 32 KB | 512B | 0 to +70, LQFP | 2.7 to 5.5 V | SOT389-1 |
| P87C51RC2BN | 32 KB | 512B | 0 to +70, DIP40 | 2.7 to 5.5 V | SOT129-1 |
| P87C51RC2FN | 32 KB | 512B | –40 to +85, DIP40 | 2.7 to 5.5 V | SOT129-1 |
| P87C51RD2BA | 64 KB | 1 KB | 0 to +70, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RD2FA | 64 KB | 1 KB | –40 to +85, PLCC | 2.7 to 5.5 V | SOT187-2 |
| P87C51RD2BBD | 64 KB | 1 KB | 0 to +70, LQFP | 2.7 to 5.5 V | SOT389-1 |
| P87C51RD2FBD | 64 KB | 1 KB | –40 to +85, LQFP | 2.7 to 5.5 V | SOT389-1 |
| P87C51RD2BN | 64 KB | 1 KB | 0 to +70, DIP40 | 2.7 to 5.5 V | SOT129-1 |

## SPECIAL FUNCTION REGISTERS

| SYMBOL | DESCRIPTION | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB | | | | | | | LSB | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ACC* | Accumulator | E0H | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | 00H |
| AUXR# | Auxiliary | 8EH | – | – | – | – | – | – | EXTRAM | AO | xxxxxx00B |
| AUXR1# | Auxiliary 1 | A2H | – | – | – | – | GF2 | 0 | – | DPS | xxxxxxx0B |
| B* | B register | F0H | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 00H |
| CCAP0H# | Module 0 Capture High | FAH | | | | | | | | | xxxxxxxxB |
| CCAP1H# | Module 1 Capture High | FBH | | | | | | | | | xxxxxxxxB |
| CCAP2H# | Module 2 Capture High | FCH | | | | | | | | | xxxxxxxxB |
| CCAP3H# | Module 3 Capture High | FDH | | | | | | | | | xxxxxxxxB |
| CCAP4H# | Module 4 Capture High | FEH | | | | | | | | | xxxxxxxxB |
| CCAP0L# | Module 0 Capture Low | EAH | | | | | | | | | xxxxxxxxB |
| CCAP1L# | Module 1 Capture Low | EBH | | | | | | | | | xxxxxxxxB |
| CCAP2L# | Module 2 Capture Low | ECH | | | | | | | | | xxxxxxxxB |
| CCAP3L# | Module 3 Capture Low | EDH | | | | | | | | | xxxxxxxxB |
| CCAP4L# | Module 4 Capture Low | EEH | | | | | | | | | xxxxxxxxB |
| CCAPM0# | Module 0 Mode | DAH | – | ECOM | CAPP | CAPN | MAT | TOG | PWM | ECCF | x0000000B |
| CCAPM1# | Module 1 Mode | DBH | – | ECOM | CAPP | CAPN | MAT | TOG | PWM | ECCF | x0000000B |
| CCAPM2# | Module 2 Mode | DCH | – | ECOM | CAPP | CAPN | MAT | TOG | PWM | ECCF | x0000000B |
| CCAPM3# | Module 3 Mode | DDH | – | ECOM | CAPP | CAPN | MAT | TOG | PWM | ECCF | x0000000B |
| CCAPM4# | Module 4 Mode | DEH | – | ECOM | CAPP | CAPN | MAT | TOG | PWM | ECCF | x0000000B |
| | | | DF | DE | DD | DC | DB | DA | D9 | D8 | |
| CCON*# | PCA Counter Control | D8H | CF | CR | – | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 | 00x00000B |
| CH# | PCA Counter High | F9H | | | | | | | | | 00H |
| CKCON# | Clock control | 8FH | – | – | – | – | – | – | – | X2 | x0000000B |
| CL# | PCA Counter Low | E9H | | | | | | | | | 00H |
| CMOD# | PCA Counter Mode | D9H | CIDL | WDTE | – | – | – | CPS1 | CPS0 | ECF | 00xxx000B |
| DPTR: | Data Pointer (2 bytes) | | | | | | | | | | |
| DPH | Data Pointer High | 83H | | | | | | | | | 00H |
| DPL | Data Pointer Low | 82H | | | | | | | | | 00H |
| | | | AF | AE | AD | AC | AB | AA | A9 | A8 | |
| IE* | Interrupt Enable 0 | A8H | EA | EC | ET2 | ES | ET1 | EX1 | ET0 | EX0 | 00H |
| | | | BF | BE | BD | BC | BB | BA | B9 | B8 | |
| IP* | Interrupt Priority | B8H | – | PPC | PT2 | PS | PT1 | PX1 | PT0 | PX0 | x0000000B |
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| IPH# | Interrupt Priority High | B7H | – | PPCH | PT2H | PSH | PT1H | PX1H | PT0H | PX0H | x0000000B |
| | | | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | |
| P0* | Port 0 | 80H | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FFH |
| | | | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | |
| P1* | Port 1 | 90H | CEX4 | CEX3 | CEX2 | CEX1 | CEX0 | ECI | T2EX | T2 | FFH |
| | | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| P2* | Port 2 | A0H | AD15 | AD14 | AD13 | AD12 | AD11 | AD10 | AD9 | AD8 | FFH |
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| P3* | Port 3 | B0H | $\overline{RD}$ | $\overline{WR}$ | T1 | T0 | $\overline{INT1}$ | $\overline{INT0}$ | TxD | RxD | FFH |
| | | | | | | | | | | | |
| PCON#[1] | Power Control | 87H | SMOD1 | SMOD0 | – | POF | GF1 | GF0 | PD | IDL | 00xxx000B |

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.
1. Reset value depends on reset source.

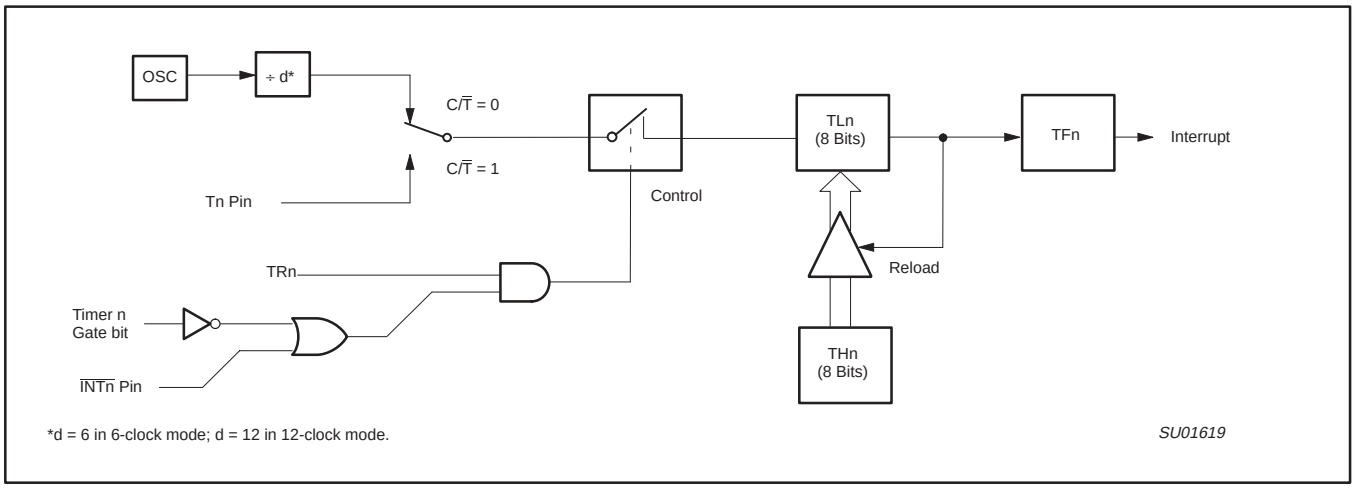


**Figure 5. Timer/Counter 0/1 Mode 2: 8-Bit Auto-Reload**

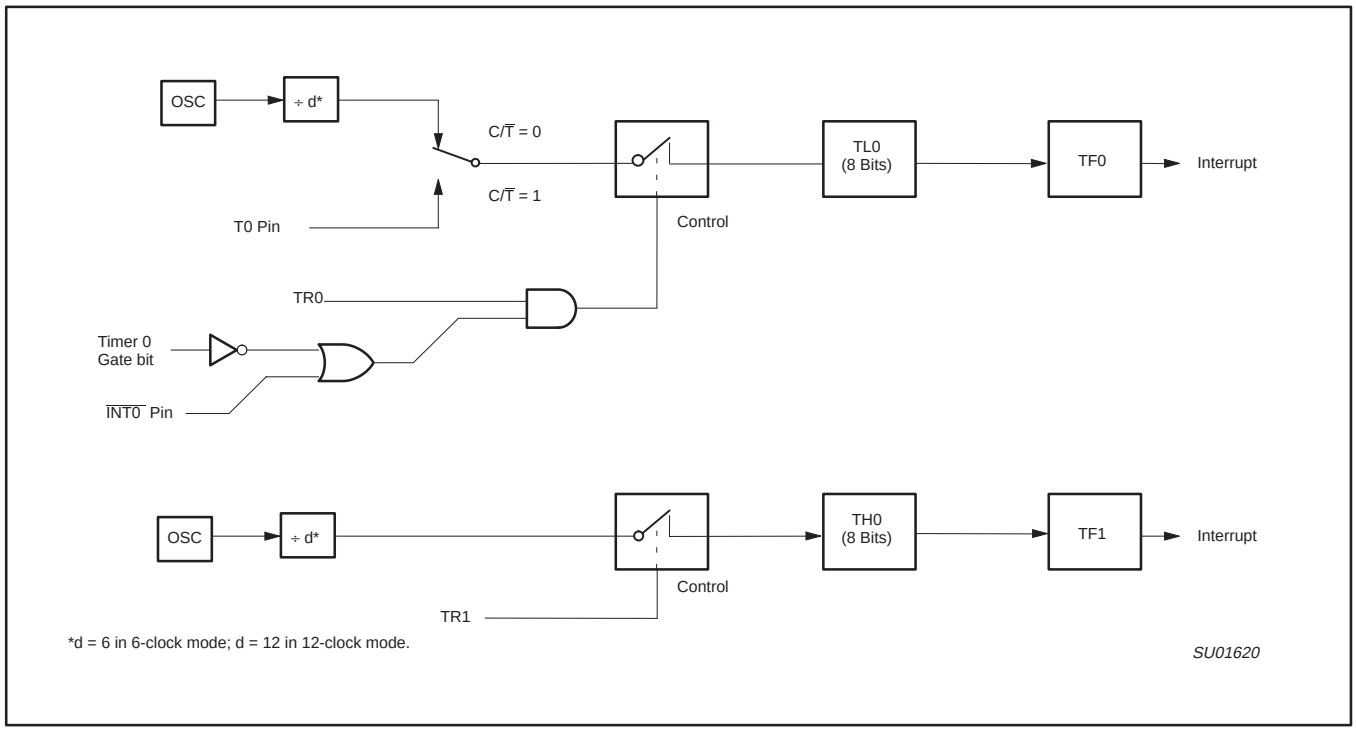


**Figure 6. Timer/Counter 0 Mode 3: Two 8-Bit Counters**

## TIMER 2 OPERATION

### Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/$\overline{T}$2 in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

### Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2 in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/6 pulses (osc/12 in 12-clock mode).).

### Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter [C/$\overline{T}$2 in T2CON]) then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

(MSB) (LSB)

| TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T}$2 | CP/$\overline{RL}$2 |
|---|---|---|---|---|---|---|---|

| Symbol | Position | Name and Significance |
|---|---|---|
| TF2 | T2CON.7 | Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1. |
| EXF2 | T2CON.6 | Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1). |
| RCLK | T2CON.5 | Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock. |
| TCLK | T2CON.4 | Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock. |
| EXEN2 | T2CON.3 | Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX. |
| TR2 | T2CON.2 | Start/stop control for Timer 2. A logic 1 starts the timer. |
| C/$\overline{T}$2 | T2CON.1 | Timer or counter select. (Timer 2)<br>0 = Internal timer (OSC/6 in 6-clock mode or OSC/12 in 12-clock mode)<br>1 = External event counter (falling edge triggered). |
| CP/$\overline{RL}$2 | T2CON.0 | Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow. |

*SU01251*

**Figure 1. Timer/Counter 2 (T2CON) Control Register**

## FULL-DUPLEX ENHANCED UART

### Standard UART operation

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

**Mode 0:** Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency in 12-clock mode or 1/6 the oscillator frequency in 6-clock mode.

**Mode 1:** 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

**Mode 2:** 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in 12-clock mode or 1/16 or 1/32 the oscillator frequency in 6-clock mode.

**Mode 3:** 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

**Multiprocessor Communications**

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

**Serial Port Control Register**

The serial port control and status register is the Special Function Register SCON, shown in Figure 7. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

**Baud Rates**

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12 (12-clock mode) or / 6 (6-clock mode). The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), and the port pins in 12-clock mode, the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency. In 6-clock mode, the baud rate is 1/32 or 1/16 the oscillator frequency, respectively.

Mode 2 Baud Rate =

$$\frac{2^{SMOD}}{n} \times (\text{Oscillator Frequency})$$

Where:

n = 64 in 12-clock mode, 32 in 6-clock mode

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

**Using Timer 1 to Generate Baud Rates**

When Timer 1 is used as the baud rate generator (T2CON.RCLK = 0, T2CON.TCLK = 0), the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate =

$$\frac{2^{SMOD}}{n} \times (\text{Timer 1 Overflow Rate})$$

Where:

n = 32 in 12-clock mode, 16 in 6-clock mode

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =

$$\frac{2^{SMOD}}{n} \times \frac{\text{Oscillator Frequency}}{12 \times [256-(TH1)]}$$

Where:

n = 32 in 12-clock mode, 16 in 6-clock mode

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Figure 8 lists various commonly used baud rates and how they can be obtained from Timer 1.

shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

**More About Mode 1**

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 80C51 the baud rate is determined by the Timer 1 or Timer 2 overflow rate.

Figure 10 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.:

1. R1 = 0, and
2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

**More About Modes 2 and 3**

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 (12-clock mode) or 1/16 or 1/32 the oscillator frequency (6-clock mode) the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1 or Timer 2.

Figures 11 and 12 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SUBF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R-D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1. RI = 0, and
2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

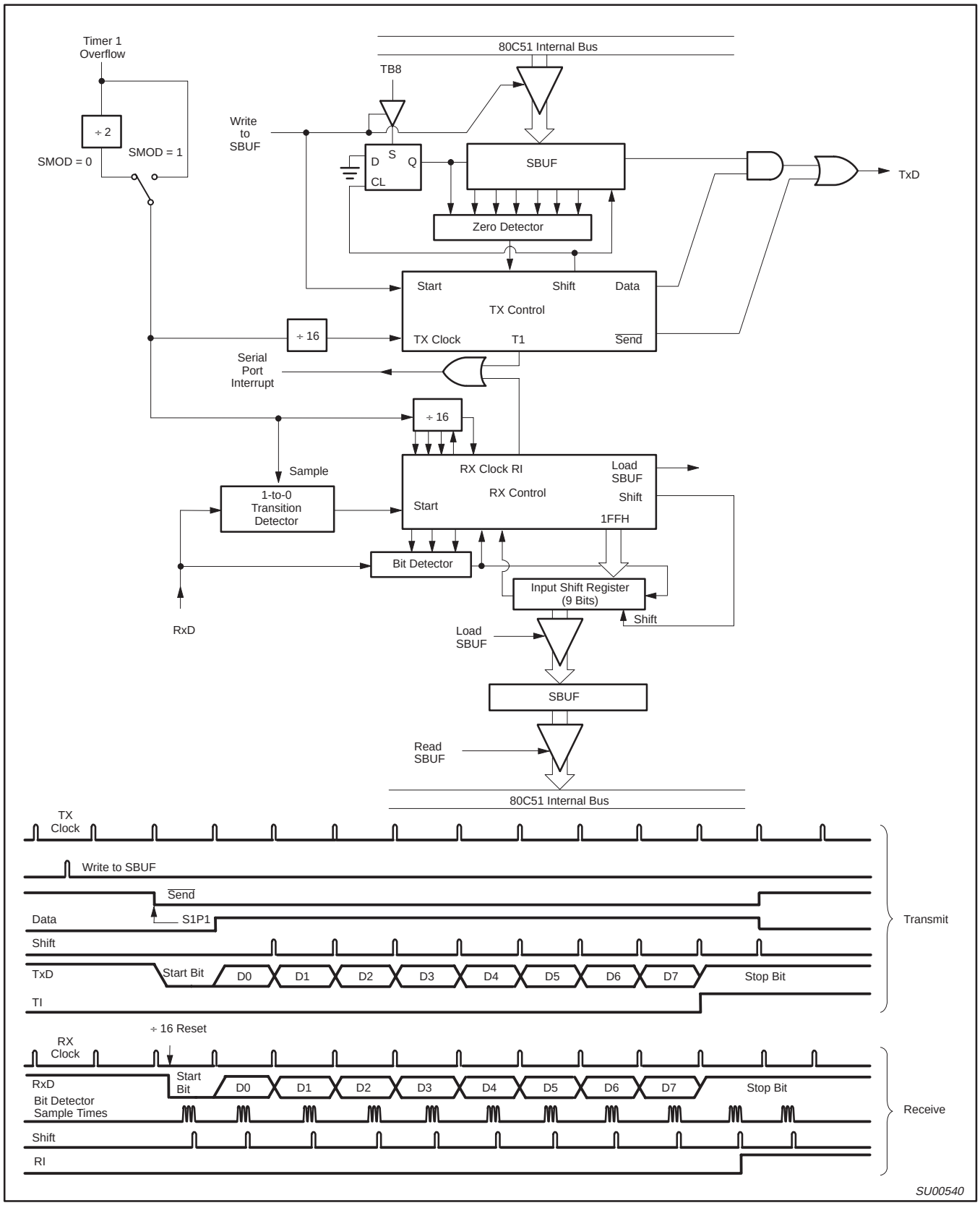


**Figure 10. Serial Port Mode 1**

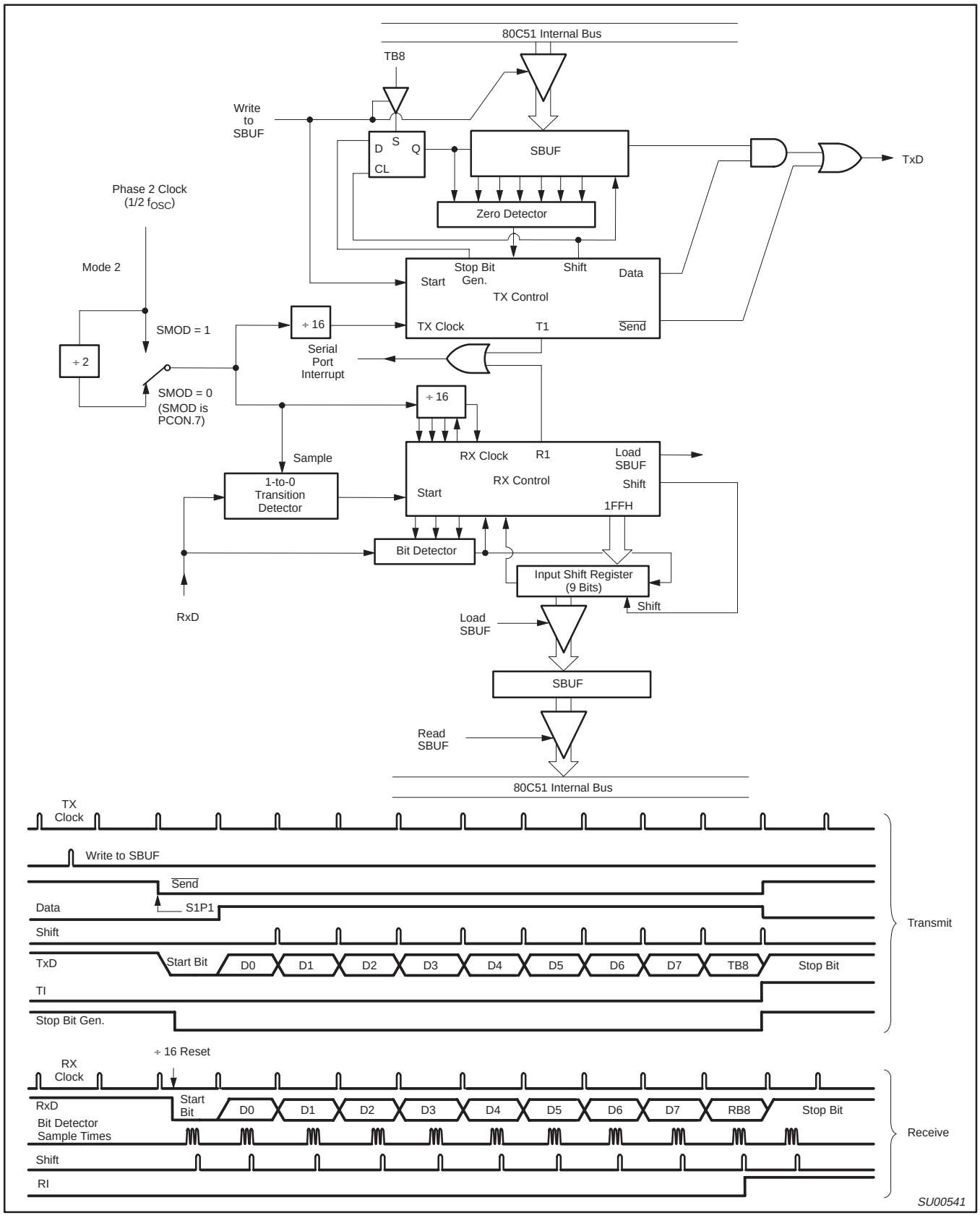


**Figure 11. Serial Port Mode 2**

## Interrupt Priority Structure

The P87C51RA2/RB2/RC2/RD2 has a 7 source four-level interrupt structure (see Table 7).

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. (See Figures 15, 16, and 17.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 17.

The function of the IPH SFR, when combined with the IP SFR, determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

| PRIORITY BITS | | INTERRUPT PRIORITY LEVEL |
|---|---|---|
| IPH.x | IP.x | |
| 0 | 0 | Level 0 (lowest priority) |
| 0 | 1 | Level 1 |
| 1 | 0 | Level 2 |
| 1 | 1 | Level 3 (highest priority) |

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

### Table 7. Interrupt Table

| SOURCE | POLLING PRIORITY | REQUEST BITS | HARDWARE CLEAR? | VECTOR ADDRESS |
|---|---|---|---|---|
| X0 | 1 | IE0 | N (L)[1] Y (T)[2] | 03H |
| T0 | 2 | TP0 | Y | 0BH |
| X1 | 3 | IE1 | N (L) Y (T) | 13H |
| T1 | 4 | TF1 | Y | 1BH |
| PCA | 5 | CF, CCFn n = 0–4 | N | 33H |
| SP | 6 | RI, TI | N | 23H |
| T2 | 7 | TF2, EXF2 | N | 2BH |

**NOTES:**
1. L = Level activated
2. T = Transition activated

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IE (0A8H)** | EA | EC | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IE.7 | EA | Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit. |
| IE.6 | EC | PCA interrupt enable bit |
| IE.5 | ET2 | Timer 2 interrupt enable bit. |
| IE.4 | ES | Serial Port interrupt enable bit. |
| IE.3 | ET1 | Timer 1 interrupt enable bit. |
| IE.2 | EX1 | External interrupt 1 enable bit. |
| IE.1 | ET0 | Timer 0 interrupt enable bit. |
| IE.0 | EX0 | External interrupt 0 enable bit. |

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**Figure 15. IE Registers**

## Expanded Data RAM Addressing

The P87C51RA2/RB2/RC2/RD2 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes expanded RAM (ERAM) (768 bytes for the RD2).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256/768-bytes expanded RAM (ERAM, 00H – 1FFH/2FFH) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared, see Figure 32.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

MOV 0A0H,#data

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 bytes of data RAM.

For example:

MOV @R0,acc

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The ERAM can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 256/768 bytes of external data memory in the P87C51RA2/RB2/RC2/RD2.

With EXTRAM = 0, the ERAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ERAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is output during external addressing. For example, with EXTRAM = 0,

MOVX @R0,acc

where R0 contains 0A0H, accesses the ERAM at address 0A0H rather than external memory. An access to external data memory locations higher than the ERAM will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 33.

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high-order eight address bits (the contents of DPH) while Port 0 multiplexes the low-order eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the ERAM.

**AUXR** Address = 8EH — Reset Value = xxxx xx00B

Not Bit Addressable

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | **EXTRAM** | **AO** |
| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| **AO** | Disable/Enable ALE |
| | **AO** **Operating Mode** |
| | 0 ALE is emitted at a constant rate of $^1/_6$ the oscillator frequency (12-clock mode; $^1/_3$ $f_{OSC}$ in 6-clock mode). |
| | 1 ALE is active only during off-chip memory access. |
| **EXTRAM** | Internal/External RAM access using MOVX @Ri/@DPTR |
| | **EXTRAM** **Operating Mode** |
| | 0 Internal ERAM access using MOVX @Ri/@DPTR |
| | 1 External data memory access. |
| — | Not implemented, reserved for future use*. |

**NOTE:**
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

*SU01613*

**Figure 32. AUXR: Auxiliary Register**

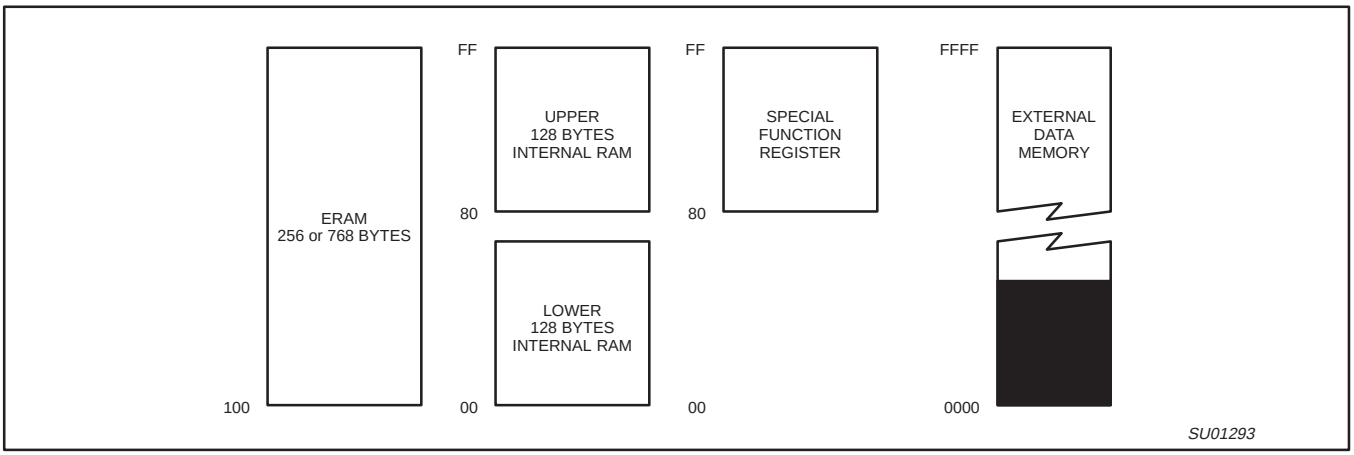


**Figure 33. Internal and External Data Memory Address Space with EXTRAM = 0**

## HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT FOR P87C51RA2/RB2/RC2/RD2)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, the user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When the WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When the WDT overflows, it will drive an output reset HIGH pulse at the RST-pin (see the note below).

### Using the WDT

To enable the WDT, the user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When the WDT overflows, it will generate an output RESET pulse at the reset pin (see note below). The RESET pulse duration is $98 \times T_{OSC}$ (6-clock mode; 196 in 12-clock mode), where $T_{OSC} = 1/f_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

## ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

| PARAMETER | RATING | UNIT |
|---|---|---|
| Operating temperature under bias | 0 to +70 or –40 to +85 | °C |
| Storage temperature range | –65 to +150 | °C |
| Voltage on $\overline{EA}/V_{PP}$ pin to $V_{SS}$ | 0 to +13.0 | V |
| Voltage on any other pin to $V_{SS}$[4] | –0.5 to +6.0 | V |
| Maximum $I_{OL}$ per I/O pin | 15 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.5 | W |

**NOTES:**
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.
4. Transient voltage only.

## AC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C or –40°C to +85°C

| SYMBOL | FIGURE | PARAMETER | OPERATING MODE | POWER SUPPLY VOLTAGE | CLOCK FREQUENCY RANGE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| $1/t_{CLCL}$ | 38 | Oscillator frequency | 6-clock | 5 V ± 10% | 0 | 30 | MHz |
| | | | 6-clock | 2.7 V to 5.5 V | 0 | 16 | MHz |
| | | | 12-clock | 5 V ± 10% | 0 | 33 | MHz |
| | | | 12-clock | 2.7 V to 5.5 V | 0 | 16 | MHz |

## DC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0 °C to +70 °C or –40 °C to +85 °C; **$V_{CC}$ = 2.7 V to 5.5 V**; $V_{SS}$ = 0 V (16 MHz max. CPU clock)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| $V_{IL}$ | Input low voltage[11] | 4.0 V < $V_{CC}$ < 5.5 V | –0.5 | | 0.2 $V_{CC}$–0.1 | V |
| | | 2.7 V < $V_{CC}$ < 4.0 V | –0.5 | | 0.7 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$) | | 0.2 $V_{CC}$+0.9 | | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST[11] | | 0.7 $V_{CC}$ | | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output low voltage, ports 1, 2, [8] | $V_{CC}$ = 2.7 V; $I_{OL}$ = 1.6 mA[2] | – | | 0.4 | V |
| $V_{OL1}$ | Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7] | $V_{CC}$ = 2.7 V; $I_{OL}$ = 3.2 mA[2] | – | | 0.4 | V |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3 [3] | $V_{CC}$ = 2.7 V; $I_{OH}$ = –20 μA | $V_{CC}$ – 0.7 | | – | V |
| | | $V_{CC}$ = 4.5 V; $I_{OH}$ = –30 μA | $V_{CC}$ – 0.7 | | – | V |
| $V_{OH1}$ | Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3] | $V_{CC}$ = 2.7 V; $I_{OH}$ = –3.2 mA | $V_{CC}$ – 0.7 | | – | V |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3 | $V_{IN}$ = 0.4 V | –1 | | –50 | μA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3[6] | $V_{IN}$ = 2.0 V; See note 4 | – | | –650 | μA |
| $I_{LI}$ | Input leakage current, port 0 | 0.45 < $V_{IN}$ < $V_{CC}$ – 0.3 | – | | ±10 | μA |
| $I_{CC}$ | Power supply current (see Figure 41 and Source Code): | | | | | |
| | Active mode @ 16 MHz | | | | | μA |
| | Idle mode @ 16 MHz | | | | | μA |
| | Power-down mode or clock stopped (see Figure 37 for conditions) [12] | $T_{amb}$ = 0 °C to 70 °C | | 2 | 30 | μA |
| | | $T_{amb}$ = –40 °C to +85 °C | | 3 | 50 | μA |
| $V_{RAM}$ | RAM keep-alive voltage | | 1.2 | | | V |
| $R_{RST}$ | Internal reset pull-down resistor | | 40 | | 225 | kΩ |
| $C_{IO}$ | Pin capacitance[10] (except $\overline{EA}$) | | – | | 15 | pF |

**NOTES:**

1. Typical ratings are not guaranteed. Values listed are based on tests conducted on limited number of samples at room temperature.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. $I_{OL}$ can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $V_{CC}$–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2 V.
5. See Figures 43 through 46 for $I_{CC}$ test conditions and Figure 41 for $I_{CC}$ vs. Frequency
   12-clock mode characteristics:
   Active mode (operating): $I_{CC}$ = 1.0 mA + 1.1 mA × FREQ.[MHz]
   Active mode (reset): $I_{CC}$ = 7.0 mA + 0.6 mA × FREQ.[MHz]
   Idle mode: $I_{CC}$ = 1.0 mA + 0.22 mA × FREQ.[MHz]
6. This value applies to $T_{amb}$ = 0 °C to +70 °C. For $T_{amb}$ = –40 °C to +85 °C, $I_{TL}$ = –750 μA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 15 mA (*NOTE: This is 85 °C specification.)
   Maximum $I_{OL}$ per 8-bit port: 26 mA
   Maximum total $I_{OL}$ for all outputs: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to $V_{OH1}$, except when ALE is off then $V_{OH}$ is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{EA}$ is 25 pF).
11. To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the $\overline{INT0}$ and $\overline{INT1}$ pins. Previous devices provided only an inherent 5 ns of glitch rejection.
12. Power down mode for 3 V range: Commercial Temperature Range – typ: 0.5 μA, max. 20 μA; Industrial Temperature Range – typ. 1.0 μA, max. 30 μA;

## DC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0 °C to +70 °C or –40 °C to +85 °C; **$V_{CC}$ = 5 V ±10%**; $V_{SS}$ = 0 V (30/33 MHz max. CPU clock)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| $V_{IL}$ | Input low voltage[11] | 4.5 V < $V_{CC}$ < 5.5 V | –0.5 | | 0.2 $V_{CC}$–0.1 | V |
| $V_{IH}$ | Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$) | | 0.2 $V_{CC}$+0.9 | | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST[11] | | 0.7 $V_{CC}$ | | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output low voltage, ports 1, 2, 3 [8] | $V_{CC}$ = 4.5 V; $I_{OL}$ = 1.6 mA[2] | – | | 0.4 | V |
| $V_{OL1}$ | Output low voltage, port 0, ALE, $\overline{PSEN}$ [7, 8] | $V_{CC}$ = 4.5 V; $I_{OL}$ = 3.2 mA[2] | – | | 0.4 | V |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3 [3] | $V_{CC}$ = 4.5 V; $I_{OH}$ = –30 µA | $V_{CC}$ – 0.7 | | – | V |
| $V_{OH1}$ | Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3] | $V_{CC}$ = 4.5 V; $I_{OH}$ = –3.2 mA | $V_{CC}$ – 0.7 | | – | V |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3 | $V_{IN}$ = 0.4 V | –1 | | –50 | µA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3[6] | $V_{IN}$ = 2.0 V; See note 4 | – | | –650 | µA |
| $I_{LI}$ | Input leakage current, port 0 | 0.45 < $V_{IN}$ < $V_{CC}$ – 0.3 | – | | ±10 | µA |
| $I_{CC}$ | Power supply current | | | | | |
| | Active mode (see Note 5) | | | | | |
| | Idle mode (see Note 5) | | | | | |
| | Power-down mode or clock stopped (see Figure 46 for conditions) | $T_{amb}$ = 0 °C to 70 °C | | 2 | 30 | µA |
| | | $T_{amb}$ = –40 °C to +85 °C | | 3 | 50 | µA |
| $V_{RAM}$ | RAM keep-alive voltage | | 1.2 | | | V |
| $R_{RST}$ | Internal reset pull-down resistor | | 40 | | 225 | kΩ |
| $C_{IO}$ | Pin capacitance[10] (except $\overline{EA}$) | | – | | 15 | pF |

**NOTES:**

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. $I_{OL}$ can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $V_{CC}$–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2 V.
5. See Figures 43 through 46 for $I_{CC}$ test conditions and Figure 41 for $I_{CC}$ vs. Frequency.
   12-clock mode characteristics:
   Active mode (operating): $I_{CC}$ = 1.0 mA + 1.1 mA × FREQ.[MHz]
   Active mode (reset): $I_{CC}$ = 7.0 mA + 0.6 mA × FREQ.[MHz]
   Idle mode: $I_{CC}$ = 1.0 mA + 0.22 mA × FREQ.[MHz]
6. This value applies to $T_{amb}$ = 0°C to +70°C. For $T_{amb}$ = –40°C to +85°C, $I_{TL}$ = –750 µA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 15 mA (*NOTE: This is 85 °C specification.)
   Maximum $I_{OL}$ per 8-bit port: 26 mA
   Maximum total $I_{OL}$ for all outputs: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to $V_{OH1}$, except when ALE is off then $V_{OH}$ is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{EA}$ is 25 pF).
11. To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the $\overline{INT0}$ and $\overline{INT1}$ pins. Previous devices provided only an inherent 5 ns of glitch rejection.

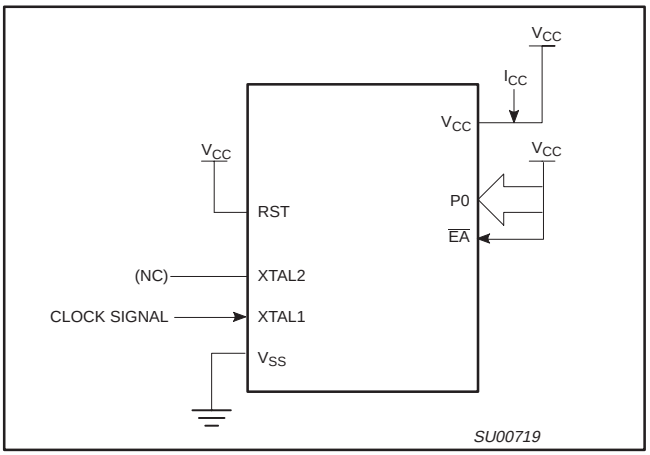


**Figure 43. $I_{CC}$ Test Condition, Active Mode**
**All other pins are disconnected**

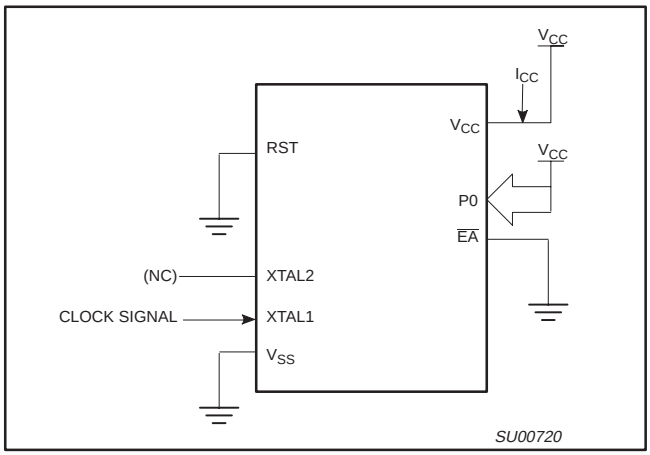


**Figure 44. $I_{CC}$ Test Condition, Idle Mode**
**All other pins are disconnected**

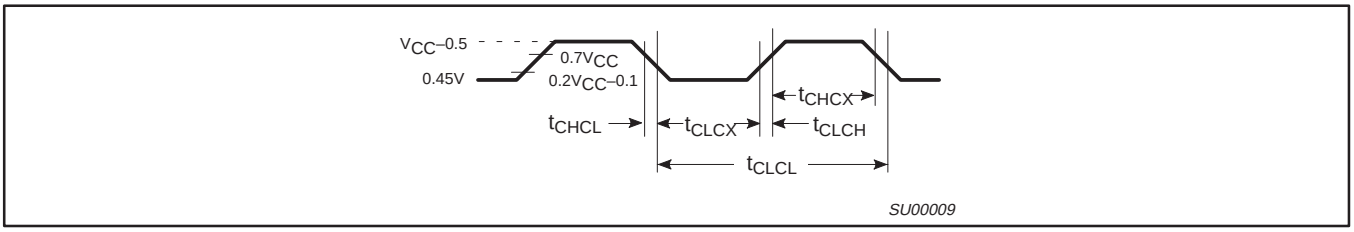


**Figure 45. Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes**
**$t_{CLCH} = t_{CHCL} = 5ns$**

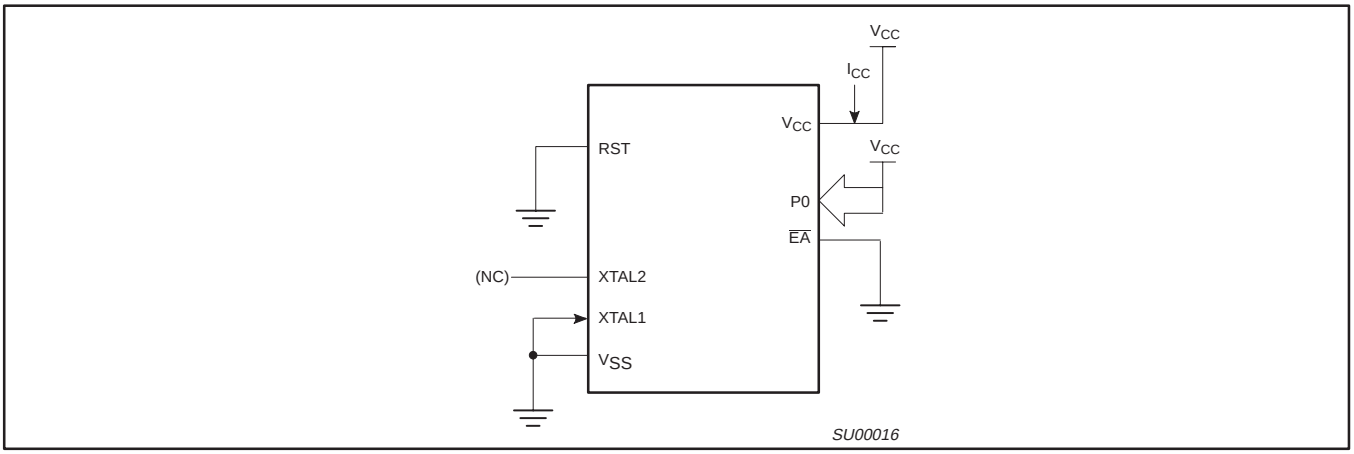


**Figure 46. $I_{CC}$ Test Condition, Power Down Mode**
**All other pins are disconnected. $V_{CC}$ = 2 V to 5.5 V**

## EPROM CHARACTERISTICS

All these devices can be programmed by using a modified Improved Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for $V_{PP}$ (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The family contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as being manufactured by Philips.

Table 8 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 47 and 48. Figure 49 shows the circuit configuration for normal program memory verification.

### Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 47. Note that the device is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 47. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 8 are held at the 'Program Code Data' levels indicated in Table 8. The ALE/$\overline{PROG}$ is pulsed low 5 times as shown in Figure 48.

To program the encryption table, repeat the 5 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 5 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bits can still be programmed.

Note that the $\overline{EA}$/$V_{PP}$ pin must not be allowed to go above the maximum specified $V_{PP}$ level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The $V_{PP}$ source should be well regulated and free of glitches and overshoot.

**Program Verification**

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 49. The other pins are held at the 'Verify Code Data' levels indicated in Table 8. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

**Reading the Signature Bytes**

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips
(031H) = CAH indicates 87C51RA2
CBH indicates 87C51RB2
CCH indicates 87C51RC2
CDH indicates 87C51RD2
(060H) = NA

### Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 8, and which satisfies the timing specifications, is suitable.

### Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 9) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

### Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

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## ROM CODE SUBMISSION FOR 16K ROM DEVICES (87C51RB2)

When submitting ROM code for the 16K ROM devices, the following must be specified:

1. 16 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

| ADDRESS | CONTENT | BIT(S) | COMMENT |
|---|---|---|---|
| 0000H to 3FFFH | DATA | 7:0 | User ROM Data |
| 4000H to 403FH | KEY | 7:0 | ROM Encryption Key<br>FFH = no encryption |
| 4040H | SEC | 0 | ROM Security Bit 1<br>0 = enable security<br>1 = disable security |
| 4040H | SEC | 1 | ROM Security Bit 2<br>0 = enable security<br>1 = disable security |

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

## ROM CODE SUBMISSION FOR 32K ROM DEVICES (87C51RC2)

When submitting ROM code for the 32K ROM devices, the following must be specified:

1. 32 kbyte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

| ADDRESS | CONTENT | BIT(S) | COMMENT |
|---|---|---|---|
| 0000H to 7FFFH | DATA | 7:0 | User ROM Data |
| 8000H to 803FH | KEY | 7:0 | ROM Encryption Key<br>FFH = no encryption |
| 8040H | SEC | 0 | ROM Security Bit 1<br>0 = enable security<br>1 = disable security |
| 8040H | SEC | 1 | ROM Security Bit 2<br>0 = enable security<br>1 = disable security |

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

## REVISION HISTORY

| Rev | Date | Description |
|---|---|---|
| _3 | 20030124 | **Product data (9397 750 10994); ECN 853-2391 29335 dated 07 Jan 2003.**<br>Modifications:<br>● Updated ordering information table. |
| _2 | 20021028 | **Product data (9397 750 10393); ECN 853-2391 29117 dated 28 Oct 2002.** |

## Data sheet status

| Level | Data sheet status [1] | Product status [2] [3] | Definitions |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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## Contact information

For additional information please visit
**http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
**sales.addresses@www.semiconductors.philips.com**.



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