



Welcome to E-XFL.COM

### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205rbt6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### Table 3. STM32F207xx features and peripheral counts (continued)

	Peripherals	STM32F207Vx	STM32F207Zx	STM32F207lx							
	SPI/(I <sup>2</sup> S)		3/(2) <sup>(2)</sup>								
	I <sup>2</sup> C		3								
Comm. interfaces	USART UART		4 2								
	USB OTG FS		Yes								
	USB OTG HS		Yes								
Comm. interfaces	CAN	2									
Camera interface			Yes								
GPIOs		82	82 114 14								
SDIO			Yes								
12-bit ADC		3									
Number of channe	els	16	24	24							
12-bit DAC Number of channe	els		Yes 2								
Maximum CPU fre	equency		120 MHz								
Operating voltage			1.8 V to 3.6 V <sup>(3)</sup>								
Operating temper			Ambient temperatures: -40 to +85 °C	/–40 to +105 °C							
Operating tempera	alures		Junction temperature: -40 to ·	+ 125 °C							
Package		LQFP100	LQFP144	LQFP176/ UFBGA176							

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.

2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.

On devices in WLCSP64+2 package, if IRROFF is set to V<sub>DD</sub>, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see Section 3.16).

### 3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

### 3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the three AHB buses, the highspeed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

The devices embed a dedicate PLL (PLLI2S) which allow to achieve audio class performance. In this case, the  $I^2S$  master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

### 3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

### 3.14 Power supply schemes

V<sub>DD</sub> = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V<sub>DD</sub> pins. On devices in WLCSP64+2 package, if IRROFF is set to V<sub>DD</sub>, the supply voltage can drop to 1.7 V when the device operates



There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes

The LP regulator mode is configured by software when entering Stop mode.

• Power-down is used in Standby mode.

The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on  $V_{CAP_1}$  and  $V_{CAP_2}$  pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

### 3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V<sub>CAP 1</sub> and V<sub>CAP 2</sub> pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

### Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V<sub>DD</sub> and IRROFF pin to V<sub>SS</sub>. On UFBGA176 package, only REGOFF must be connected to V<sub>DD</sub> (IRROFF not available). In this mode,  $V_{DD}/V_{DDA}$  minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V<sub>CAP 1</sub> and V<sub>CAP 2</sub> pins, in addition to V<sub>DD</sub>.





Figure 6. Regulator OFF/internal reset ON

The following conditions must be respected:

- V<sub>DD</sub> should always be higher than V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to avoid current injection between power domains.
- If the time for  $V_{CAP_1}$  and  $V_{CAP_2}$  to reach 1.08 V is faster than the time for  $V_{DD}$  to reach 1.8 V, then PA0 should be kept low to cover both conditions: until  $V_{CAP_1}$  and  $V_{CAP_2}$  reach 1.08 V and until  $V_{DD}$  reaches 1.8 V (see *Figure 8*).
- Otherwise, If the time for V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to reach 1.08 V is slower than the time for V<sub>DD</sub> to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).
- If V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> go below 1.08 V and V<sub>DD</sub> is higher than 1.8 V, then a reset must be asserted on PA0 pin.

### **Regulator OFF/internal reset OFF**

On WLCSP64+2 package, this mode activated by connecting REGOFF to V<sub>SS</sub> and IRROFF to V<sub>DD</sub>. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external  $V_{DD}$  supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The  $V_{DD}$  specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.



		Pi	ns								
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Note	Alternate functions	Additional functions
22	H5	31	42	52	P3	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6
23	J7	32	43	53	R3	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
24	H4	33	44	54	N5	PC4	I/O	FT	(4)	ETH_RMII_RXD0, ETH_MII_RXD0, EVENTOUT	ADC12_IN14
25	G3	34	45	55	P5	PC5	I/O	FT	(4)	ETH_RMII_RXD1, ETH_MII_RXD1, EVENTOUT	ADC12_IN15
26	J6	35	46	56	R5	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
27	J5	36	47	57	R4	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
28	J4	37	48	58	M6	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	49	59	R6	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	50	60	P6	PF12	I/O	FT	-	FSMC_A6, EVENTOUT	-
-	-	-	51	61	M8	V <sub>SS</sub>	S		-	-	-
-	-	-	52	62	N8	V <sub>DD</sub>	S		-	-	-
-	-	-	53	63	N6	PF13	I/O	FT	-	FSMC_A7, EVENTOUT	-
-	-	-	54	64	R7	PF14	1/0	FT	-	FSMC_A8, EVENTOUT	-
-	-	-	55	65	P7	PF15	1/0	FT	-	+SMC_A9, EVENTOUT	-
-	-	-	56	66	N7	PG0	1/0	FT	-	FSMC_A10, EVENTOUT	-
-	-	-	57	67	M7	PG1	I/O	ŀΤ	-	FSMC_A11, EVENTOUT	-



		Pi	ins								
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-
-	-	-	-	85	M12	PH8	I/O	FT	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	86	M13	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	-
-	-	-	-	87	L13	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	88	L12	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	89	K12	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	90	H12	V <sub>SS</sub>	S	-	-	-	-
-	-	-	-	91	J12	V <sub>DD</sub>	S	-	-	-	-
33	J1	51	73	92	P12	PB12	I/O	FT	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-
34	H2	52	74	93	P13	PB13	I/O	FT	-	SPI2_SCK, I2S2_SCK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_ VBUS
35	H1	53	75	94	R14	PB14	I/O	FT	-	SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM USART3_RTS, TIM8_CH2N, EVENTOUT	-
36	G1	54	76	95	R15	PB15	I/O	FT	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, RTC_50Hz, EVENTOUT	-
-	-	55	77	96	P15	PD8	I/O	FT	-	FSMC_D13, USART3_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)



		Pi	ns								
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Note	Alternate functions	Additional functions
38	F2	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	-
39	F3	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	D1	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	E2	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	E3	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	D3	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	D2	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4,OTG_FS_DM, EVENTOUT	-
45	C1	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	В2	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	C2	73	106	125	F13	V <sub>CAP_2</sub>	S	-	-	-	-
-	B1	74	107	126	F12	V <sub>SS</sub>	S	-	-	-	
48	A8	75	108	127	G13	V <sub>DD</sub>	S	-	-	-	-
-	-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

Table 8. STM32F20x	pin and ball definition	s (continued)
		0 (0011011000)



S
22
ĸ

# DocID15818 Rev 13

		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		
	Port	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ЕТН	FSMC/SDIO/ OTG_HS	DCMI	AF014	AF15
	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_ STP	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ULPI_ DIR	ETH_MII_TXD2	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI	-	-	-	-	OTG_HS_ULPI_ NXT	ETH _MII_TX_CLK	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD1 ETH_RMII_RXD1	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
Port C	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	I2S3_CKIN	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK I2S3_SCK	USART3_TX	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	-	EVENTOUT
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14- OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15- OSC32_OU T	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 10. Alternate function mapping (continued)

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f<sub>HCLK</sub> frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz and 3 wait states from 90 to 120 MHz).
- When the peripherals are enabled HCLK is the system clock, f<sub>PCLK1</sub> = f<sub>HCLK</sub>/4, and f<sub>PCLK2</sub> = f<sub>HCLK</sub>/2, except is explicitly mentioned.
- The maximum values are obtained for  $V_{DD}$  = 3.6 V and maximum ambient temperature (T<sub>A</sub>), and the typical values for T<sub>A</sub>= 25 °C and V<sub>DD</sub> = 3.3 V unless otherwise specified.

# Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM <sup>(1)</sup>

Symbol	Baramatar	Conditions		Тур	Ма	Unit	
Symbol	Farameter	Conditions	HCLK	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	Unit
			120 MHz	49	63	72	
			90 MHz	38	51	61	
	Supply current		60 MHz	26	39	49	
		(3)	30 MHz	14	27	37	
		External clock <sup>(3)</sup> , all peripherals enabled <sup>(4)</sup>	25 MHz	11	24	34	
			16 MHz <sup>(5)</sup>	8	21	30	
			8 MHz	5	17	27	mA
			4 MHz	3	16	26	
1			2 MHz	2	15	25	
<b>I</b> DD	in Run mode		120 MHz	21	34	44	
			90 MHz	17	30	40	
			60 MHz	12	25	35	
		(3)	30 MHz	7	20	30	
		External clock <sup>(3)</sup> , all peripherals disabled	25 MHz	5	18	28	
		P -	16 MHz <sup>(5)</sup>	4.0	17.0	27.0	-
			8 MHz	2.5	15.5	25.5	
			4 MHz	2.0	14.7	24.8	
			2 MHz	1.6	14.5	24.6	

1. Code and data processing running from SRAM1 using boot pins.

2. Guaranteed by characterization, tested in production at  $V_{DD}$  max and  $f_{HCLK}$  max with peripherals enabled.

3. External clock is 4 MHz and PLL is on when  $f_{HCLK}$  > 25 MHz.

4. When the ADC is on (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5. In this case HCLK = system clock/2.





Figure 23. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals ON

Figure 24. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals OFF







Figure 34. ACC<sub>HSI</sub> versus temperature

### Low-speed internal (LSI) RC oscillator

Table 33. LS	l oscillator	characteristics	(1)
--------------	--------------	-----------------	-----

Symbol	Parameter	Min	Тур	Мах	Unit
f <sub>LSI</sub> <sup>(2)</sup>	Frequency	17	32	47	kHz
t <sub>su(LSI)</sub> <sup>(3)</sup>	LSI oscillator startup time	-	15	40	μs
I <sub>DD(LSI)</sub> <sup>(3)</sup>	LSI oscillator power consumption	-	0.4	0.6	μA

1.  $V_{DD}$  = 3 V,  $T_A$  = -40 to 105 °C unless otherwise specified.

2. Guaranteed by characterization results, not tested in production.

3. Guaranteed by design, not tested in production.





Figure 35. ACC<sub>LSI</sub> versus temperature

### 6.3.10 PLL characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under temperature and  $V_{DD}$  supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
f <sub>PLL_IN</sub>	PLL input clock <sup>(1)</sup>	-	0.95 <sup>(2)</sup>	1	2.10 <sup>(2)</sup>	MHz
f <sub>PLL_OUT</sub>	PLL multiplier output clock	-	24	-	120	MHz
f <sub>PLL48_OUT</sub>	48 MHz PLL multiplier output clock	-	-	-	48	MHz
f <sub>VCO_OUT</sub>	PLL VCO output	-	192	-	432	MHz
t <sub>LOCK</sub>	PLL lock time	VCO freq = 192 MHz	75	-	200	116
		VCO freq = 432 MHz	100	-	300	μο

Table 34. Main PLL characteristics



Symbol	Paran	Parameter		Min	Тур	Мах	Unit
Weak pull-up R <sub>PU</sub> equivalent	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50		
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	kO
R <sub>PD</sub>	Weak pull-down equivalent resister <sup>(7)</sup>	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	K22
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
C <sub>IO</sub> <sup>(8)</sup>	I/O pin capacitance		-	-	5	-	pF

Table 46. I/O static characteristics (continued)

1. Guaranteed by design, not tested in production.

2. Guaranteed by tests in production.

3. With a minimum of 200 mV.

- 4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to Table 45: I/O current injection susceptibility
- To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to Table 45: I/O current injection susceptibility
- 6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
- 7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
- 8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.



being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in Section 6.3.16 does not affect the ADC accuracy.





- Example of an actual transfer curve 1.
- 2. Ideal transfer curve
- End point correlation line. 3.
- $E_T$  = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves. EO = Offset Error: deviation between the first actual transition and the first ideal one. 4. EG = Gain Error: deviation between the last ideal transition and the last actual one. ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.

EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.





 $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{parasitic}$  value downgrades conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced. 2.



Refer to Table 66 for the values of  $\mathsf{R}_{AIN},\,\mathsf{R}_{ADC}$  and  $\mathsf{C}_{ADC}$ 1.

Symbol	Parameter	Min	Max	Unit
t <sub>d(CLKL-NWEL)</sub>	FSMC_CLK low to FSMC_NWE low	-	1	ns
t <sub>d(CLKL-NWEH)</sub>	FSMC_CLK low to FSMC_NWE high	0	-	ns
t <sub>d(CLKL-ADIV)</sub>	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
t <sub>d(CLKL-DATA</sub> )	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	2	ns
t <sub>d(CLKL-NBLH)</sub>	FSMC_CLK low to FSMC_NBL high	0.5	-	ns

Table 77. Synchronous multiplexed PSRAM write timings<sup>(1)(2)</sup> (continued)

1. C<sub>L</sub> = 30 pF.

2. Guaranteed by characterization results, not tested in production.



### Figure 63. Synchronous non-multiplexed NOR/PSRAM read timings

Table 78. Synchronous non-multiplexed NOR/PSRAM read	timinas <sup>(1)(2)</sup>
Table 70. Oynemonous non-maniplexed North Ortam read	unnings

Symbol	Parameter	Min	Max	Unit
t <sub>w(CLK)</sub>	FSMC_CLK period	2T <sub>HCLK</sub>	-	ns
t <sub>d(CLKL-NExL)</sub>	FSMC_CLK low to FSMC_NEx low (x=02)	-	0	ns
t <sub>d(CLKL-NExH)</sub>	FSMC_CLK low to FSMC_NEx high (x= 02)	1	-	ns
t <sub>d(CLKL-NADVL)</sub>	FSMC_CLK low to FSMC_NADV low	-	2.5	ns





Figure 65. PC Card/CompactFlash controller waveforms for common memory read access

1. FSMC\_NCE4\_2 remains high (inactive during 8-bit access.







### 7.7 Thermal characteristics

The maximum chip-junction temperature,  $T_{\rm J}$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J max = T_A max + (P_D max x \Theta_{JA})$$

Where:

- T<sub>A</sub> max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in ° C/W,
- P<sub>D</sub> max is the sum of P<sub>INT</sub> max and P<sub>I/O</sub> max (P<sub>D</sub> max = P<sub>INT</sub> max + P<sub>I/O</sub>max),
- P<sub>INT</sub> max is the product of I<sub>DD</sub> and V<sub>DD</sub>, expressed in Watts. This is the maximum chip internal power.

P<sub>I/O</sub> max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I}/\mathsf{O}} \max = \Sigma \; (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma ((\mathsf{V}_{\mathsf{DD}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$ 

taking into account the actual V\_{OL} / I\_{OL} and V\_{OH} / I\_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
	Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	
Θ <sub>JA</sub>	Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch	51	°C ///
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	C/W
	<b>Thermal resistance junction-ambient</b> LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Table 95	. Package	thermal	characteristics
----------	-----------	---------	-----------------

### **Reference document**

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.



## 8 Part numbering

Table 96. Ordering informati	on scheme					
Example:	STM32 F	205	R	Е	те	6 Vxxx
Device family						
STM22 - ADM based 32 bit microcentroller						
STNISZ – ARIVI-based Sz-bit microcontroller						
Product type						
F = general-purpose						
Device subfamily						
205 = STM32F20x, connectivity						
207= STM32F20x, connectivity, camera interface,						
Ethernet						
Pin count						
R = 64 pins or 66 pins <sup>(1)</sup>						
V = 100 pins						
Z = 144 pins						
I = 176 pins						
Flash memory size						
B = 128 Kbytes of Flash memory						
C = 256 Kbytes of Flash memory						
E = 512 Kbytes of Flash memory						
F = 768 Kbytes of Flash memory						
G = 1024 Kbytes of Flash memory						
Package						
T = LQFP						
H = UFBGA						
Y = WLCSP						
Temperature range						
6 = Industrial temperature range, -40 to 85 °C.						
7 = Industrial temperature range, -40 to 105 °C.						
Software option						
Internal code or Blank						
Options						

xxx = programmed parts TR = tape and reel

1. The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



Date	Revision	Changes
29-Oct-2012	10 (continued)	Replaced t <sub>d(CLKL-NOEL)</sub> by t <sub>d(CLKH-NOEL)</sub> in Table 76: Synchronous multiplexed NOR/PSRAM read timings, Table 78: Synchronous non- multiplexed NOR/PSRAM read timings, Figure 61: Synchronous multiplexed NOR/PSRAM read timings and Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings. Added Figure 87: LQFP176 recommended footprint. Added Note 2 below Figure 86: Regulator OFF/internal reset ON. Updated device subfamily in Table 96: Ordering information scheme. Remove reference to note 2 for USB IOTG FS in Table 101: Main applications versus package for STM32F2xxx microcontrollers.

Table 97.	Document revisio	on history	(continued)
	Document revisit		(continued)



Date	Revision	Changes
Date	Revision   11	Changes   In the whole document, updated notes related to WLCSP64+2 usage with IRROFF set to V <sub>DD</sub> . Updated Section 3.16.1: Regulator ON and Section 3.16: Power supply supervisor, Section 3.16.1: Regulator ON and Section 3.16: Regulator OFF. Added Section 3.16.3: Regulator ON/OFF and internal reset ON/OFF availability. Added note related to WLCSP64+2 package.   Restructured RTC features and added reference clock detection in Section 3.17: Real-time clock (RTC), backup SRAM and backup registers.   Added note indicating the package view below Figure 10: STM32F20X LQFP64 pinout, Figure 12: STM32F20X LQFP100 pinout, Figure 13: STM32F20x LQFP144 pinout, and Figure 14: STM32F20x LQFP176 pinout.   Added Table 7: Legend/abbreviations used in the pinout table. Table 8: STM32F20x pin and ball definitions: content reformatted; removed indexes on V <sub>SS</sub> and V <sub>DD</sub> ; updated PA4, PA5, PA6, PC4, BOOT0; replaced DCMI_12 by DCMI_D12, TIM8_CHIN by TIM8_CH1N, ETH_MII_RX_D0 by ETH_MII_RXD0, ETH_MII_RXD0, ETH_MII_RXD0, ETH_MII_RXD1, and RMII_CRS_DV by ETH_RMII_RXD1, ETH_RMII_RXD1, and RMII_CRS_DV by ETH_RMII_RXD1, ETH_RMII_RXD1, and RMII_CRS_DV by ETH_RMII_RXD1, added EVENTOUT as AF15 alternated function for PC13, PC14, PC15, PH0, PH1, and PI8.   Updated figure 17: Pin loading conditions and Figure 18: Pin input voltage.   Added V <sub>IN</sub> in Table 14: General operating conditions.   Removed note applying to V <sub>POR/PER</sub> minimum value in Table 19: Embedded reset and power control block characteristics.   Updated Power control block characteristics.   Updated conditions in Table 41: EMS characteristics.

