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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205ret6

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

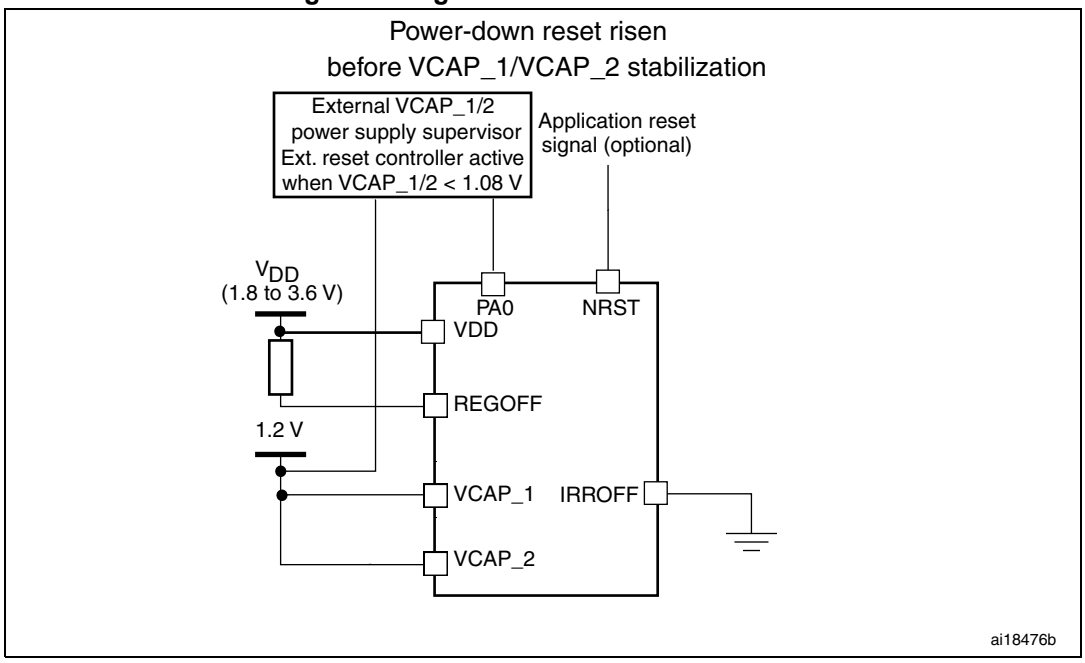
The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

Figure 6. Regulator OFF/internal reset ON



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 8*).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD}. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	56	78	97	P14	PD9	I/O	FT	-	FSMC_D14, USART3_RX, EVENTOUT	-
-	-	57	79	98	N15	PD10	I/O	FT	-	FSMC_D15, USART3_CK, EVENTOUT	-
-	-	58	80	99	N14	PD11	I/O	FT	-	FSMC_A16,USART3_CTS, EVENTOUT	-
-	-	59	81	100	N13	PD12	I/O	FT	-	FSMC_A17,TIM4_CH1, USART3_RTS, EVENTOUT	-
-	-	60	82	101	M15	PD13	I/O	FT	-	FSMC_A18,TIM4_CH2, EVENTOUT	-
-	-	-	83	102	-	V_{SS}	S	-	-	-	-
-	-	-	84	103	J13	V_{DD}	S	-	-	-	-
-	-	61	85	104	M14	PD14	I/O	FT	-	FSMC_D0,TIM4_CH3, EVENTOUT	-
-	-	62	86	105	L14	PD15	I/O	FT	-	FSMC_D1,TIM4_CH4, EVENTOUT	-
-	-	-	87	106	L15	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	88	107	K15	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	89	108	K14	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	90	109	K13	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	91	110	J15	PG6	I/O	FT	-	FSMC_INT2, EVENTOUT	-
-	-	-	92	111	J14	PG7	I/O	FT	-	FSMC_INT3 ,USART6_CK, EVENTOUT	-
-	-	-	93	112	H14	PG8	I/O	FT	-	USART6_RTS, ETH_PPS_OUT, EVENTOUT	-
-	-	-	94	113	G12	V_{SS}	S	-	-	-	-
-	-	-	95	114	H13	V_{DD}	S	-	-	-	-
37	G2	63	96	115	H15	PC6	I/O	FT	-	I2S2_MCK, TIM8_CH1, SDIO_D6, USART6_TX, DCMI_D0, TIM3_CH1, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
38	F2	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	-
39	F3	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	D1	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	E2	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	E3	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	D3	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	D2	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4,OTG_FS_DM, EVENTOUT	-
45	C1	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	B2	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	C2	73	106	125	F13	V_{CAP_2}	S	-	-	-	-
-	B1	74	107	126	F12	V_{SS}	S	-	-	-	-
48	A8	75	108	127	G13	V_{DD}	S	-	-	-	-
-	-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port H	PH0 - OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1 - OSC_OUT	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-				-	-	-	-	-	-	ETH _MII_CRS	-	-	-	EVENTOUT
	PH3	-	-				-	-	-	-	-	-	ETH _MII_COL	-	-	-	EVENTOUT
	PH4	-	-			I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-			I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH6	-	-			I2C2_SMBA	-	-	-	-	TIM12_CH1	-	ETH _MII_RXD2	-	-	-	EVENTOUT
	PH7	-	-			I2C3_SCL	-	-	-	-	-	-	ETH _MII_RXD3	-	-	-	EVENTOUT
	PH8	-	-			I2C3_SDA	-	-	-	-	-	-	-	-	DCMI_HSYNC	-	EVENTOUT
	PH9	-	-			I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	-	DCMI_D0	-	EVENTOUT
	PH10	-	-	TIM5_CH1			-	-	-	-	-	-	-	-	DCMI_D1	-	EVENTOUT
	PH11	-	-	TIM5_CH2			-	-	-	-	-	-	-	-	DCMI_D2	-	EVENTOUT
	PH12	-	-	TIM5_CH3			-	-	-	-	-	-	-	-	DCMI_D3	-	EVENTOUT
	PH13	-	-		TIM8_CH1N		-	-	-	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-		TIM8_CH2N		-	-	-	-	-	-	-	-	DCMI_D4	-	EVENTOUT
	PH15	-	-		TIM8_CH3N		-	-	-	-	-	-	-	-	DCMI_D11	-	EVENTOUT
Port I	PI0	-	-	TIM5_CH4			SPI2_NSS I2S2_WS	-	-	-	-	-	-	-	DCMI_D13	-	EVENTOUT
	PI1	-	-				SPI2_SCK I2S2_SCK	-	-	-	-	-	-	-	DCMI_D8	-	EVENTOUT
	PI2	-	-		TIM8_CH4		SPI2_MISO	-	-	-	-	-	-	-	DCMI_D9	-	EVENTOUT
	PI3	-	-		TIM8_ETR		SPI2_MOSI I2S2_SD	-	-	-	-	-	-	-	DCMI_D10	-	EVENTOUT
	PI4	-	-		TIM8_BKIN		-	-	-	-	-	-	-	-	DCMI_D5	-	EVENTOUT
	PI5	-	-		TIM8_CH1		-	-	-	-	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	PI6	-	-		TIM8_CH2		-	-	-	-	-	-	-	-	DCMI_D6	-	EVENTOUT
	PI7	-	-		TIM8_CH3		-	-	-	-	-	-	-	-	DCMI_D7	-	EVENTOUT
	PI8	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-				-	-	-	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-				-	-	-	-	-	-	ETH _MII_RX_ER	-	-	-	EVENTOUT
	PI11	-	-				-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 17*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 18*.

Figure 17. Pin loading conditions

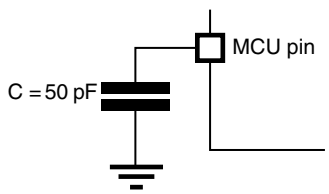
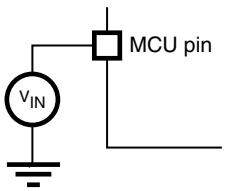
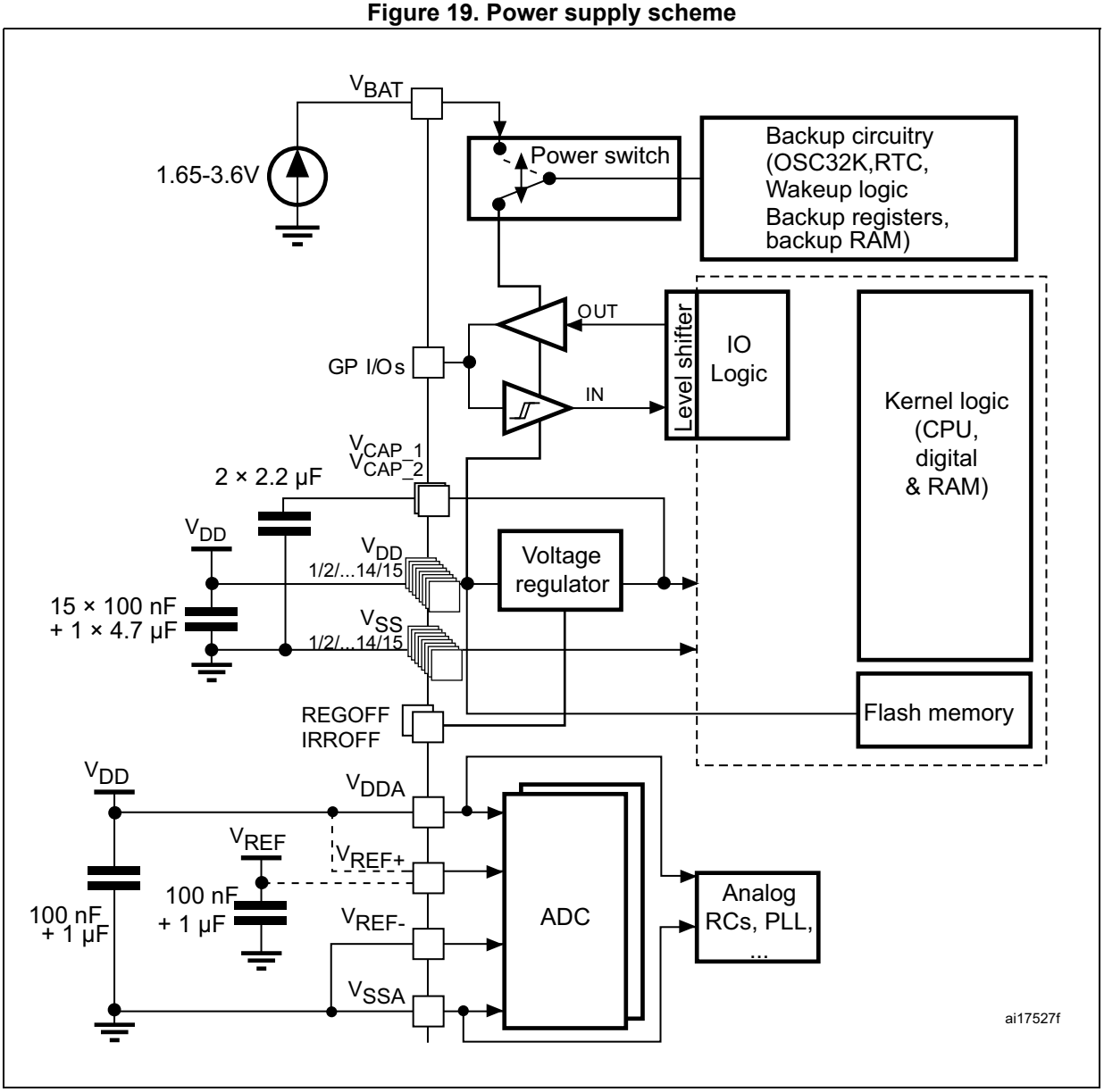


Figure 18. Pin input voltage



6.1.6 Power supply scheme

Figure 19. Power supply scheme



1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect REGOFF and IRROFF pins, refer to *Section 3.16: Voltage regulator*.
3. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
4. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB, to ensure good device operation. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect device operation.

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled(3)	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz(4)	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock(2), all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz(4)	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Table 22. Typical and maximum current consumption in Sleep mode

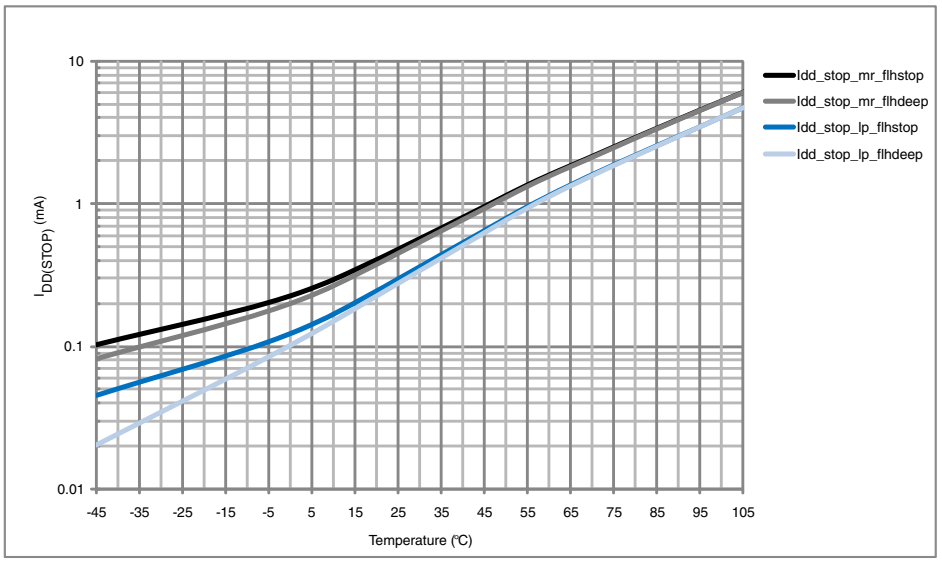
Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	120 MHz	38	51	61	mA
			90 MHz	30	43	53	
			60 MHz	20	33	43	
			30 MHz	11	25	35	
			25 MHz	8	21	31	
			16 MHz	6	19	29	
			8 MHz	3.6	17.0	27.0	
			4 MHz	2.4	15.4	25.3	
			2 MHz	1.9	14.9	24.7	
		External clock(2), all peripherals disabled	120 MHz	8	21	31	
			90 MHz	7	20	30	
			60 MHz	5	18	28	
			30 MHz	3.5	16.0	26.0	
			25 MHz	2.5	16.0	25.0	
			16 MHz	2.1	15.1	25.0	
			8 MHz	1.7	15.0	25.0	
			4 MHz	1.5	14.6	24.6	
			2 MHz	1.4	14.2	24.3	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Figure 29. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Table 26. Peripheral current consumption (continued)

Peripheral[1]		Typical consumption at 25 °C	Unit
APB2	SDIO	0.69	mA
	TIM1	1.06	
	TIM8	1.03	
	TIM9	0.58	
	TIM10	0.37	
	TIM11	0.39	
	ADC1[4]	2.13	
	ADC2[4]	2.04	
	ADC3[4]	2.12	
	SPI1	1.20	
	USART1	0.38	
	USART6	0.37	

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC_CR register.
3. EN2 bit is set in DAC_CR register.
4. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

6.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Unit
$t_{WUSLEEP}$[2]	Wakeup from Sleep mode	-	1	-	µs
t_{WUSTOP}[2]	Wakeup from Stop mode (regulator in Run mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}$[2][3]	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

Table 39. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 40. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-2	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 48. I/O AC characteristics(1) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-3	6	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100(3)	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	120(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. The maximum frequency is defined in *Figure 39*.
3. For maximum frequencies above 50 MHz and V_{DD} above 2.4 V, the compensation cell should be used.

Figure 44. SPI timing diagram - master mode

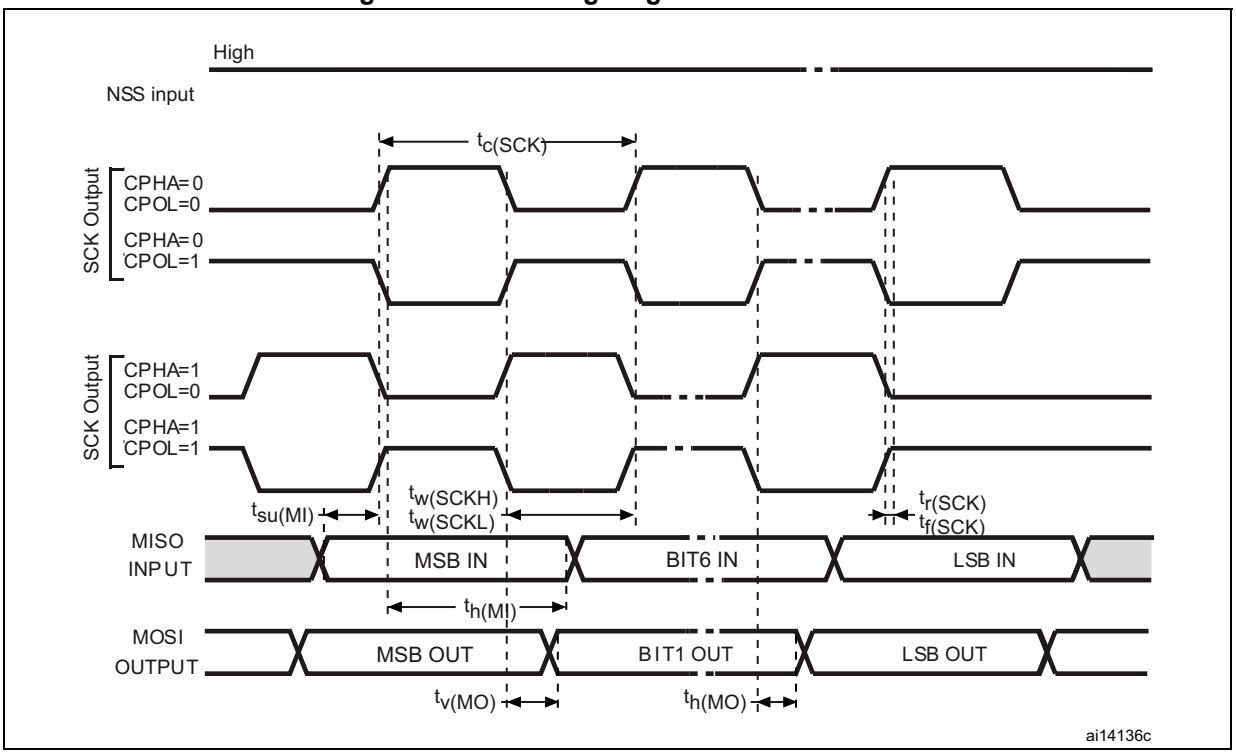


Table 83. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}$- 1	$4T_{HCLK}$+ 3	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$+ 2	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}$- 2	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

6.3.26 Camera interface (DCMI) timing specifications

Table 84. DCMI characteristics

Symbol	Parameter	Conditions	Min	Max
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	DCMI_PIXCLK= 48 MHz	-	0.4

6.3.27 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 85* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 75. SDIO high-speed mode

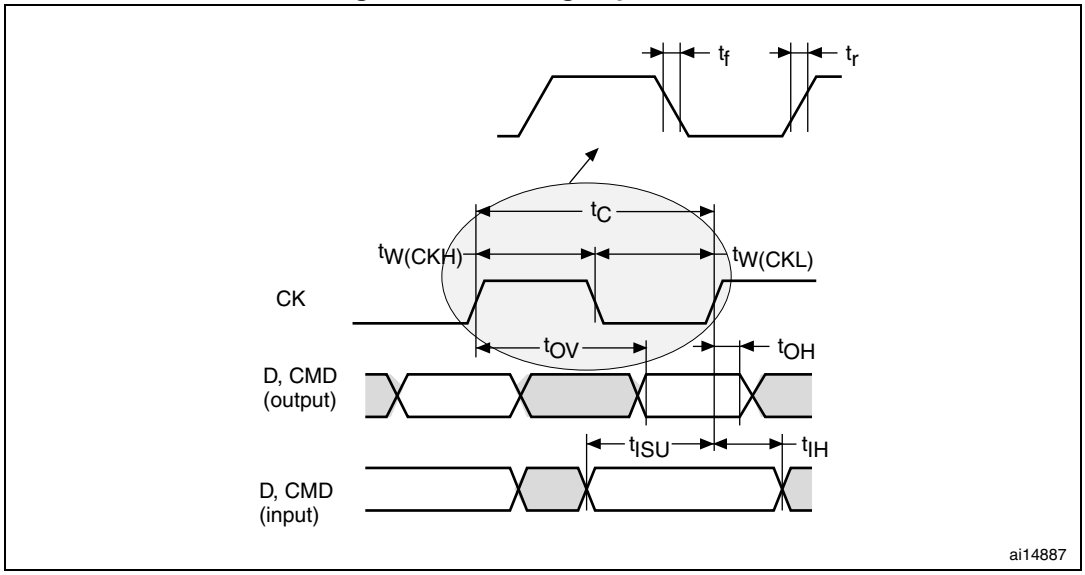


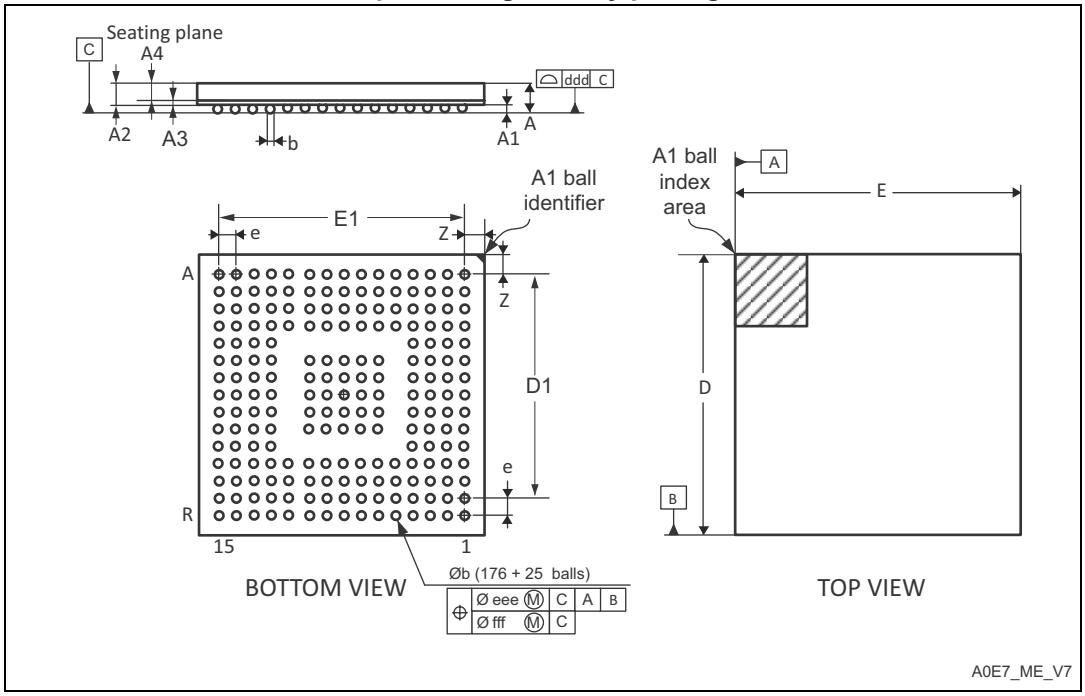
Table 92. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data (continued)

Symbol	Dimensions					
	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
HD	25.900	-	26.100	1.0197	-	1.0276
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L[2]	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

7.6 UFBGA176+25 package information

Figure 89. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 97. Document revision history (continued)

Date	Revision	Changes
14-Jun-2011	7	Added SDIO in *Table 2: STM32F205xx features and peripheral counts*. Updated V_{IN} for 5V tolerant pins in *Table 11: Voltage characteristics*. Updated jitter parameters description in *Table 34: Main PLL characteristics*. Remove jitter values for system clock in *Table 35: PLLI2S (audio PLL) characteristics*. Updated *Table 42: EMI characteristics*. Update *Note 2* in *Table 52: I2C characteristics*. Updated Avg_Slope typical value and T_{S_temp} minimum value in *Table 69: Temperature sensor characteristics*. Updated T_{S_vbat} minimum value in *Table 70: VBAT monitoring characteristics*. Updated $T_{S\_vrefint}$ minimum value in *Table 71: Embedded internal reference voltage*. Added Software option in *Section 8: Part numbering*. In *Table 101: Main applications versus package for STM32F2xxx microcontrollers*, renamed USB1 and USB2, USB OTG FS and USB OTG HS, respectively; and removed USB OTG FS and camera interface for 64-pin package; added USB OTG HS on 64-pin package; added *Note 1* and *Note 2*.
20-Dec-2011	8	Updated SDIO register addresses in *Figure 16: Memory map*. Updated *Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package*, *Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package*, *Figure 1: Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package*, and added *Figure 4: Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package*. Updated *Section 3.3: Memory protection unit*. Updated *Section 3.6: Embedded SRAM*. Updated *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)* to remove external FS OTG PHY support. In *Table 8: STM32F20x pin and ball definitions*: changed SPI2_MCK and SPI3_MCK to I2S2_MCK and I2S3_MCK, respectively. Added ETH _RMII_TX_EN atlternate function to PG11. Added EVENTOUT in the list of alternate functions for I/O pin/balls. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. In *Table 10: Alternate function mapping*: changed I2S3_SCK to I2S3_MCK for PC7/AF6, added FSMC_NCE3 for PG9, FSMC_NE3 for PG10, and FSMC_NCE2 for PD7. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. Changed I2S3_SCK into I2S3_MCK for PC7/AF6. Updated peripherals corresponding to AF12. Removed CEXT and ESR from *Table 14: General operating conditions*.

Table 97. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	10	Changed minimum supply voltage from 1.65 to 1.8 V. Updated number of AHB buses in *Section 2: Description* and *Section 3.12: Clocks and startup*. Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package. Updated *Note 2* below *Figure 4: STM32F20x block diagram*. Changed System memory to System memory + OTP in *Figure 16: Memory map*. Added *Note 1* below *Table 16: VCAP1/VCAP2 operating conditions*. Updated V_{DDA} and V_{REF+} decouping capacitor in *Figure 19: Power supply scheme* and updated *Note 3*. Changed simplex mode into half-duplex mode in *Section 3.24: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively.Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in *Table 10: Alternate function mapping*. Updated note applying to I_{DD} (external clock and all peripheral disabled) in *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Note 3* below *Table 22: Typical and maximum current consumption in Sleep mode*. Removed f_{HSE_ext} typical value in *Table 28: High-speed external user clock characteristics*. Updated master I2S clock jitter conditions and vlaues in *Table 35: PLLI2S (audio PLL) characteristics*. Updated equations in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in *Table 47: Output voltage characteristics*. Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 49: NRST pin characteristics*. Updated *Table 54: SPI characteristics* and *Table 55: I2S characteristics*. Removed note 1 related to measurement points below *Figure 43: SPI timing diagram - slave mode and CPHA = 1*, *Figure 44: SPI timing diagram - master mode*, and *Figure 45: I2S slave timing diagram (Philips protocol)(1)*. Updated t_{HC} in *Table 61: ULPI timing*. Updated *Figure 49: Ethernet SMI timing diagram*, *Table 63: Dynamics characteristics: Ethernet MAC signals for SMI* and *Table 65: Dynamics characteristics: Ethernet MAC signals for MII*. Update f_{TRIG} in *Table 66: ADC characteristics*. Updated I_{DDA} description in *Table 68: DAC characteristics*. Updated note below *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*.