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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	•
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205rft6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Figure 3. Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package



1. RFU = reserved for future use.





Figure 8. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP-1}/V_{CAP-2} stabilization

1. This figure is valid both whatever the internal reset mode (ON or OFF).



Figure 9. Startup in regulator OFF: fast V_{DD} slope - power-down reset risen before V_{CAP} ₁/ V_{CAP} ₂ stabilization



The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see Section 3.18: Low-power modes).

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or the V_{BAT} pin.

3.18 Low-power modes

The STM32F20x family supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

• Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

3.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

 V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT} , external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When using WLCSP64+2 package, if IRROFF pin is connected to V_{DD} , the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .



USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	х	х	х	х	х	х	1.87	7.5	APB2 (max. 60 MHz)
USART2	х	х	х	х	х	x	1.87	3.75	APB1 (max. 30 MHz)
USART3	x	х	х	х	х	x	1.87	3.75	APB1 (max. 30 MHz)
UART4	x	-	х	-	х	-	1.87	3.75	APB1 (max. 30 MHz)
UART5	x	-	х	-	х	-	3.75	3.75	APB1 (max. 30 MHz)
USART6	x	х	х	х	х	x	3.75	7.5	APB2 (max. 60 MHz)

 Table 6. USART feature comparison

3.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.24 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx interfaces can be served by the DMA controller.

3.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.



3.34 ADCs (analog-to-digital converters)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers TIM1, TIM2, TIM3, TIM4, TIM5 and TIM8 can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.35 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.



		Pi	ns								
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	-	131	159	C7	V _{DD}	S	-	-	-	-
-	-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCMI_D13, EVENTOUT	-
55	A4	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/ TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	В4	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	A5	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	-
58	B5	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL,, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT	-
59	A6	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL ⁽⁶⁾ , DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	B6	94	138	166	D6	BOOT0	Ι	В	-	-	V _{PP}
61	B7	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	A7	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)



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	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13			
	Port	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ЕТН	FSMC/SDIO/ OTG_HS	DCMI	AF014	AF15
	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_ STP	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ULPI_ DIR	ETH_MII_TXD2	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI	-	-	-	-	OTG_HS_ULPI_ NXT	ETH _MII_TX_CLK	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD1 ETH_RMII_RXD1	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
Port C	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	I2S3_CKIN	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK I2S3_SCK	USART3_TX	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	-	EVENTOUT
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14- OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15- OSC32_OU T	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 10. Alternate function mapping (continued)

Symbol	Ratings	Max.	Unit	
I _{VDD}	Total current into V _{DD} power lines (source) ⁽¹⁾	120		
I _{VSS}	I _{VSS} Total current out of V _{SS} ground lines (sink) ⁽¹⁾			
1	Output current sunk by any I/O and control pin	25		
ЧО	Output current source by any I/Os and control pin	25	mA	
(2)	Injected current on five-volt tolerant I/O ⁽³⁾	-5/+0		
INJ(PIN)	Injected current on any other pin ⁽⁴⁾	±5		
$\Sigma I_{\rm INJ(PIN)}^{(4)}$	Total injected current (sum of all I/O and control pins) ⁽⁵⁾	±25		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. Negative injection disturbs the analog performance of the device. See note in Section 6.3.20: 12-bit ADC characteristics.

 Positive injection is not possible on these I/Os. A negative injection is induced by V_{IN}<V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.

4. A positive injection is induced by V_{IN} > V_{DD} while a negative injection is induced by V_{IN} < V_{SS} . $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.

5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13.	Thermal	characteristics
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Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	–65 to +150	°C
TJ	Maximum junction temperature	125	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit
f _{HCLK}	Internal AHB clock frequency	-	0	120	
f _{PCLK1}	Internal APB1 clock frequency	-	0	30	MHz
f _{PCLK2}	Internal APB2 clock frequency	-	0	60	



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{BOR2}	Brownout level 2	Falling edge	2.44	2.50	2.56	V
	threshold	Rising edge	2.53	2.59	2.63	V
M	Brownout level 3	Falling edge	2.75	2.83	2.88	V
VBOR3	threshold	Rising edge	2.85	2.92	2.97	V
V _{BORhyst} ⁽¹⁾	BOR hysteresis	-	-	100	-	mV
T _{RSTTEMPO} ⁽¹⁾⁽²⁾	Reset temporization	-	0.5	1.5	3.0	ms
I _{RUSH} ⁽¹⁾	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E _{RUSH} ⁽¹⁾	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V _{DD} = 1.8 V, T _A = 105 °C, I _{RUSH} = 171 mA for 31 μs	-	-	5.4	μC

 Table 19. Embedded reset and power control block characteristics (continued)

1. Guaranteed by design, not tested in production.

2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 20: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using CoreMark code.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
f _{OSC_IN}	Oscillator frequency	-	4	-	26	MHz	
R _F	Feedback resistor	-	-	200	-	kΩ	
I _{DD}		V _{DD} =3.3 V, ESR= 30 Ω, C _L =5 pF@25 MHz	-	449	-		
		V _{DD} =3.3 V, ESR= 30 Ω, C _L =10 pF@25 MHz	-	532	-	μΑ	
9 _m	Oscillator transconductance	Startup	5	-	-	mA/V	
$t_{\rm SU(HSE}^{(3)}$	Startup time	V _{DD} is stabilized	-	2	-	ms	

 Table 30. HSE 4-26 MHz oscillator characteristics^{(1) (2)}

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by characterization results, not tested in production.

 t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 32*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note:

For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website <u>www.st.com</u>.



Figure 32. Typical application with an 8 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
R _F	Feedback resistor	-	-	18.4	-	MΩ	
I _{DD}	LSE current consumption	-	-	-	1	μA	
9 _m	Oscillator Transconductance	-	2.8	-	-	μA/V	
t _{SU(LSE)} ⁽²⁾	startup time	V _{DD} is stabilized	-	2	-	s	

Table 31. LSE oscillator characteristics ($f_{LSE} = 32.768 \text{ kHz}$)⁽¹⁾

1. Guaranteed by design, not tested in production.

 t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website <u>www.st.com</u>.



Figure 33. Typical application with a 32.768 kHz crystal

6.3.9 Internal clock source characteristics

The parameters given in *Table 32* and *Table 33* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI}	Frequency	-	-	16	-	MHz
100	HSI user-trimming step ⁽²⁾	-	-	-	1	%
	Accuracy of the HSI oscillator	$T_A = -40$ to 105 °C ⁽³⁾	- 8	-	4.5	%
ACCHSI		$T_A = -10$ to 85 °C ⁽³⁾	- 4	-	4	%
		$T_A = 25 \ ^{\circ}C^{(4)}$	– 1	-	1	%
t _{su(HSI)} ⁽²⁾	HSI oscillator startup time	-	-	2.2	4.0	μs
DD(HSI) ⁽²⁾	HSI oscillator power consumption	-	-	60	80	μA

 Table 32. HSI oscillator characteristics ⁽¹⁾

1. V_{DD} = 3.3 V, T_A = -40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

- 3. Guaranteed by characterization results.
- 4. Factory calibrated, parts not soldered.



Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
t _{prog}	Double word programming		-	16	100 ⁽²⁾	μs
t _{ERASE16KB}	Sector (16 KB) erase time	T _A = 0 to +40 °C	-	230	-	
t _{ERASE64KB}	Sector (64 KB) erase time	V _{DD} = 3.3 V	-	490	-	ms
t _{ERASE128KB}	Sector (128 KB) erase time	V _{PP} = 8.5 V	-	875	-	
t _{ME}	Mass erase time		-	6.9	-	S
V _{prog}	Programming voltage	-	2.7	-	3.6	V
V _{PP}	V _{PP} voltage range	-	7	-	9	V
I _{PP}	Minimum current sunk on the $V_{\rm PP}$ pin	-	10	-	-	mA
t _{VPP} ⁽³⁾	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

Table 39.	Flash memor	y programming	with V _F	ъР
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1. Guaranteed by design, not tested in production.

2. The maximum programming time is measured after 100K erase operations.

3. V_{PP} should only be connected during programming/erasing.

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N _{END}	Endurance	$T_A = -40$ to +85 °C (6 suffix versions) $T_A = -40$ to +105 °C (7 suffix versions)	10	kcycles
t _{RET}		1 kcycle ⁽²⁾ at T _A = 85 °C	30	
	Data retention	1 kcycle ⁽²⁾ at T _A = 105 °C	10	Years
		10 kcycles ⁽²⁾ at T _A = 55 °C	20	

Table 40. Flash memory endurance and data retention

1. Guaranteed by characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.





Figure 47. USB OTG FS timings: definition of data signal rise and fall time

Table 58. USB OTG FS electrical characteristics⁽¹⁾

Driver characteristics										
Symbol	Parameter	Conditions	Min	Мах	Unit					
t _r	Rise time ⁽²⁾	C _L = 50 pF	4	20	ns					
t _f	Fall time ⁽²⁾	C _L = 50 pF	4	20	ns					
t _{rfm}	Rise/fall time matching	t _r /t _f	90	110	%					
V _{CRS}	Output signal crossover voltage	-	1.3	2.0	V					

1. Guaranteed by design, not tested in production.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Table 59 shows the USB HS operating voltage.

Table 59. USB HS DC electrical characteristics

Symbol		Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level	V _{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 60. Clock timing parameters

Parameter ⁽¹⁾		Symbol	Min	Nominal	Max	Unit
Frequency (first transition)	8-bit ±10%	F _{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500	ppm	F _{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition) 8-bit ±10%		D _{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D _{STEADY}	49.975	50	50.025	%
Time to reach the steady state duty cycle after the first transiti	frequency and on	T _{STEADY}	-	-	1.4	ms
Clock startup time after the	Peripheral	T _{START_DEV}	-	-	5.6	me
de-assertion of SuspendM	Host	T _{START_HOST}	-	-	-	1115
PHY preparation time after the first transition of the input clock		T _{PREP}	-	-	-	μs

1. Guaranteed by design, not tested in production.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _S ⁽³⁾		12-bit resolution Single ADC	-	-	2	Msps
	Sampling rate (f _{ADC} = 30 MHz)	12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I _{VREF+} ⁽³⁾	ADC V _{REF} DC current consumption in conversion mode	-	-	300	500	μA
I _{VDDA} ⁽³⁾	ADC VDDA DC current consumption in conversion mode	-	-	1.6	1.8	mA

Table 66. ADC characteristics (continued)

 On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see Section 3.16).

2. It is recommended to maintain the voltage difference between V_{REF+} and V_{DDA} below 1.8 V.

3. Guaranteed by characterization results, not tested in production.

4. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .

5. R_{ADC} maximum value is given for V_{DD}=1.8 V, and minimum value for V_{DD}=3.3 V.

6. For external triggers, a delay of 1/f_{PCLK2} must be added to the latency specified in Table 66.

Equation 1: RAIN max formula

$$\mathsf{R}_{\mathsf{AIN}} = \frac{(k - 0.5)}{\mathsf{f}_{\mathsf{ADC}} \times \mathsf{C}_{\mathsf{ADC}} \times \mathsf{In}(2^{\mathsf{N}+2})} - \mathsf{R}_{\mathsf{ADC}}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Symbol	Parameter	Test conditions	Тур	Max ⁽²⁾	Unit
ET	Total unadjusted error		±2	±5	
EO	Offset error	fронка = 60 MHz.	±1.5	±2.5	
EG	Gain error	$f_{ADC} = 30 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$	±1.5	±3	LSB
ED	Differential linearity error	$V_{DDA} = 1.8^{(3)}$ to 3.6 V	±1	±2	
EL	Integral linearity error		±1.5	±3	

Table	67.	ADC	accuracy	(1)
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1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.

2. Guaranteed by characterization results, not tested in production.

 On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see Section 3.16).

Note:

ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion



being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.16 does not affect the ADC accuracy.





- Example of an actual transfer curve 1.
- 2. Ideal transfer curve
- End point correlation line. 3.
- E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves. EO = Offset Error: deviation between the first actual transition and the first ideal one. 4. EG = Gain Error: deviation between the last ideal transition and the last actual one. ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.

EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.





 $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced. 2.



Refer to Table 66 for the values of $\mathsf{R}_{AIN},\,\mathsf{R}_{ADC}$ and C_{ADC} 1.



Figure 58. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 73. Asynchronous	non-multiplexed SRA	M/PSRAM/NO	R write timin	gs ⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FSMC_NE low time	3T _{HCLK}	3T _{HCLK} + 4	ns
t _{v(NWE_NE})	FSMC_NEx low to FSMC_NWE low	T _{HCLK} – 0.5	T _{HCLK} + 0.5	ns
t _{w(NWE)}	FSMC_NWE low time	T _{HCLK} – 0.5	T _{HCLK} + 3	ns
t _{h(NE_NWE)}	FSMC_NWE high to FSMC_NE high hold time	T _{HCLK}	-	ns
t _{v(A_NE)}	FSMC_NEx low to FSMC_A valid	-	0	ns
t _{h(A_NWE)}	Address hold time after FSMC_NWE high	T _{HCLK} - 3	-	ns
t _{v(BL_NE)}	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
t _{h(BL_NWE)}	FSMC_BL hold time after FSMC_NWE high	T _{HCLK} – 1	-	ns
t _{v(Data_NE)}	Data to FSMC_NEx low to Data valid	-	T _{HCLK} + 5	ns
t _{h(Data_NWE)}	Data hold time after FSMC_NWE high	T _{HCLK} +0.5	-	ns
t _{v(NADV_NE)}	FSMC_NEx low to FSMC_NADV low	-	2	ns
t _{w(NADV)}	FSMC_NADV low time	-	T _{HCLK} + 1.5	ns

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.





Figure 67. PC Card/CompactFlash controller waveforms for attribute memory read access

1. Only data bits 0...7 are read (bits 8...15 are disregarded).





Symbol	Parameter	Conditions	Min	Max	Unit
f _{PP}	Clock frequency in data transfer mode	$C_L \le 30 \text{ pF}$	0	48	MHz
-	SDIO_CK/f _{PCLK2} frequency ratio	-	-	8/3	-
t _{W(CKL)}	Clock low time, f _{PP} = 16 MHz	$C_L \le 30 \text{ pF}$	32	-	
t _{W(CKH)}	Clock high time, f _{PP} = 16 MHz	$C_L \le 30 \text{ pF}$	31	-	20
t _r	Clock rise time	$C_L \le 30 \text{ pF}$	-	3.5	ns
t _f	Clock fall time	$C_L \le 30 \text{ pF}$	-	5	
CMD, D inputs (referenced to CK)					
t _{ISU}	Input setup time	$C_L \le 30 \text{ pF}$	2	-	200
t _{IH}	Input hold time	$C_L \le 30 \text{ pF}$	0	-	115
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t _{OV}	Output valid time	$C_L \le 30 \text{ pF}$	-	6	20
t _{OH}	Output hold time	$C_L \le 30 \text{ pF}$	0.3	-	115
CMD, D outputs (referenced to CK) in SD default mode ⁽¹⁾					
t _{OVD}	Output valid default time	$C_L \le 30 \text{ pF}$	-	7	20
t _{OHD}	Output hold default time	$C_L \le 30 \text{ pF}$	0.5	-	115

Table 85. SD/MMC characteristics

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

6.3.28 RTC characteristics

Table 86. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f _{PCLK1} /RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-



7.3 LQFP100 package information

Figure 81. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

mechanical data						
Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Мах
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 90. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data



Date	Revision	Changes
Date	Revision 11	Changes In the whole document, updated notes related to WLCSP64+2 usage with IRROFF set to V _{DD} . Updated Section 3.16.1: Regulator ON and Section 3.16: Power supply supervisor, Section 3.16.1: Regulator ON and Section 3.16: Regulator OFF. Added Section 3.16.3: Regulator ON/OFF and internal reset ON/OFF availability. Added note related to WLCSP64+2 package. Restructured RTC features and added reference clock detection in Section 3.17: Real-time clock (RTC), backup SRAM and backup registers. Added note indicating the package view below Figure 10: STM32F20X LQFP64 pinout, Figure 12: STM32F20X LQFP100 pinout, Figure 13: STM32F20x LQFP144 pinout, and Figure 14: STM32F20x LQFP176 pinout. Added Table 7: Legend/abbreviations used in the pinout table. Table 8: STM32F20x pin and ball definitions: content reformatted; removed indexes on V _{SS} and V _{DD} ; updated PA4, PA5, PA6, PC4, BOOT0; replaced DCMI_12 by DCMI_D12, TIM8_CHIN by TIM8_CH1N, ETH_MII_RX_D0 by ETH_MII_RXD0, ETH_MII_RXD0, ETH_MII_RXD0, ETH_MII_RXD1, and RMII_CRS_DV by ETH_RMII_RXD1, ETH_RMII_RXD1, and RMII_CRS_DV by ETH_RMII_RXD1, ETH_RMII_RXD1, and RMII_CRS_DV by ETH_RMII_RXD1, added EVENTOUT as AF15 alternated function for PC13, PC14, PC15, PH0, PH1, and PI8. Updated figure 17: Pin loading conditions and Figure 18: Pin input voltage. Added V _{IN} in Table 14: General operating conditions. Removed note applying to V _{POR/PER} minimum value in Table 19: Embedded reset and power control block characteristics. Updated Power control block characteristics. Updated conditions in Table 41: EMS characteristics.

