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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                               |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                        |
| Core Processor             | ARM® Cortex®-M3                                                                                                                                               |
| Core Size                  | 32-Bit Single-Core                                                                                                                                            |
| Speed                      | 120MHz                                                                                                                                                        |
| Connectivity               | CANbus, I <sup>2</sup> C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG                                                                                         |
| Peripherals                | Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT                                                                                             |
| Number of I/O              | 51                                                                                                                                                            |
| Program Memory Size        | 768KB (768K x 8)                                                                                                                                              |
| Program Memory Type        | FLASH                                                                                                                                                         |
| EEPROM Size                | -                                                                                                                                                             |
| RAM Size                   | 132K x 8                                                                                                                                                      |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V                                                                                                                                                   |
| Data Converters            | A/D 16x12b; D/A 2x12b                                                                                                                                         |
| Oscillator Type            | Internal                                                                                                                                                      |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                                                                 |
| Package / Case             | 64-LQFP                                                                                                                                                       |
| Supplier Device Package    | 64-LQFP (10x10)                                                                                                                                               |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205rft6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205rft6tr</a> |

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# 1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

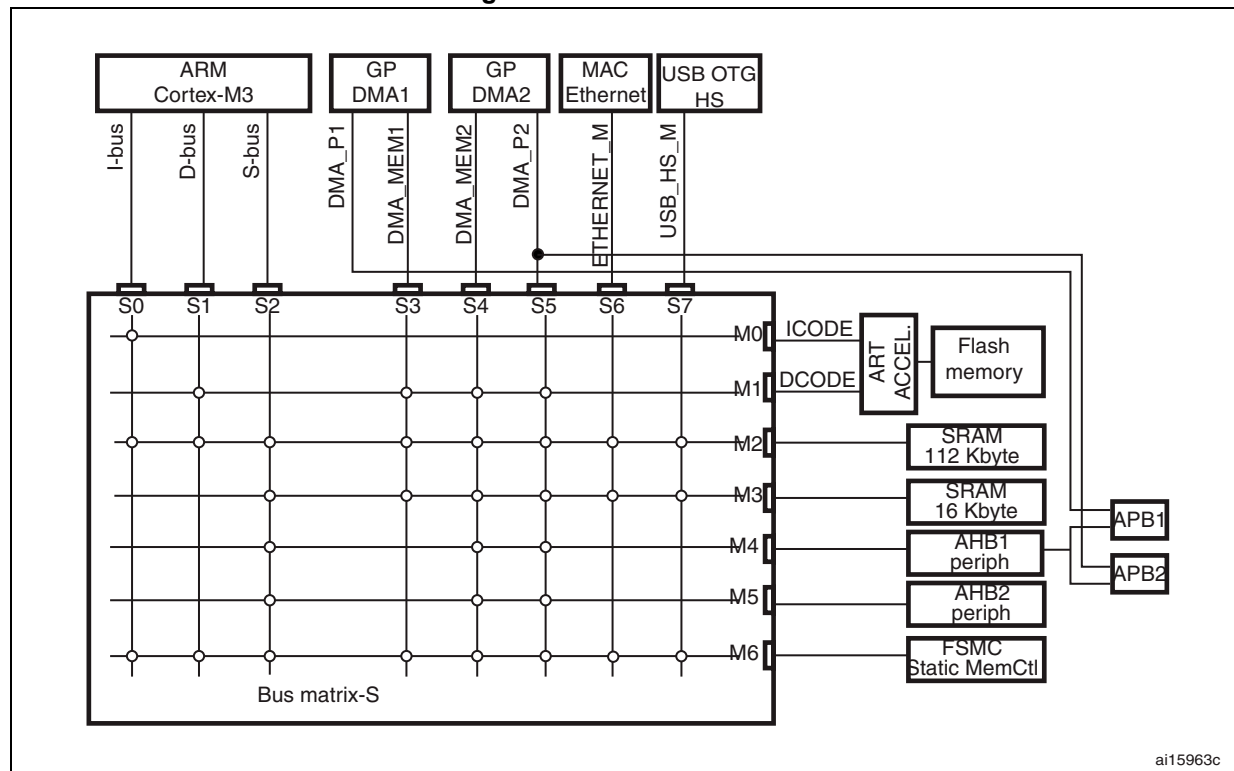
The reference and Flash programming manuals are both available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the Cortex<sup>®</sup>-M3 core please refer to the Cortex<sup>®</sup>-M3 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website.

**Table 2. STM32F205xx features and peripheral counts**

| Peripherals             |                        | STM32F205Rx                   |            |              |     |      | STM32F205Vx        |            |              |     |      | STM32F205Zx |              |     |      |
|-------------------------|------------------------|-------------------------------|------------|--------------|-----|------|--------------------|------------|--------------|-----|------|-------------|--------------|-----|------|
| Flash memory in Kbytes  |                        | 128                           | 256        | 512          | 768 | 1024 | 128                | 256        | 512          | 768 | 1024 | 256         | 512          | 768 | 1024 |
| SRAM in Kbytes          | System (SRAM1+SRAM2)   | 64 (48+16)                    | 96 (80+16) | 128 (112+16) |     |      | 64 (48+16)         | 96 (80+16) | 128 (112+16) |     |      | 96 (80+16)  | 128 (112+16) |     |      |
|                         | Backup                 | 4                             |            |              |     |      | 4                  |            |              |     |      | 4           |              |     |      |
| FSMC memory controller  |                        | No                            |            |              |     |      | Yes <sup>(1)</sup> |            |              |     |      |             |              |     |      |
| Ethernet                |                        | No                            |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Timers                  | General-purpose        | 10                            |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | Advanced-control       | 2                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | Basic                  | 2                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | IWDG                   | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | WWDG                   | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| RTC                     |                        | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Random number generator |                        | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Comm. interfaces        | SPI/(I <sup>2</sup> S) | 3/(2) <sup>(2)</sup>          |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | I <sup>2</sup> C       | 3                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | USART                  | 4                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | UART                   | 2                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | USB OTG FS             | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
|                         | USB OTG HS             | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| CAN                     |                        | 2                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Camera interface        |                        | No                            |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| GPIOs                   |                        | 51                            |            |              |     |      | 82                 |            |              |     |      | 114         |              |     |      |
| SDIO                    |                        | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| 12-bit ADC              |                        | 3                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Number of channels      |                        | 16                            |            |              |     |      | 16                 |            |              |     |      | 24          |              |     |      |
| 12-bit DAC              |                        | Yes                           |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Number of channels      |                        | 2                             |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Maximum CPU frequency   |                        | 120 MHz                       |            |              |     |      |                    |            |              |     |      |             |              |     |      |
| Operating voltage       |                        | 1.8 V to 3.6 V <sup>(3)</sup> |            |              |     |      |                    |            |              |     |      |             |              |     |      |

Figure 5. Multi-AHB matrix



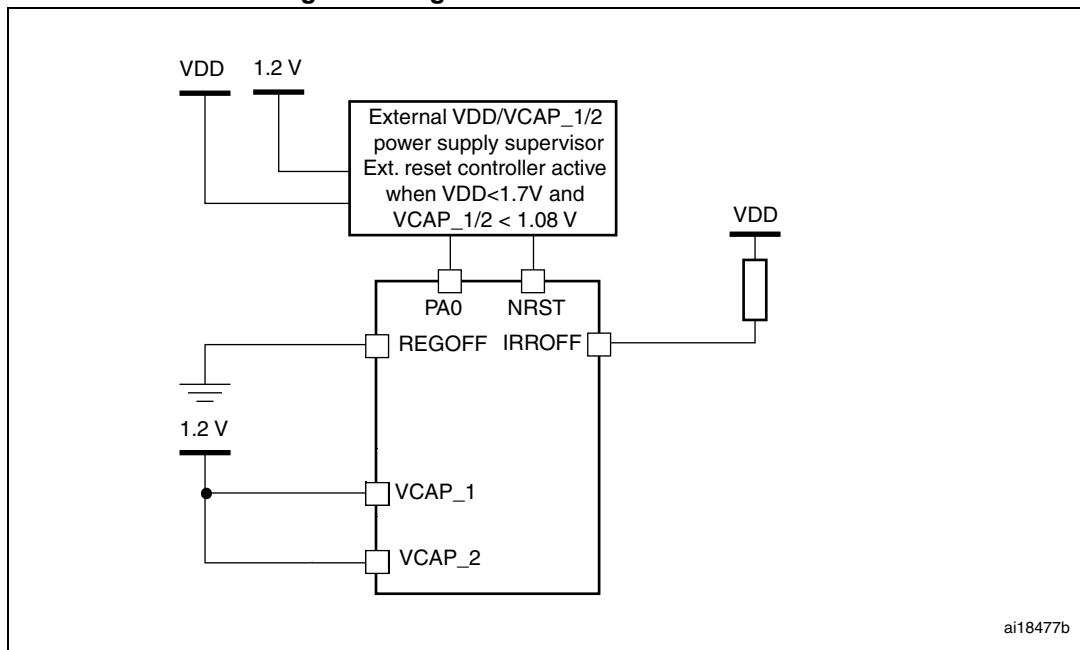
### 3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

Figure 7. Regulator OFF/internal reset OFF



The following conditions must be respected:

- $V_{DD}$  should always be higher than  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to avoid current injection between power domains (see [Figure 8](#)).
- PA0 should be kept low to cover both conditions: until  $V_{CAP\_1}$  and  $V_{CAP\_2}$  reach 1.08 V, and until  $V_{DD}$  reaches 1.7 V.
- NRST should be controlled by an external reset controller to keep the device under reset when  $V_{DD}$  is below 1.7 V (see [Figure 9](#)).

In this mode, when the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry is disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$  functionality is no more available and  $V_{BAT}$  pin should be connected to VDD.

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

### 3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see [Table 5](#) for differences).

#### TIM2, TIM3, TIM4, TIM5

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

#### TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

#### TIM12, TIM13 and TIM14

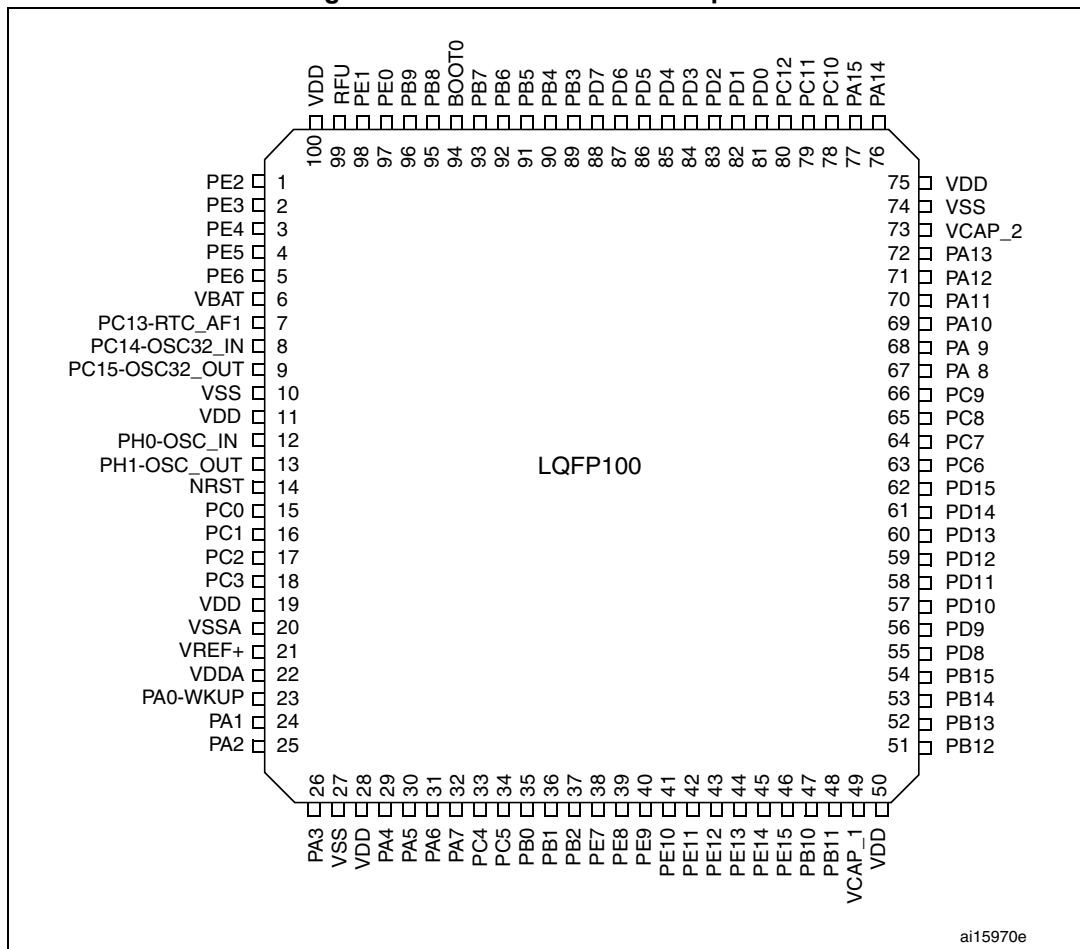
These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

### 3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

Figure 12. STM32F20x LQFP100 pinout



1. RFU means "reserved for future use". This pin can be tied to  $V_{DD}$ ,  $V_{SS}$  or left unconnected.
2. The above figure shows the package top view.



Table 10. Alternate function mapping (continued)

| Port   |      | AF0 | AF1    | AF2      | AF3          | AF4            | AF5            | AF6       | AF7        | AF8                | AF9                       | AF10           | AF11                            | AF12                     | AF13     | AF014 | AF15     |
|--------|------|-----|--------|----------|--------------|----------------|----------------|-----------|------------|--------------------|---------------------------|----------------|---------------------------------|--------------------------|----------|-------|----------|
|        |      | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/<br>USART6 | CAN1/CAN2/<br>TIM12/13/14 | OTG_FS/ OTG_HS | ETH                             | FSMC/SDIO/<br>OTG_HS     | DCMI     |       |          |
| Port F | PF0  | -   | -      | -        | -            | I2C2_SDA       | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A0                  | -        | -     | EVENTOUT |
|        | PF1  | -   | -      | -        | -            | I2C2_SCL       | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A1                  | -        | -     | EVENTOUT |
|        | PF2  | -   | -      | -        | -            | I2C2_SMBA      | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A2                  | -        | -     | EVENTOUT |
|        | PF3  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A3                  | -        | -     | EVENTOUT |
|        | PF4  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A4                  | -        | -     | EVENTOUT |
|        | PF5  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A5                  | -        | -     | EVENTOUT |
|        | PF6  | -   | -      | -        | TIM10_CH1    | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_NIORD               | -        | -     | EVENTOUT |
|        | PF7  | -   | -      | -        | TIM11_CH1    | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_NREG                | -        | -     | EVENTOUT |
|        | PF8  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | TIM13_CH1                 | -              | -                               | FSMC_NIOWR               | -        | -     | EVENTOUT |
|        | PF9  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | TIM14_CH1                 | -              | -                               | FSMC_CD                  | -        | -     | EVENTOUT |
|        | PF10 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_INTR                | -        | -     | EVENTOUT |
|        | PF11 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               |                          | DCMI_D12 | -     | EVENTOUT |
|        | PF12 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A6                  | -        | -     | EVENTOUT |
|        | PF13 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A7                  | -        | -     | EVENTOUT |
|        | PF14 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A8                  | -        | -     | EVENTOUT |
|        | PF15 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A9                  | -        | -     | EVENTOUT |
| Port G | PG0  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A10                 | -        | -     | EVENTOUT |
|        | PG1  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A11                 | -        | -     | EVENTOUT |
|        | PG2  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A12                 | -        | -     | EVENTOUT |
|        | PG3  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A13                 | -        | -     | EVENTOUT |
|        | PG4  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A14                 | -        | -     | EVENTOUT |
|        | PG5  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_A15                 | -        | -     | EVENTOUT |
|        | PG6  | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_INT2                | -        | -     | EVENTOUT |
|        | PG7  | -   | -      | -        | -            | -              | -              | -         | -          | USART6_CK          | -                         | -              | -                               | FSMC_INT3                | -        | -     | EVENTOUT |
|        | PG8  | -   | -      | -        | -            | -              | -              | -         | -          | USART6_RTS         | -                         | -              | ETH_PPS_OUT                     | -                        | -        | -     | EVENTOUT |
|        | PG9  | -   | -      | -        | -            | -              | -              | -         | -          | USART6_RX          | -                         | -              | -                               | FSMC_NE2/<br>FSMC_NCE3   | -        | -     | EVENTOUT |
|        | PG10 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | -                               | FSMC_NCE4_1/<br>FSMC_NE3 | -        | -     | EVENTOUT |
|        | PG11 | -   | -      | -        | -            | -              | -              | -         | -          | -                  | -                         | -              | ETH_MII_TX_EN<br>ETH_RMII_TX_EN | FSMC_NCE4_2              | -        | -     | EVENTOUT |
|        | PG12 | -   | -      | -        | -            | -              | -              | -         | -          | USART6_RTS         | -                         | -              | -                               | FSMC_NE4                 | -        | -     | EVENTOUT |
|        | PG13 | -   | -      | -        | -            | -              | -              | -         | -          | UART6_CTS          | -                         | -              | ETH_MII_TXD0<br>ETH_RMII_TXD0   | FSMC_A24                 | -        | -     | EVENTOUT |
|        | PG14 | -   | -      | -        | -            | -              | -              | -         | -          | USART6_TX          | -                         | -              | ETH_MII_TXD1<br>ETH_RMII_TXD1   | FSMC_A25                 | -        | -     | EVENTOUT |
|        | PG15 | -   | -      | -        | -            | -              | -              | -         | -          | USART6_CTS         | -                         | -              | -                               | -                        | DCMI_D13 | -     | EVENTOUT |

|             |                                                       |                              |                           |
|-------------|-------------------------------------------------------|------------------------------|---------------------------|
| 0xFFFF FFFF | 512-Mbyte block 7<br>Cortex-M3's internal peripherals | Reserved                     | 0xA000 1000 - 0xBFFF FFFF |
| 0xE000 0000 | 512-Mbyte block 6<br>Not used                         | FSMC control register        | 0xA000 0000 - 0xA000 0FFF |
| 0xDFFF FFFF |                                                       | FSMC bank4 PC Card           | 0x9000 0000 - 0x9FFF FFFF |
| 0xC000 0000 | 512-Mbyte block 5<br>FSMC registers                   | FSMC bank3 NAND (NAND2)      | 0x8000 0000 - 0x8FFF FFFF |
| 0xBFFF FFFF |                                                       | FSMC bank2 NAND (NAND1)      | 0x7000 0000 - 0x7FFF FFFF |
| 0xA000 0000 | 512-Mbyte block 4<br>FSMC bank 3 & bank4              | FSMC bank1 NOR/PSRAM 4       | 0x6C00 0000 - 0x6FFF FFFF |
| 0x9FFF FFFF |                                                       | FSMC bank1 NOR/PSRAM 3       | 0x6800 0000 - 0x6BFF FFFF |
| 0x8000 0000 | 512-Mbyte block 3<br>FSMC bank1 & bank2               | FSMC bank1 NOR/PSRAM 2       | 0x6400 0000 - 0x67FF FFFF |
| 0x7FFF FFFF |                                                       | FSMC bank1 NOR/PSRAM 1       | 0x6000 0000 - 0x63FF FFFF |
| 0x6000 0000 | 512-Mbyte block 2<br>Peripherals                      | Reserved                     | 0x5006 1000 - 0x5FFF FFFF |
| 0x5FFF FFFF |                                                       | RNG                          | 0x5006 0800 - 0x5006 0FFF |
| 0x4000 0000 | 512-Mbyte block 1<br>SRAM                             | Reserved                     | 0x5005 0400 - 0x5006 7FFF |
| 0x3FFF FFFF |                                                       | DCMI                         | 0x5005 0000 - 0x5005 03FF |
| 0x2000 0000 | 512-Mbyte block 0<br>Code                             | Reserved                     | 0x5004 0000 - 0x5004 0FFF |
| 0x1FFF FFFF |                                                       | USB OTG FS                   | 0x5000 0000 - 0x5003 FFFF |
| 0x0000 0000 |                                                       | Reserved                     | 0x4002 9400 - 0x4FFF FFFF |
|             |                                                       | USB OTG HS                   | 0x4004 0000 - 0x4007 FFFF |
|             |                                                       | Reserved                     | 0x4002 9400 - 0x4003 FFFF |
|             |                                                       | ETHERNET                     | 0x4002 8000 - 0x4002 93FF |
|             |                                                       | Reserved                     | 0x4002 6800 - 0x4002 7FFF |
|             |                                                       | DMA2                         | 0x4002 6400 - 0x4002 67FF |
|             |                                                       | DMA1                         | 0x4002 6000 - 0x4002 63FF |
|             |                                                       | Reserved                     | 0x4002 5000 - 0x4002 5FFF |
|             |                                                       | BKPSRAM                      | 0x4002 4000 - 0x4002 4FFF |
|             |                                                       | Flash interface              | 0x4002 3C00 - 0x4002 3FFF |
|             |                                                       | Reset clock controller (RCC) | 0x4002 3800 - 0x4002 3BFF |
|             |                                                       | Reserved                     | 0x4002 3400 - 0x4002 37FF |
|             |                                                       | CRC                          | 0x4002 3000 - 0x4002 33FF |
|             |                                                       | Reserved                     | 0x4002 2400 - 0x4002 2FFF |
|             |                                                       | Port I                       | 0x4002 2000 - 0x4002 23FF |
|             |                                                       | Port H                       | 0x4002 1C00 - 0x4002 1FFF |
|             |                                                       | Port G                       | 0x4002 1800 - 0x4002 1BFF |
|             |                                                       | Port F                       | 0x4002 1400 - 0x4002 17FF |
|             |                                                       | Port E                       | 0x4002 1000 - 0x4002 13FF |
|             |                                                       | Port D                       | 0x4002 0C00 - 0x4002 0FFF |
|             |                                                       | Port C                       | 0x4002 0800 - 0x4002 0BFF |
|             |                                                       | Port B                       | 0x4002 0400 - 0x4002 07FF |
|             |                                                       | Port A                       | 0x4002 0000 - 0x4002 03FF |
|             |                                                       | Reserved                     | 0x4001 4C00 - 0x4001 FFFF |
|             |                                                       | TIM11                        | 0x4001 4800 - 0x4001 4BFF |
|             |                                                       | TIM10                        | 0x4001 4400 - 0x4001 47FF |
|             |                                                       | TIM9                         | 0x4001 4000 - 0x4001 43FF |
|             |                                                       | EXTI                         | 0x4001 3C00 - 0x4001 3FFF |
|             |                                                       | SYSCFG                       | 0x4001 3800 - 0x4001 3BFF |
|             |                                                       | Reserved                     | 0x4001 3400 - 0x4001 37FF |
|             |                                                       | SP11                         | 0x4001 3000 - 0x4001 33FF |
|             |                                                       | SDIO                         | 0x4001 2C00 - 0x4001 2FFF |
|             |                                                       | Reserved                     | 0x4001 2800 - 0x4001 2BFF |
|             |                                                       | Reserved                     | 0x4001 2400 - 0x4001 27FF |
|             |                                                       | ADC1 - ADC2 - ADC3           | 0x4001 2000 - 0x4001 23FF |
|             |                                                       | Reserved                     | 0x4001 1800 - 0x4001 1FFF |
|             |                                                       | USART6                       | 0x4001 1400 - 0x4001 17FF |
|             |                                                       | USART1                       | 0x4001 1000 - 0x4001 13FF |
|             |                                                       | Reserved                     | 0x4001 0800 - 0x4001 0FFF |
|             |                                                       | TIM8 / PWM2                  | 0x4001 0400 - 0x4001 07FF |
|             |                                                       | TIM1 / PWM1                  | 0x4001 0000 - 0x4001 03FF |
|             |                                                       | Reserved                     | 0x4000 7800 - 0x4000 FFFF |
|             |                                                       | DAC1/DAC2                    | 0x4000 7400 - 0x4000 77FF |
|             |                                                       | PWR                          | 0x4000 7000 - 0x4000 73FF |
|             |                                                       | Reserved                     | 0x4000 6C00 - 0x4000 6FFF |
|             |                                                       | BxCAN2                       | 0x4000 6800 - 0x4000 6BFF |
|             |                                                       | BxCAN1                       | 0x4000 6400 - 0x4000 67FF |
|             |                                                       | Reserved                     | 0x4000 6000 - 0x4000 63FF |
|             |                                                       | I2C3                         | 0x4000 5C00 - 0x4000 5FFF |
|             |                                                       | I2C2                         | 0x4000 5800 - 0x4000 5BFF |
|             |                                                       | I2C1                         | 0x4000 5400 - 0x4000 57FF |
|             |                                                       | UART5                        | 0x4000 5000 - 0x4000 53FF |
|             |                                                       | UART4                        | 0x4000 4C00 - 0x4000 4FFF |
|             |                                                       | USART3                       | 0x4000 4800 - 0x4000 4BFF |
|             |                                                       | USART2                       | 0x4000 4400 - 0x4000 47FF |
|             |                                                       | Reserved                     | 0x4000 4000 - 0x4000 43FF |
|             |                                                       |                              |                           |

Table 15. Limitations depending on the operating power supply range

| Operating power supply range                                   | ADC operation                | Maximum Flash memory access frequency ( $f_{\text{Flashmax}}$ ) | Number of wait states at maximum CPU frequency ( $f_{\text{CPUmax}} = 120 \text{ MHz}$ ) <sup>(1)</sup> | I/O operation                                                                                                    | FSMC_CLK frequency for synchronous accesses                                                                                                                                                                              | Possible Flash memory operations        |
|----------------------------------------------------------------|------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|
| $V_{\text{DD}} = 1.8 \text{ to } 2.1 \text{ V}$ <sup>(2)</sup> | Conversion time up to 1 Msps | 16 MHz with no Flash memory wait state                          | 7 <sup>(3)</sup>                                                                                        | <ul style="list-style-type: none"> <li>– Degraded speed performance</li> <li>– No I/O compensation</li> </ul>    | Up to 30 MHz                                                                                                                                                                                                             | 8-bit erase and program operations only |
| $V_{\text{DD}} = 2.1 \text{ to } 2.4 \text{ V}$                | Conversion time up to 1 Msps | 18 MHz with no Flash memory wait state                          | 6 <sup>(3)</sup>                                                                                        | <ul style="list-style-type: none"> <li>– Degraded speed performance</li> <li>– No I/O compensation</li> </ul>    | Up to 30 MHz                                                                                                                                                                                                             | 16-bit erase and program operations     |
| $V_{\text{DD}} = 2.4 \text{ to } 2.7 \text{ V}$                | Conversion time up to 2 Msps | 24 MHz with no Flash memory wait state                          | 4 <sup>(3)</sup>                                                                                        | <ul style="list-style-type: none"> <li>– Degraded speed performance</li> <li>– I/O compensation works</li> </ul> | Up to 48 MHz                                                                                                                                                                                                             | 16-bit erase and program operations     |
| $V_{\text{DD}} = 2.7 \text{ to } 3.6 \text{ V}$ <sup>(4)</sup> | Conversion time up to 2 Msps | 30 MHz with no Flash memory wait state                          | 3 <sup>(3)</sup>                                                                                        | <ul style="list-style-type: none"> <li>– Full-speed operation</li> <li>– I/O compensation works</li> </ul>       | <ul style="list-style-type: none"> <li>– Up to 60 MHz when <math>V_{\text{DD}} = 3.0 \text{ to } 3.6 \text{ V}</math></li> <li>– Up to 48 MHz when <math>V_{\text{DD}} = 2.7 \text{ to } 3.0 \text{ V}</math></li> </ul> | 32-bit erase and program operations     |

1. The number of wait states can be reduced by reducing the CPU frequency (see [Figure 21](#)).
2. On devices in WLCSP64+2 package, if IRROFF is set to  $V_{\text{DD}}$ , the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

Table 26. Peripheral current consumption (continued)

| Peripheral <sup>(1)</sup> |                     | Typical consumption at 25 °C | Unit |
|---------------------------|---------------------|------------------------------|------|
| APB2                      | SDIO                | 0.69                         | mA   |
|                           | TIM1                | 1.06                         |      |
|                           | TIM8                | 1.03                         |      |
|                           | TIM9                | 0.58                         |      |
|                           | TIM10               | 0.37                         |      |
|                           | TIM11               | 0.39                         |      |
|                           | ADC1 <sup>(4)</sup> | 2.13                         |      |
|                           | ADC2 <sup>(4)</sup> | 2.04                         |      |
|                           | ADC3 <sup>(4)</sup> | 2.12                         |      |
|                           | SPI1                | 1.20                         |      |
|                           | USART1              | 0.38                         |      |
|                           | USART6              | 0.37                         |      |

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC\_CR register.
3. EN2 bit is set in DAC\_CR register.
4.  $f_{ADC} = f_{PCLK2}/2$ , ADON bit set in ADC\_CR2 register.

### 6.3.7 Wakeup time from low-power mode

The wakeup times given in [Table 27](#) is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 14](#).

Table 27. Low-power mode wakeup timings

| Symbol                 | Parameter                                                                                    | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|------------------------|----------------------------------------------------------------------------------------------|--------------------|--------------------|--------------------|------|
| $t_{WUSLEEP}^{(2)}$    | Wakeup from Sleep mode                                                                       | -                  | 1                  | -                  | μs   |
| $t_{WUSTOP}^{(2)}$     | Wakeup from Stop mode (regulator in Run mode)                                                | -                  | 13                 | -                  | μs   |
|                        | Wakeup from Stop mode (regulator in low-power mode)                                          | -                  | 17                 | 40                 |      |
|                        | Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode) | -                  | 110                | -                  |      |
| $t_{WUSTDBY}^{(2)(3)}$ | Wakeup from Standby mode                                                                     | 260                | 375                | 480                | μs   |

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3.  $t_{WUSTDBY}$  minimum and maximum values are given at 105 °C and -45 °C, respectively.

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC<sup>®</sup> code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

**Table 42. EMI characteristics**

| Symbol           | Parameter  | Conditions                                                                                                                                                                               | Monitored frequency band | Max vs. [f <sub>HSE</sub> /f <sub>CPU</sub> ] | Unit |
|------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-----------------------------------------------|------|
|                  |            |                                                                                                                                                                                          |                          | 25/120 MHz                                    |      |
| S <sub>EMI</sub> | Peak level | V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, peripheral clock disabled                              | 0.1 to 30 MHz            | 25                                            | dBμV |
|                  |            |                                                                                                                                                                                          | 30 to 130 MHz            |                                               |      |
|                  |            |                                                                                                                                                                                          | 130 MHz to 1GHz          |                                               |      |
|                  |            |                                                                                                                                                                                          | SAE EMI Level            | 4                                             | -    |
|                  |            | V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, PLL spread spectrum enabled, peripheral clock disabled | 0.1 to 30 MHz            | 28                                            | dBμV |
|                  |            |                                                                                                                                                                                          | 30 to 130 MHz            | 26                                            |      |
|                  |            |                                                                                                                                                                                          | 130 MHz to 1GHz          | 22                                            |      |
|                  |            |                                                                                                                                                                                          | SAE EMI level            | 4                                             | -    |

### 6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 43. ESD absolute maximum ratings**

| Symbol                | Ratings                                               | Conditions                                        | Class | Maximum value <sup>(1)</sup> | Unit |
|-----------------------|-------------------------------------------------------|---------------------------------------------------|-------|------------------------------|------|
| V <sub>ESD(HBM)</sub> | Electrostatic discharge voltage (human body model)    | T <sub>A</sub> = +25 °C conforming to JESD22-A114 | 2     | 2000 <sup>(2)</sup>          | V    |
| V <sub>ESD(CDM)</sub> | Electrostatic discharge voltage (charge device model) | T <sub>A</sub> = +25 °C conforming to JESD22-C101 | II    | 500                          |      |

1. Guaranteed by characterization results, not tested in production.

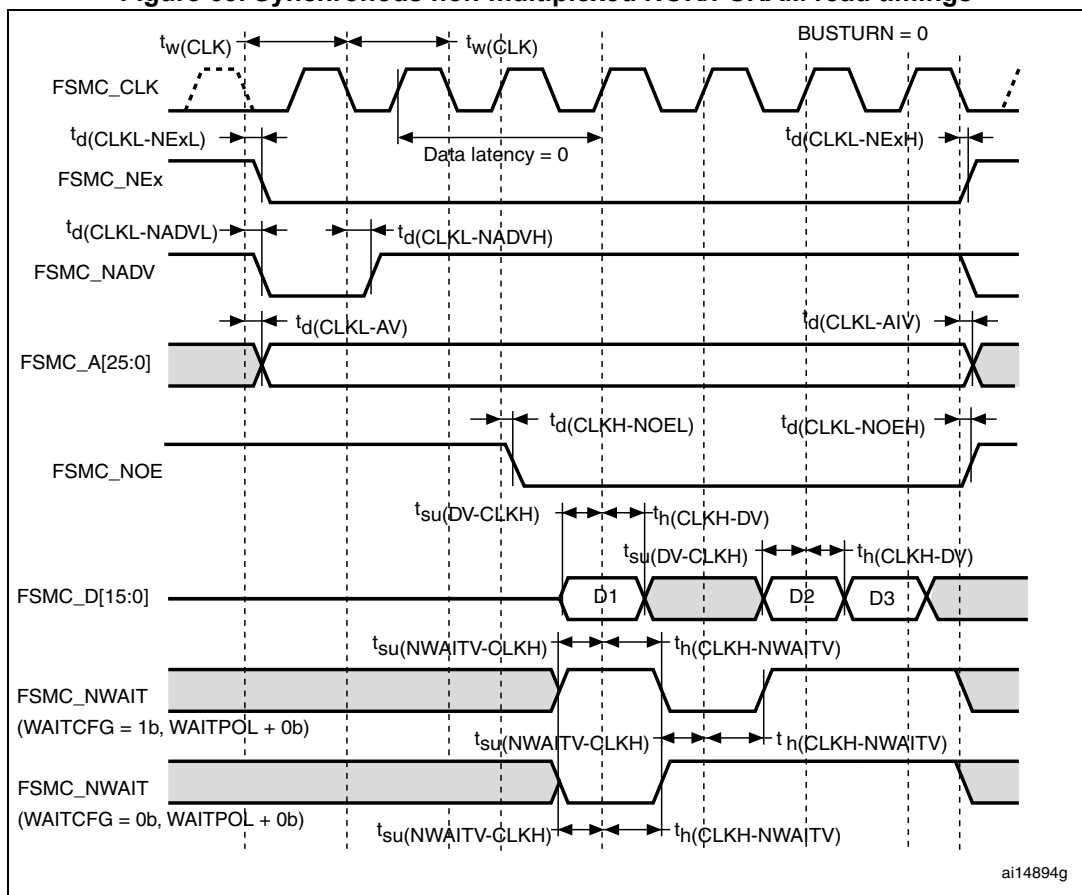
2. On V<sub>BAT</sub> pin, V<sub>ESD(HBM)</sub> is limited to 1000 V.

**Table 77. Synchronous multiplexed PSRAM write timings<sup>(1)(2)</sup> (continued)**

| Symbol             | Parameter                                    | Min | Max | Unit |
|--------------------|----------------------------------------------|-----|-----|------|
| $t_{d(CLKL-NWEL)}$ | FSMC_CLK low to FSMC_NWE low                 | -   | 1   | ns   |
| $t_{d(CLKL-NWEH)}$ | FSMC_CLK low to FSMC_NWE high                | 0   | -   | ns   |
| $t_{d(CLKL-ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid        | 0   | -   | ns   |
| $t_{d(CLKL-DATA)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK low | -   | 2   | ns   |
| $t_{d(CLKL-NBLH)}$ | FSMC_CLK low to FSMC_NBL high                | 0.5 | -   | ns   |

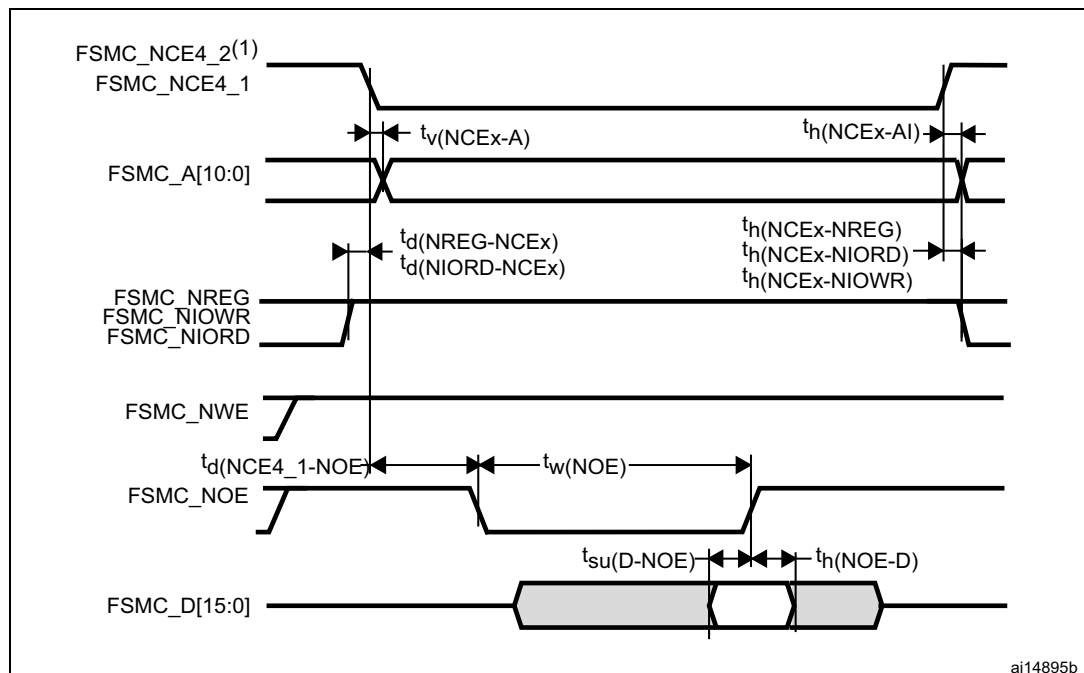
1.  $C_L = 30$  pF.

2. Guaranteed by characterization results, not tested in production.

**Figure 63. Synchronous non-multiplexed NOR/PSRAM read timings****Table 78. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup>**

| Symbol             | Parameter                                | Min         | Max | Unit |
|--------------------|------------------------------------------|-------------|-----|------|
| $t_w(CLK)$         | FSMC_CLK period                          | $2T_{HCLK}$ | -   | ns   |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x=0..2)    | -           | 0   | ns   |
| $t_{d(CLKL-NExH)}$ | FSMC_CLK low to FSMC_NEx high (x= 0...2) | 1           | -   | ns   |
| $t_{d(CLKL-NADV)}$ | FSMC_CLK low to FSMC_NADV low            | -           | 2.5 | ns   |

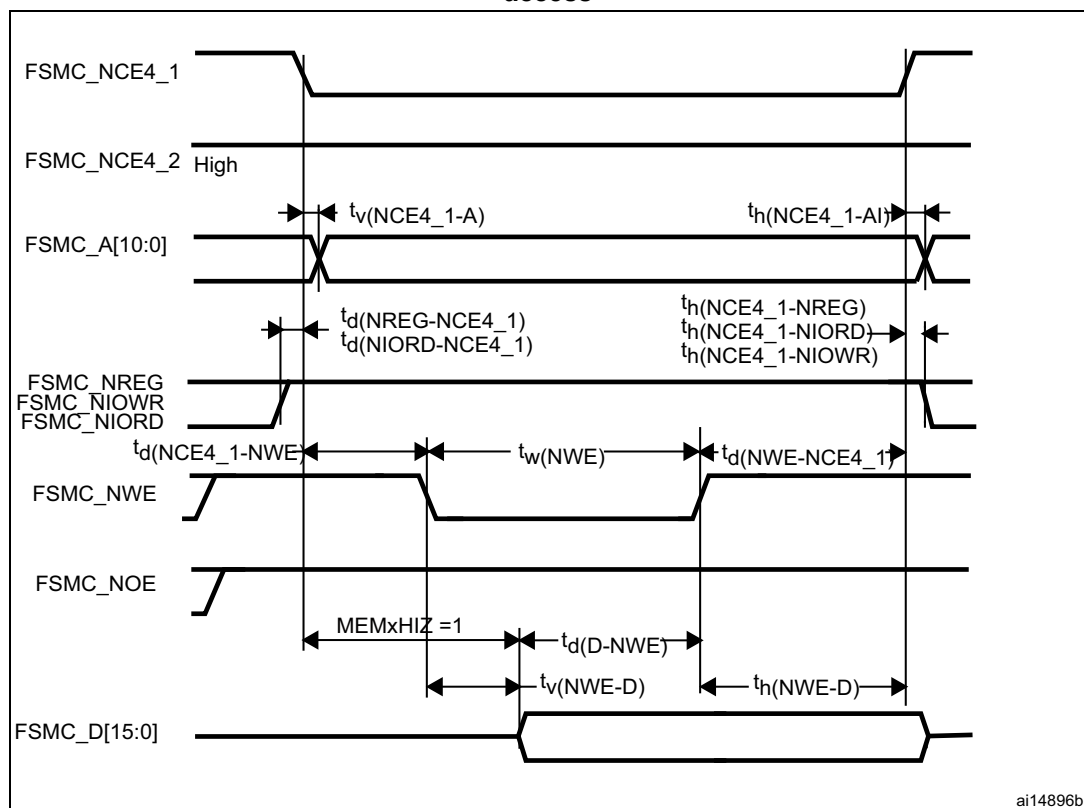
**Figure 65. PC Card/CompactFlash controller waveforms for common memory read access**



ai14895b

1. FSMC\_NCE4\_2 remains high (inactive during 8-bit access).

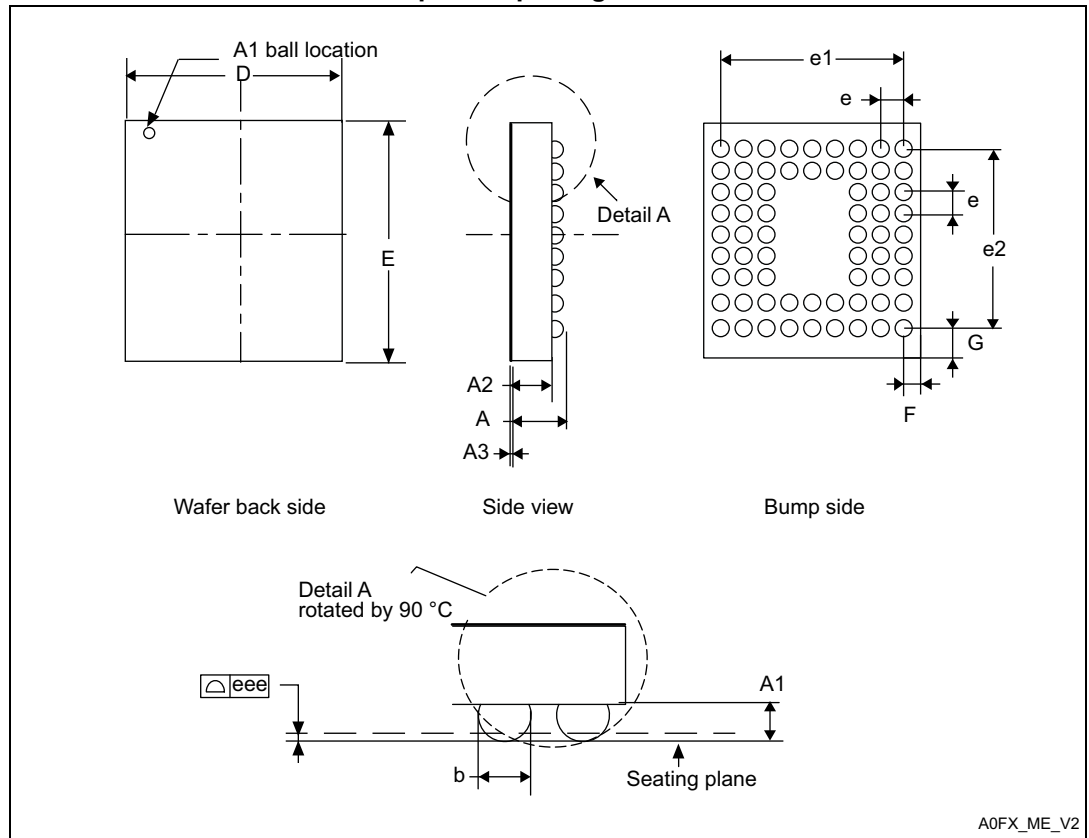
**Figure 66. PC Card/CompactFlash controller waveforms for common memory write access**



ai14896b

## 7.2 WLCSP64+2 package information

Figure 79. WLCSP64+2 - 66-ball, 3.639 x 3.971 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data

| Symbol           | millimeters |       |       | inches <sup>(1)</sup> |        |        |
|------------------|-------------|-------|-------|-----------------------|--------|--------|
|                  | Min         | Typ   | Max   | Min                   | Typ    | Max    |
| A                | 0.540       | 0.570 | 0.600 | 0.0213                | 0.0224 | 0.0236 |
| A1               | -           | 0.190 | -     | -                     | 0.0075 | -      |
| A2               | -           | 0.380 | -     | -                     | 0.0150 | -      |
| A3               | -           | 0.025 | -     | -                     | 0.010  | -      |
| b <sup>(2)</sup> | 0.240       | 0.270 | 0.300 | 0.0094                | 0.0106 | 0.0118 |
| D                | 3.604       | 3.939 | 3.674 | 0.1419                | 0.1551 | 0.1446 |
| E                | 3.936       | 3.971 | 4.006 | 0.1550                | 0.1563 | 0.1577 |
| e                | -           | 0.400 | -     | -                     | 0.0157 | -      |
| e1               | -           | 3.200 | -     | -                     | 0.1260 | -      |
| e2               | -           | 3.200 | -     | -                     | 0.1260 | -      |

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| D3     | -           | 12.000 | -      | -                     | 0.4724 | -      |
| E      | 15.800      | 16.000 | 16.200 | 0.6220                | 0.6299 | 0.6378 |
| E1     | 13.800      | 14.000 | 14.200 | 0.5433                | 0.5512 | 0.5591 |
| E3     | -           | 12.000 | -      | -                     | 0.4724 | -      |
| e      | -           | 0.500  | -      | -                     | 0.0197 | -      |
| L      | 0.450       | 0.600  | 0.750  | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000  | -      | -                     | 0.0394 | -      |
| k      | 0.0°        | 3.5°   | 7.0°   | 0.0°                  | 3.5°   | 7.0°   |
| ccc    | -           | -      | 0.080  | -                     | -      | 0.0031 |

**Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**

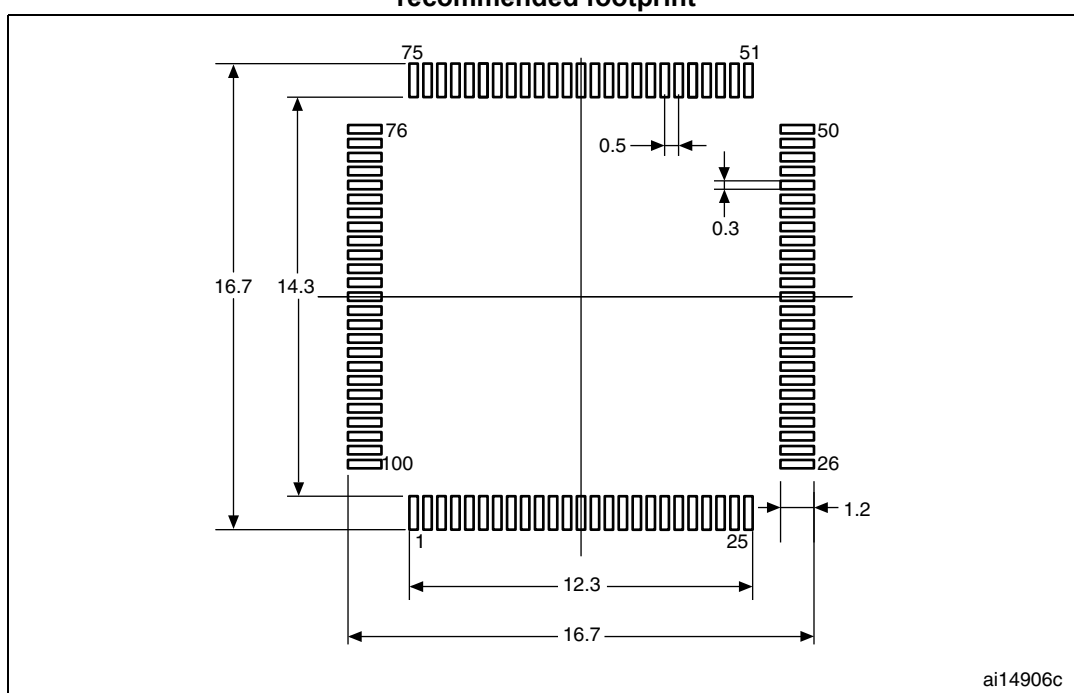
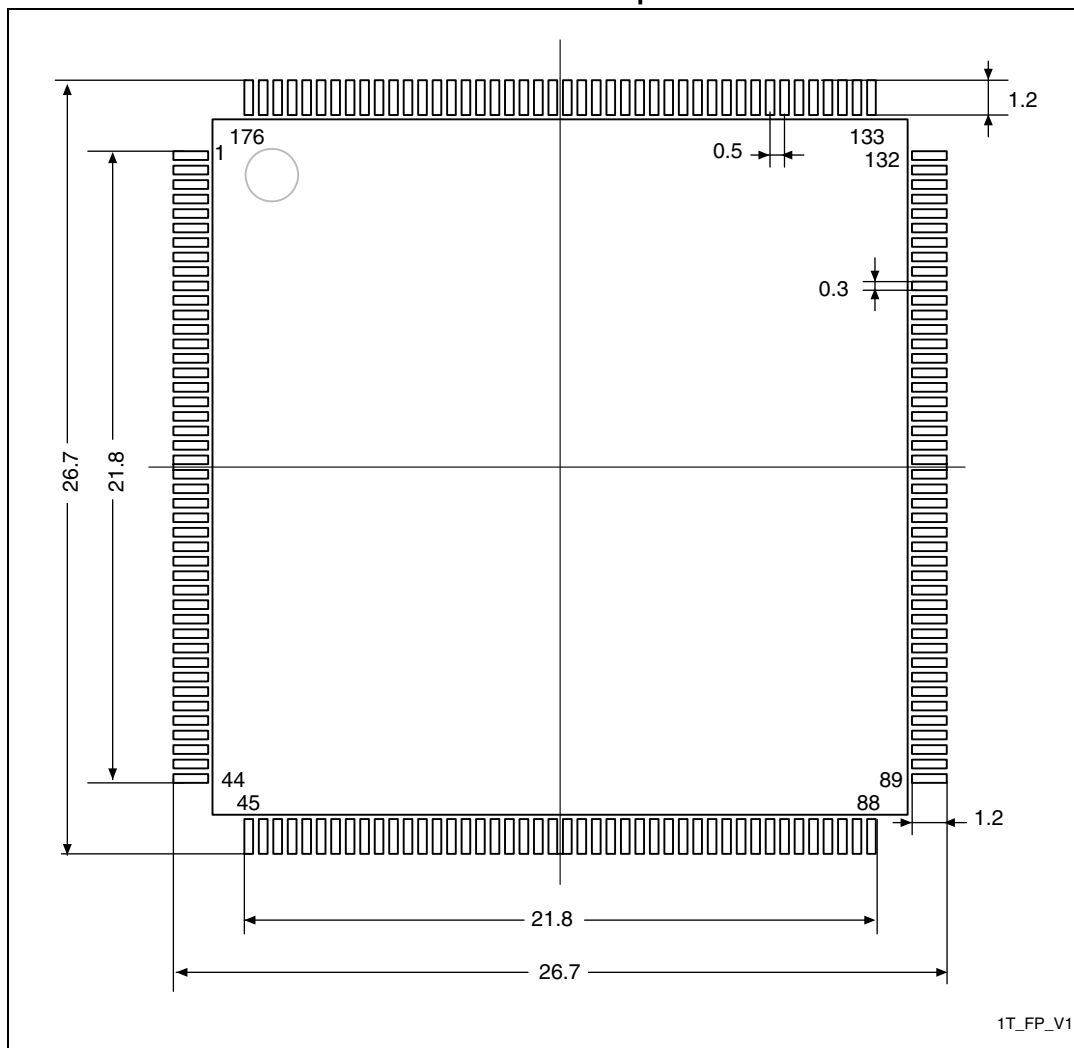


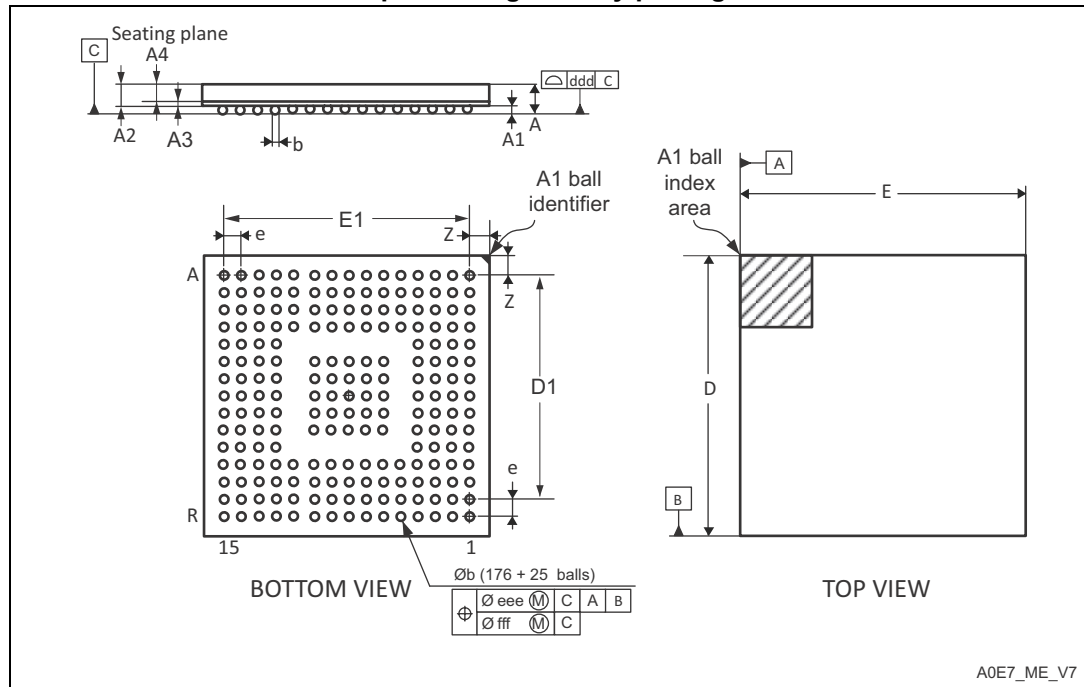
Figure 88. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

## 7.6 UFBGA176+25 package information

**Figure 89. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline**



1. Drawing is not to scale.

**Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data**

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min.        | Typ.   | Max.   | Min.                  | Typ.   | Max.   |
| A      | -           | -      | 0.600  | -                     | -      | 0.0236 |
| A1     | -           | -      | 0.110  | -                     | -      | 0.0043 |
| A2     | -           | 0.450  | -      | -                     | 0.0177 | -      |
| A3     | -           | 0.130  | -      | -                     | 0.0051 | 0.0094 |
| A4     | -           | 0.320  | -      | -                     | 0.0126 | -      |
| b      | 0.240       | 0.290  | 0.340  | 0.0094                | 0.0114 | 0.0134 |
| D      | 9.850       | 10.000 | 10.150 | 0.3878                | 0.3937 | 0.3996 |
| D1     | -           | 9.100  | -      | -                     | 0.3583 | -      |
| E      | 9.850       | 10.000 | 10.150 | 0.3878                | 0.3937 | 0.3996 |
| E1     | -           | 9.100  | -      | -                     | 0.3583 | -      |
| e      | -           | 0.650  | -      | -                     | 0.0256 | -      |
| Z      | -           | 0.450  | -      | -                     | 0.0177 | -      |
| ddd    | -           | -      | 0.080  | -                     | -      | 0.0031 |

## 8 Part numbering

Table 96. Ordering information scheme

|                                                                                                                                                                         |       |   |     |   |   |   |   |      |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|---|-----|---|---|---|---|------|
| Example:                                                                                                                                                                | STM32 | F | 205 | R | E | T | 6 | Vxxx |
| <b>Device family</b>                                                                                                                                                    |       |   |     |   |   |   |   |      |
| STM32 = ARM-based 32-bit microcontroller                                                                                                                                |       |   |     |   |   |   |   |      |
| <b>Product type</b>                                                                                                                                                     |       |   |     |   |   |   |   |      |
| F = general-purpose                                                                                                                                                     |       |   |     |   |   |   |   |      |
| <b>Device subfamily</b>                                                                                                                                                 |       |   |     |   |   |   |   |      |
| 205 = STM32F20x, connectivity<br>207= STM32F20x, connectivity, camera interface, Ethernet                                                                               |       |   |     |   |   |   |   |      |
| <b>Pin count</b>                                                                                                                                                        |       |   |     |   |   |   |   |      |
| R = 64 pins or 66 pins <sup>(1)</sup><br>V = 100 pins<br>Z = 144 pins<br>I = 176 pins                                                                                   |       |   |     |   |   |   |   |      |
| <b>Flash memory size</b>                                                                                                                                                |       |   |     |   |   |   |   |      |
| B = 128 Kbytes of Flash memory<br>C = 256 Kbytes of Flash memory<br>E = 512 Kbytes of Flash memory<br>F = 768 Kbytes of Flash memory<br>G = 1024 Kbytes of Flash memory |       |   |     |   |   |   |   |      |
| <b>Package</b>                                                                                                                                                          |       |   |     |   |   |   |   |      |
| T = LQFP<br>H = UFBGA<br>Y = WLCSP                                                                                                                                      |       |   |     |   |   |   |   |      |
| <b>Temperature range</b>                                                                                                                                                |       |   |     |   |   |   |   |      |
| 6 = Industrial temperature range, –40 to 85 °C.<br>7 = Industrial temperature range, –40 to 105 °C.                                                                     |       |   |     |   |   |   |   |      |
| <b>Software option</b>                                                                                                                                                  |       |   |     |   |   |   |   |      |
| Internal code or Blank                                                                                                                                                  |       |   |     |   |   |   |   |      |
| <b>Options</b>                                                                                                                                                          |       |   |     |   |   |   |   |      |
| xxx = programmed parts<br>TR = tape and reel                                                                                                                            |       |   |     |   |   |   |   |      |

1. The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.