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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205rgt6w

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Table 2. STM32F205xx features and peripheral counts (continued)

Peripherals	STM32F205Rx				STM32F205Vx		STM32F205Zx
Operating temperatures	Ambient temperatures: −40 to +85 °C /−40 to +105 °C						
	Junction temperature: −40 to + 125 °C						
Package	LQFP64	LQFP64 WLCSP64 +2	LQFP6 4	LQFP64 WLCSP6 4+2	LQFP100		LQFP144

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD} , the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).

Table 3. STM32F207xx features and peripheral counts

Peripherals		STM32F207Vx				STM32F207Zx				STM32F207Ix			
Flash memory in Kbytes		256	512	768	1024	256	512	768	1024	256	512	768	1024
SRAM in Kbytes	System (SRAM1+SRAM2)	128 (112+16)											
	Backup	4											
FSMC memory controller		Yes ⁽¹⁾											
Ethernet		Yes											
Timers	General-purpose	10											
	Advanced-control	2											
	Basic	2											
	IWDG	Yes											
	WWDG	Yes											
RTC		Yes											
Random number generator		Yes											

3.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All STM32F20x products embed:

- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

The content of this area is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes
The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to [Figure 19: Power supply scheme](#) and [Table 16: VCAP1/VCAP2 operating conditions](#).

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

The two 2.2 μ F ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to [Figure 19: Power supply scheme](#).

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS} . On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD} .

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see [Table 5](#) for differences).

TIM2, TIM3, TIM4, TIM5

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

TIM12, TIM13 and TIM14

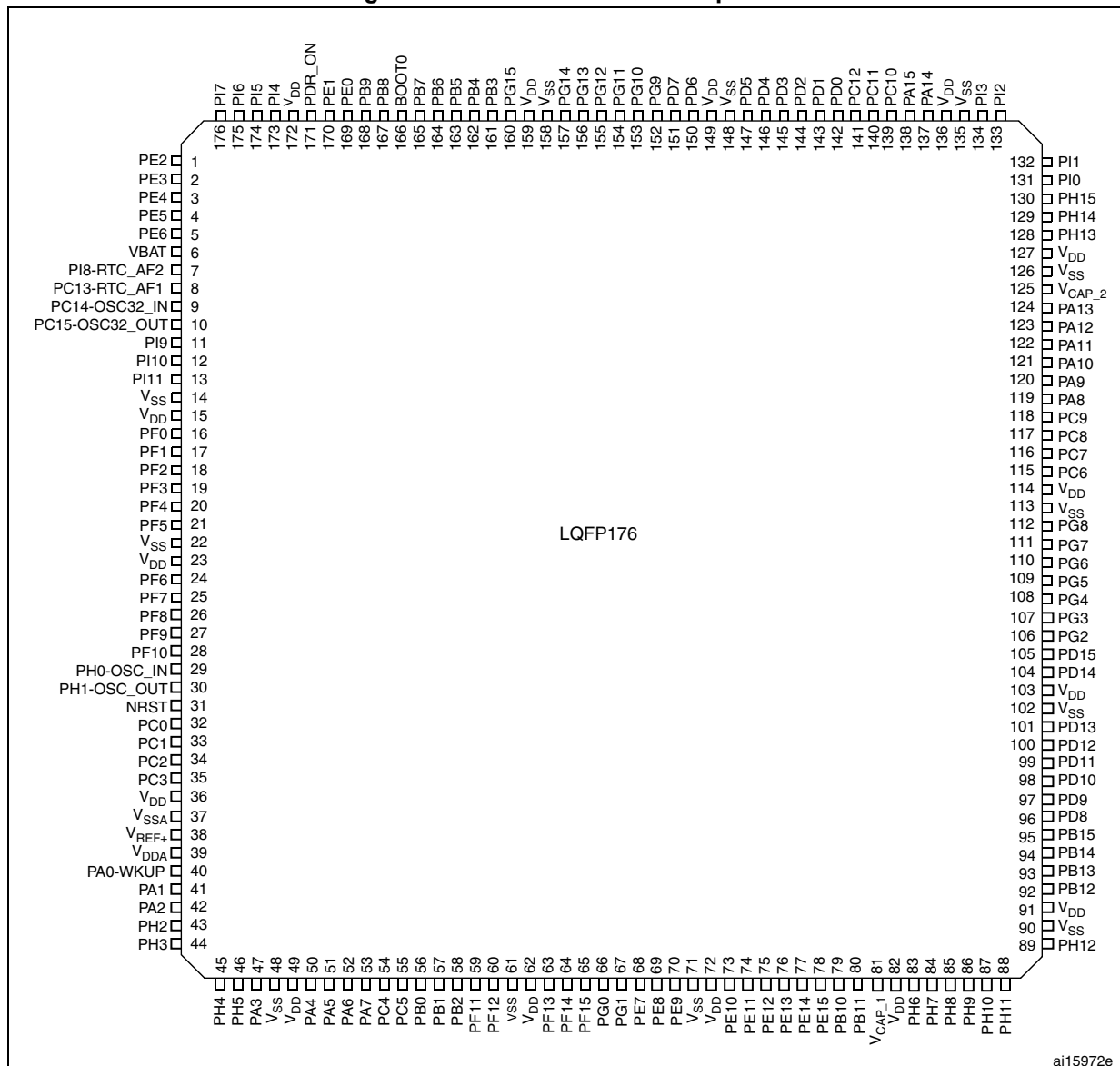
These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

Figure 14. STM32F20x LQFP176 pinout



ai15972e

1. RFU means "reserved for future use". This pin can be tied to V_{DD}, V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	38	58	68	R8	PE7	I/O	FT	-	FSMC_D4,TIM1_ETR, EVENTOUT	-
-	-	39	59	69	P8	PE8	I/O	FT	-	FSMC_D5,TIM1_CH1N, EVENTOUT	-
-	-	40	60	70	P9	PE9	I/O	FT	-	FSMC_D6,TIM1_CH1, EVENTOUT	-
-	-	-	61	71	M9	V _{SS}	S		-	-	-
-	-	-	62	72	N9	V _{DD}	S		-	-	-
-	-	41	63	73	R9	PE10	I/O	FT	-	FSMC_D7,TIM1_CH2N, EVENTOUT	-
-	-	42	64	74	P10	PE11	I/O	FT	-	FSMC_D8,TIM1_CH2, EVENTOUT	-
-	-	43	65	75	R10	PE12	I/O	FT	-	FSMC_D9,TIM1_CH3N, EVENTOUT	-
-	-	44	66	76	N11	PE13	I/O	FT	-	FSMC_D10,TIM1_CH3, EVENTOUT	-
-	-	45	67	77	P11	PE14	I/O	FT	-	FSMC_D11,TIM1_CH4, EVENTOUT	-
-	-	46	68	78	R11	PE15	I/O	FT	-	FSMC_D12,TIM1_BKIN, EVENTOUT	-
29	H3	47	69	79	R12	PB10	I/O	FT	-	SPI2_SCK, I2S2_SCK, I2C2_SCL,USART3_TX,OT G_HS_ULPI_D3,ETH_MII_R X_ER,TIM2_CH3, EVENTOUT	-
30	J2	48	70	80	R13	PB11	I/O	FT	-	I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_RMII_TX_EN, ETH_MII_TX_EN, TIM2_CH4, EVENTOUT	-
31	J3	49	71	81	M10	V _{CAP_1}	S		-	-	-
32	-	50	72	82	N10	V _{DD}	S		-	-	-
-	-	-	-	83	M11	PH6	I/O	FT	-	I2C2_SMBA, TIM12_CH1, ETH_MII_RXD2, EVENTOUT	-



Table 10. Alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port A	PA0-WKUP	-	TIM2_CH1_ETR	TIM5_CH1	TIM8_ETR	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	-	EVENTOUT
	PA4	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	-	EVENTOUT
	PA5	-	TIM2_CH1_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	DCMI_PIXCK	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1 TIM2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-	-	-	-	-	-	-	EVENTOUT

6.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 19](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}^{(1)}$	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

[Table 65](#) gives the list of Ethernet MAC signals for MII and [Figure 50](#) shows the corresponding timing diagram.

Figure 51. Ethernet MII timing diagram

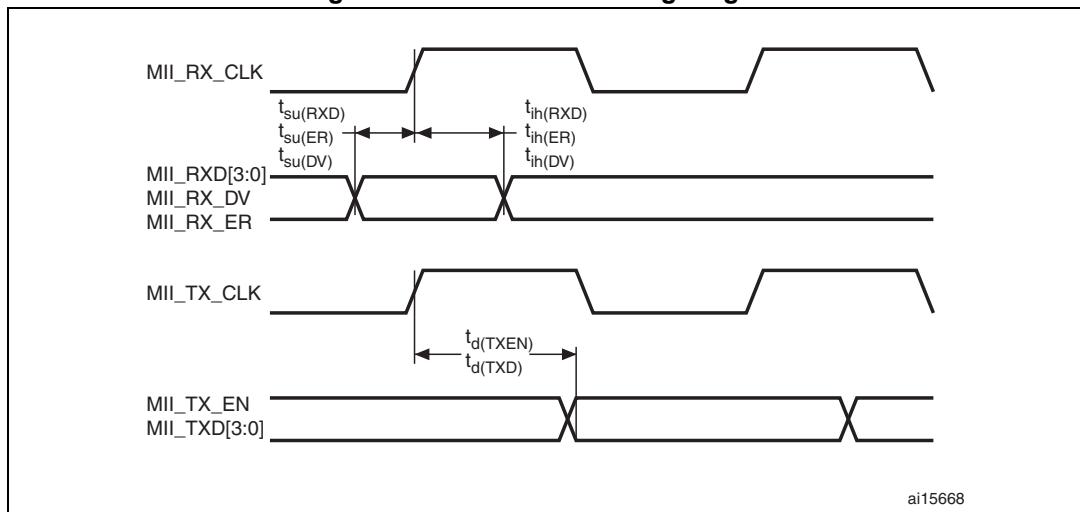


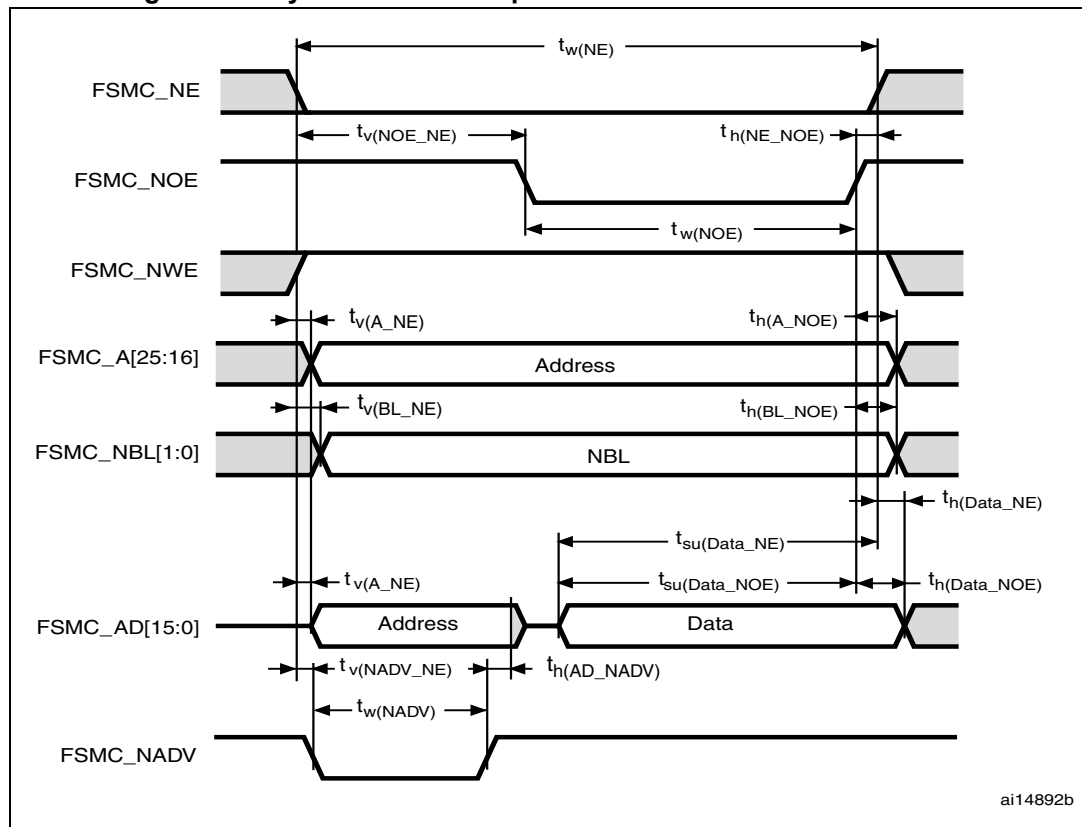
Table 65. Dynamics characteristics: Ethernet MAC signals for MII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	7.5	-	-	ns
$t_{oh}(RXD)$	Receive data hold time	1	-	-	ns
$t_{su}(DV)$	Data valid setup time	4	-	-	ns
$t_{oh}(DV)$	Data valid hold time	0	-	-	ns
$t_{su}(ER)$	Error setup time	3.5	-	-	ns
$t_{oh}(ER)$	Error hold time	0	-	-	ns
$t_d(TXEN)$	Transmit enable valid delay time	-	11	14	ns
$t_d(TXD)$	Transmit data valid delay time	-	11	14	ns

CAN (controller area network) interface

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANTX and CANRX).

Figure 59. Asynchronous multiplexed PSRAM/NOR read waveforms

Table 74. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}-1$	$3T_{HCLK}+1$	ns
$t_{v(NOE_NE)}$	FSMC_NEx low to FSMC_NOE low	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$T_{HCLK}-1$	$T_{HCLK}+1$	ns
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	2	ns
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK}-1.5$	T_{HCLK}	ns
$t_{h(AD_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high	T_{HCLK}	-	ns
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}	-	ns
$t_{h(BL_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	ns
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1	ns
$t_{su(Data_NE)}$	Data to FSMC_NEx high setup time	$T_{HCLK}+2$	-	ns
$t_{su(Data_NOE)}$	Data to FSMC_NOE high setup time	$T_{HCLK}+3$	-	ns

Table 75. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK} - 0.5$	-	ns
$t_{h(BL_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 1$	-	ns
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{v(Data_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK} + 2$	ns
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} - 0.5$	-	ns

1. $C_L = 30$ pF.

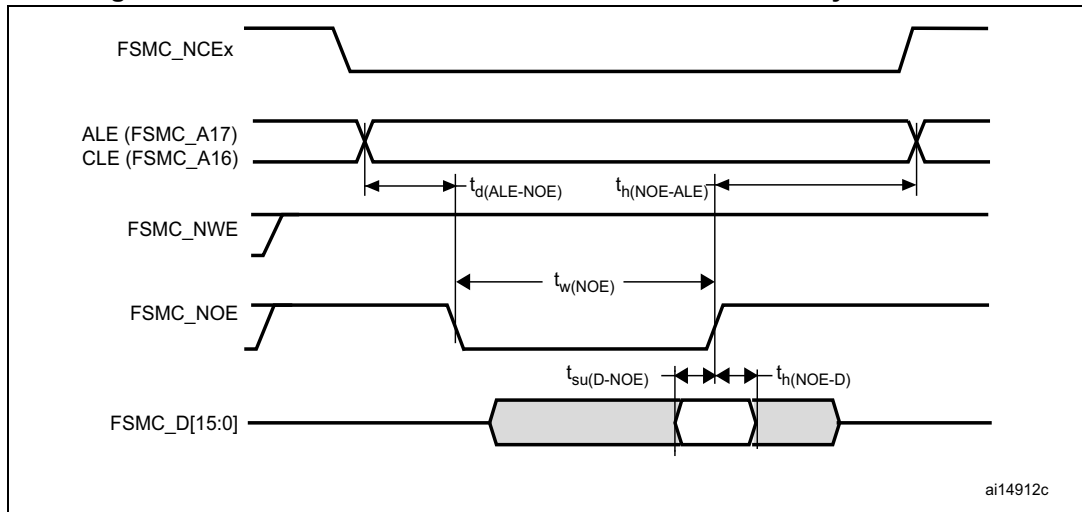
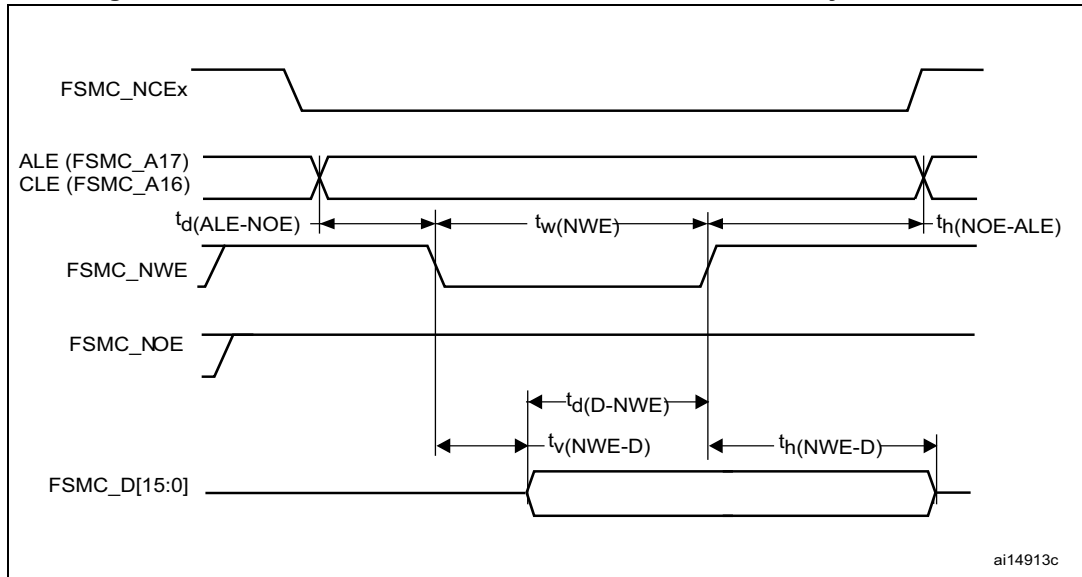
2. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

[Figure 61](#) through [Figure 64](#) represent synchronous waveforms, and [Table 77](#) through [Table 79](#) provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 73. NAND controller waveforms for common memory read access**Figure 74. NAND controller waveforms for common memory write access****Table 82. Switching characteristics for NAND Flash read cycles⁽¹⁾⁽²⁾**

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FSMC_NOE low width	$4T_{HCLK} - 1$	$4T_{HCLK} + 2$	ns
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	9	-	ns
$t_{h(NOE-D)}$	FSMC_D[15:0] valid data after FSMC_NOE high	3	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$3T_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK} + 2$	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results, not tested in production.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Technical drawing of a 12.7mm square grid. The grid is 12.7mm wide and 12.7mm high. The grid is divided into four quadrants by a vertical center line and a horizontal center line. The grid is composed of 16 columns and 16 rows of squares. The columns are numbered 1 to 16 from left to right, and the rows are numbered 1 to 16 from bottom to top. The grid is labeled with dimensions and coordinates. The overall width is 12.7mm, and the overall height is 12.7mm. The grid is divided into four quadrants by a vertical center line and a horizontal center line. The grid is composed of 16 columns and 16 rows of squares. The columns are numbered 1 to 16 from left to right, and the rows are numbered 1 to 16 from bottom to top. The grid is labeled with dimensions and coordinates. The overall width is 12.7mm, and the overall height is 12.7mm. The grid is divided into four quadrants by a vertical center line and a horizontal center line. The grid is composed of 16 columns and 16 rows of squares. The columns are numbered 1 to 16 from left to right, and the rows are numbered 1 to 16 from bottom to top. The grid is labeled with dimensions and coordinates. The overall width is 12.7mm, and the overall height is 12.7mm.

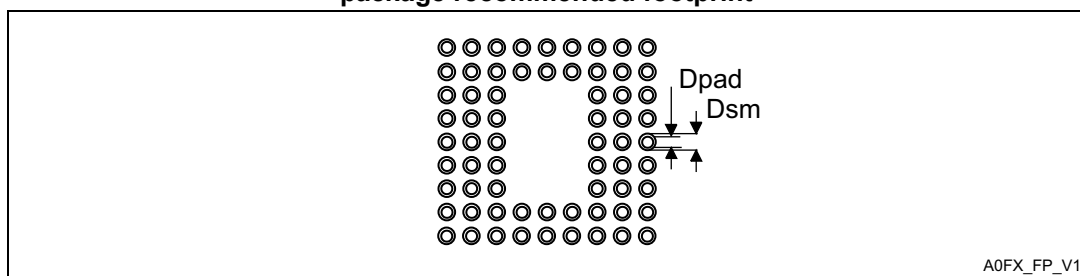
1. Dimensions are expressed in millimeters.

Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
F	-	0.220	-	-	0.0087	-
G	-	0.386	-	-	0.0152	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

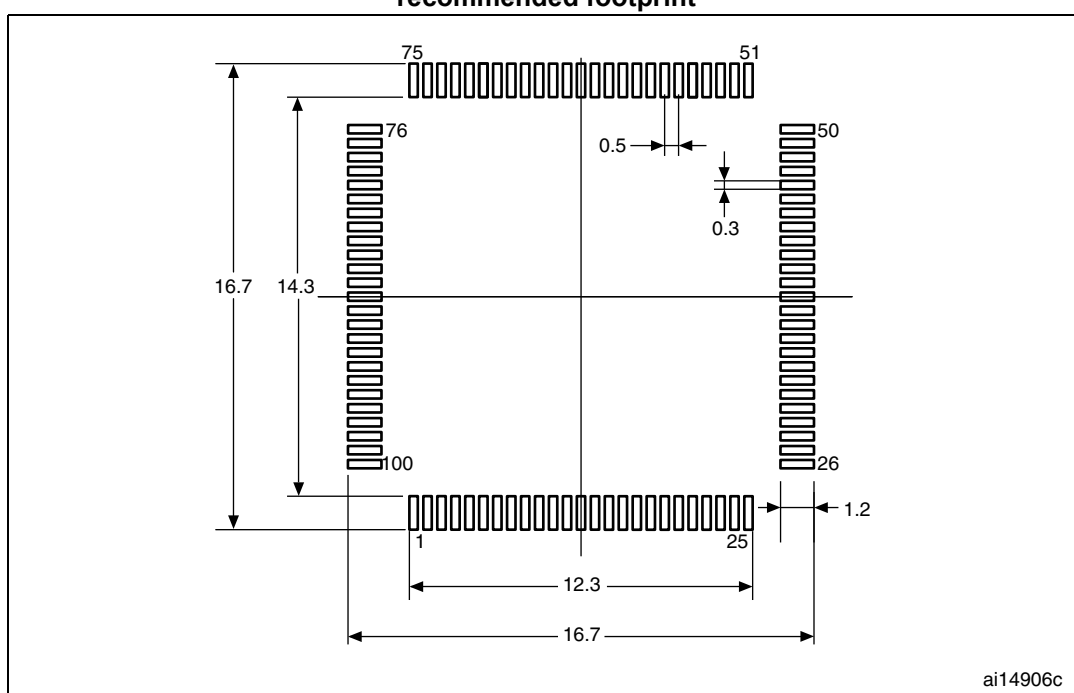
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 80. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**Table 89. WLCSP64 recommended PCB design rules (0.4 mm pitch)**

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

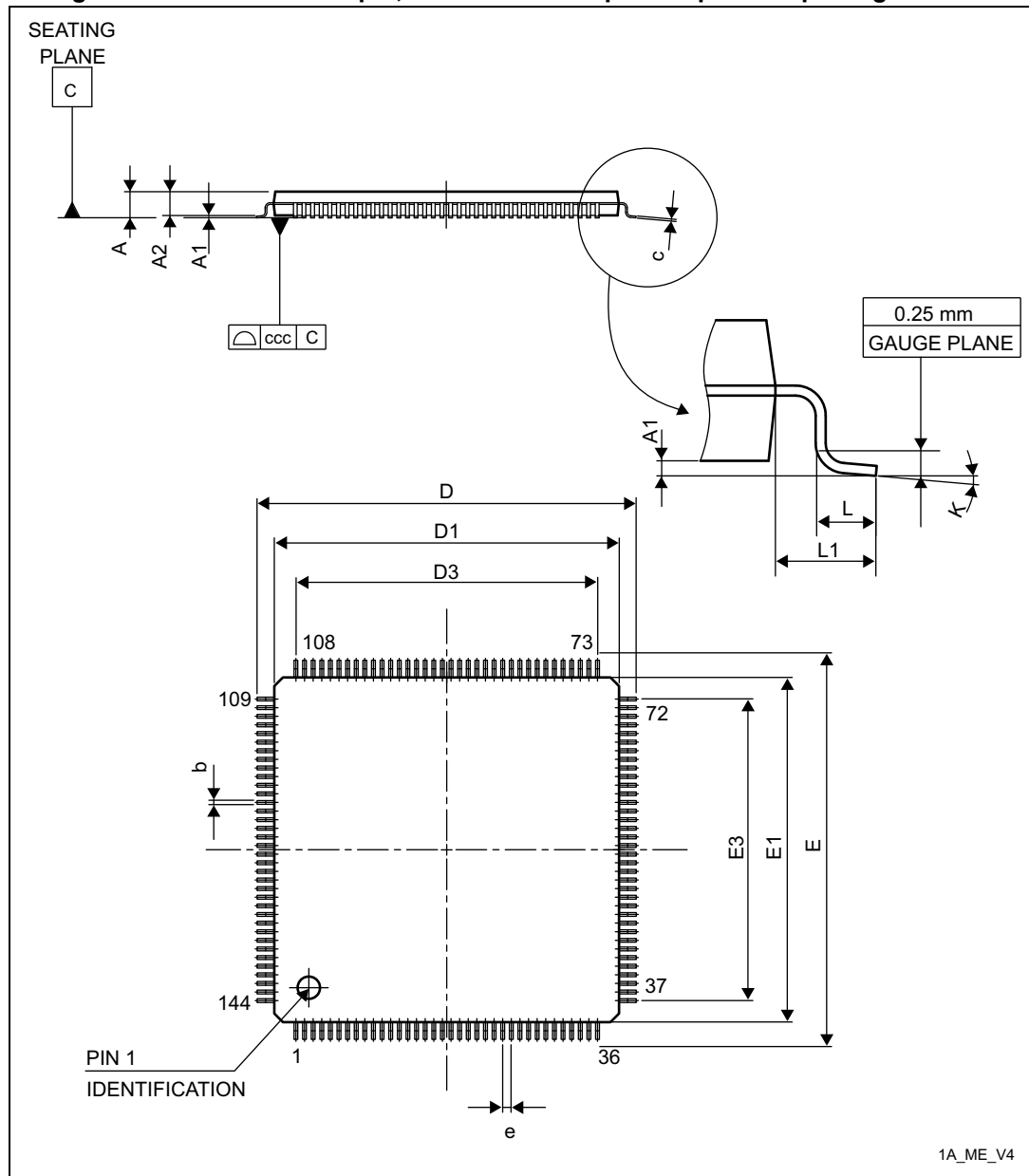
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



7.4 LQFP144 package information

Figure 84. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 91. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Part numbering

Table 96. Ordering information scheme

Example:	STM32	F	205	R	E	T	6	Vxxx
Device family								
STM32 = ARM-based 32-bit microcontroller								
Product type								
F = general-purpose								
Device subfamily								
205 = STM32F20x, connectivity 207= STM32F20x, connectivity, camera interface, Ethernet								
Pin count								
R = 64 pins or 66 pins ⁽¹⁾ V = 100 pins Z = 144 pins I = 176 pins								
Flash memory size								
B = 128 Kbytes of Flash memory C = 256 Kbytes of Flash memory E = 512 Kbytes of Flash memory F = 768 Kbytes of Flash memory G = 1024 Kbytes of Flash memory								
Package								
T = LQFP H = UFBGA Y = WLCSP								
Temperature range								
6 = Industrial temperature range, –40 to 85 °C. 7 = Industrial temperature range, –40 to 105 °C.								
Software option								
Internal code or Blank								
Options								
xxx = programmed parts TR = tape and reel								

1. The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 97. Document revision history (continued)

Date	Revision	Changes
25-Nov-2010	5	<p>Update I/Os in Section : Features.</p> <p>Added WLCSP64+2 package. Added note 1 related to LQFP176 on cover page.</p> <p>Added trademark for ART accelerator. Updated Section 3.2: Adaptive real-time memory accelerator (ART Accelerator™).</p> <p>Updated Figure 5: Multi-AHB matrix.</p> <p>Added case of BOR inactivation using IRROFF on WLCSP devices in Section 3.15: Power supply supervisor.</p> <p>Reworked Section 3.16: Voltage regulator to clarify regulator off modes. Renamed PDROFF, IRROFF in the whole document.</p> <p>Added Section 3.19: VBAT operation.</p> <p>Updated LIN and IrDA features for UART4/5 in Table 6: USART feature comparison.</p> <p>Table 8: STM32F20x pin and ball definitions: Modified V_{DD_3} pin, and added note related to the FSMC_NL pin; renamed BYPASS-REG REGOFF, and add IRROFF pin; renamed USART4/5 UART4/5. USART4 pins renamed UART4.</p> <p>Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use.</p> <p>Updated maximum HSE crystal frequency to 26 MHz.</p> <p>Section 6.2: Absolute maximum ratings: Updated V_{IN} minimum and maximum values and note related to five-volt tolerant inputs in Table 11: Voltage characteristics. Updated I_{INJ(PIN)} maximum values and related notes in Table 12: Current characteristics.</p> <p>Updated V_{DDA} minimum value in Table 14: General operating conditions.</p> <p>Added Note 2 and updated Maximum CPU frequency in Table 15: Limitations depending on the operating power supply range, and added Figure 21: Number of wait states versus fCPU and VDD range.</p> <p>Added brownout level 1, 2, and 3 thresholds in Table 19: Embedded reset and power control block characteristics.</p> <p>Changed f_{OSC_IN} maximum value in Table 30: HSE 4-26 MHz oscillator characteristics.</p> <p>Changed f_{PLL_IN} maximum value in Table 34: Main PLL characteristics, and updated jitter parameters in Table 35: PLLI2S (audio PLL) characteristics.</p> <p>Section 6.3.16: I/O port characteristics: updated V_{IH} and V_{IL} in Table 48: I/O AC characteristics.</p> <p>Added Note 1 below Table 47: Output voltage characteristics.</p> <p>Updated R_{PD} and R_{PU} parameter description in Table 57: USB OTG FS DC electrical characteristics.</p> <p>Updated V_{REF+} minimum value in Table 66: ADC characteristics.</p> <p>Updated Table 71: Embedded internal reference voltage.</p> <p>Removed Ethernet and USB2 for 64-pin devices in Table 101: Main applications versus package for STM32F2xxx microcontrollers.</p> <p>Added A.2: USB OTG full speed (FS) interface solutions, removed “OTG FS connection with external PHY” figure, updated Figure 87, Figure 88, and Figure 90 to add STULPI01B.</p>