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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205rgt7

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

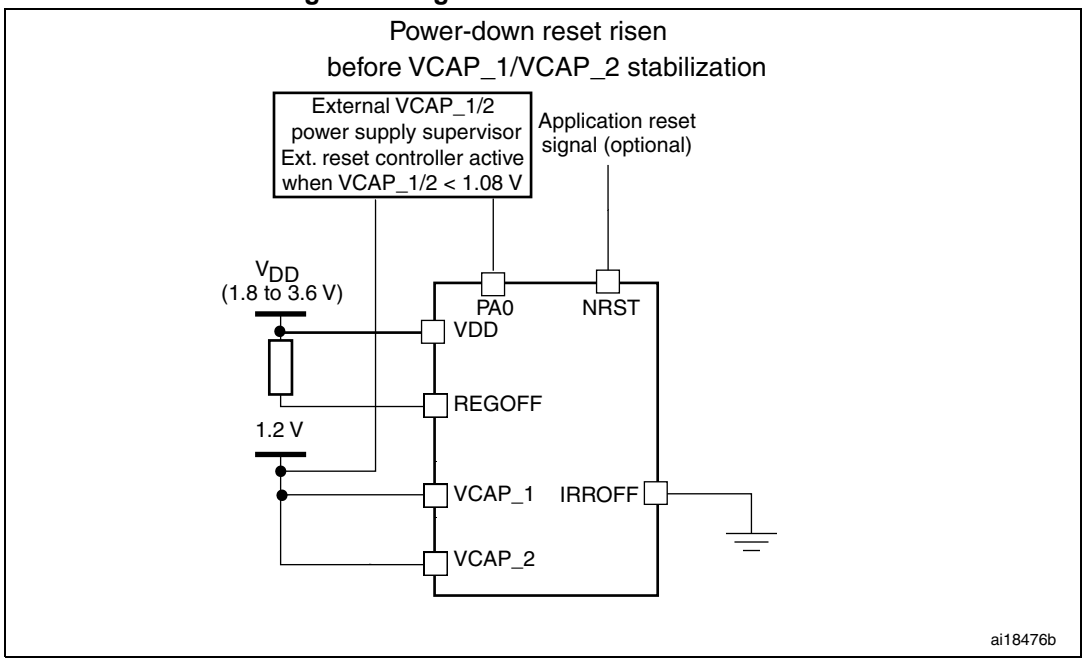
For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

Table 3. STM32F207xx features and peripheral counts (continued)

Peripherals		STM32F207Vx	STM32F207Zx	STM32F207Ix
Comm. interfaces	SPI/(I^2S)	3/(2)[2]		
	I^2C	3		
	USART UART	4 2		
	USB OTG FS	Yes		
	USB OTG HS	Yes		
	CAN	2		
Camera interface		Yes		
GPIOs		82	114	140
SDIO		Yes		
12-bit ADC Number of channels		3		
		16	24	24
12-bit DAC Number of channels		Yes 2		
Maximum CPU frequency		120 MHz		
Operating voltage		1.8 V to 3.6 V[3]		
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C		
		Junction temperature: –40 to + 125 °C		
Package		LQFP100	LQFP144	LQFP176/ UFBGA176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

Figure 6. Regulator OFF/internal reset ON



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 8*).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD}. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

Table 6. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	1.87	7.5	APB2 (max. 60 MHz)
USART2	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
USART3	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
UART4	X	-	X	-	X	-	1.87	3.75	APB1 (max. 30 MHz)
UART5	X	-	X	-	X	-	3.75	3.75	APB1 (max. 30 MHz)
USART6	X	X	X	X	X	X	3.75	7.5	APB2 (max. 60 MHz)

3.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.24 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx interfaces can be served by the DMA controller.

3.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

3.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.31 Digital camera interface (DCMI)

The camera interface is not available in STM32F205xx devices.

STM32F207xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.32 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

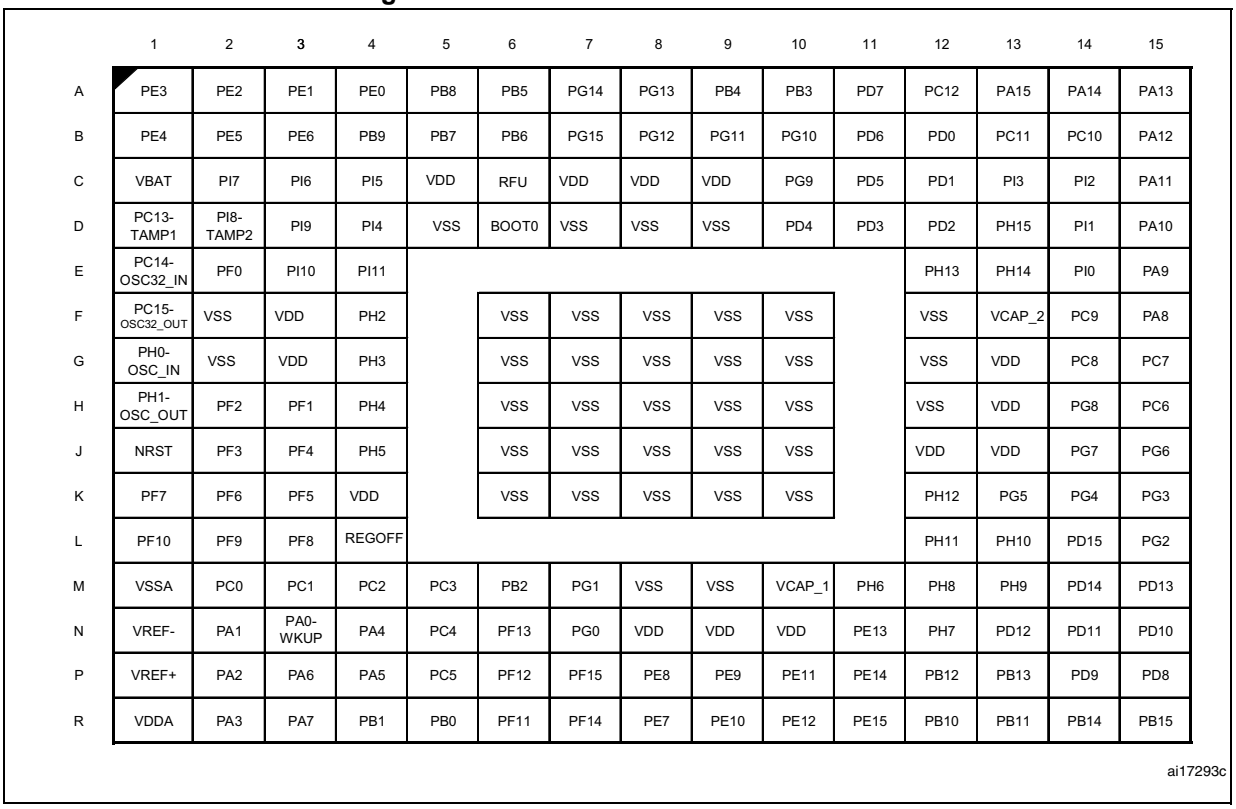
3.33 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

Figure 15. STM32F20x UFBGA176 ballout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	RFU	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13-TAMP1	PI8-TAMP2	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP_2	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	REGOFF								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0-WKUP	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

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1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	56	78	97	P14	PD9	I/O	FT	-	FSMC_D14, USART3_RX, EVENTOUT	-
-	-	57	79	98	N15	PD10	I/O	FT	-	FSMC_D15, USART3_CK, EVENTOUT	-
-	-	58	80	99	N14	PD11	I/O	FT	-	FSMC_A16,USART3_CTS, EVENTOUT	-
-	-	59	81	100	N13	PD12	I/O	FT	-	FSMC_A17,TIM4_CH1, USART3_RTS, EVENTOUT	-
-	-	60	82	101	M15	PD13	I/O	FT	-	FSMC_A18,TIM4_CH2, EVENTOUT	-
-	-	-	83	102	-	V_{SS}	S	-	-	-	-
-	-	-	84	103	J13	V_{DD}	S	-	-	-	-
-	-	61	85	104	M14	PD14	I/O	FT	-	FSMC_D0,TIM4_CH3, EVENTOUT	-
-	-	62	86	105	L14	PD15	I/O	FT	-	FSMC_D1,TIM4_CH4, EVENTOUT	-
-	-	-	87	106	L15	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	88	107	K15	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	89	108	K14	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	90	109	K13	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	91	110	J15	PG6	I/O	FT	-	FSMC_INT2, EVENTOUT	-
-	-	-	92	111	J14	PG7	I/O	FT	-	FSMC_INT3 ,USART6_CK, EVENTOUT	-
-	-	-	93	112	H14	PG8	I/O	FT	-	USART6_RTS, ETH_PPS_OUT, EVENTOUT	-
-	-	-	94	113	G12	V_{SS}	S	-	-	-	-
-	-	-	95	114	H13	V_{DD}	S	-	-	-	-
37	G2	63	96	115	H15	PC6	I/O	FT	-	I2S2_MCK, TIM8_CH1, SDIO_D6, USART6_TX, DCMI_D0, TIM3_CH1, EVENTOUT	-

Table 9. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE5	-	A21	A21	-	Yes
PE6	-	A22	A22	-	Yes
PF0	A0	A0	-	-	-
PF1	A1	A1	-	-	-
PF2	A2	A2	-	-	-
PF3	A3	A3	-	-	-
PF4	A4	A4	-	-	-
PF5	A5	A5	-	-	-
PF6	NIORD	-	-	-	-
PF7	NREG	-	-	-	-
PF8	NIOWR	-	-	-	-
PF9	CD	-	-	-	-
PF10	INTR	-	-	-	-
PF12	A6	A6	-	-	-
PF13	A7	A7	-	-	-
PF14	A8	A8	-	-	-
PF15	A9	A9	-	-	-
PG0	A10	A10	-	-	-
PG1	-	A11	-	-	-
PE7	D4	D4	DA4	D4	Yes
PE8	D5	D5	DA5	D5	Yes
PE9	D6	D6	DA6	D6	Yes
PE10	D7	D7	DA7	D7	Yes
PE11	D8	D8	DA8	D8	Yes
PE12	D9	D9	DA9	D9	Yes
PE13	D10	D10	DA10	D10	Yes
PE14	D11	D11	DA11	D11	Yes
PE15	D12	D12	DA12	D12	Yes
PD8	D13	D13	DA13	D13	Yes
PD9	D14	D14	DA14	D14	Yes
PD10	D15	D15	DA15	D15	Yes
PD11	-	A16	A16	CLE	Yes
PD12	-	A17	A17	ALE	Yes

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL		-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	-	-	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	-	-	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	-	-	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INT2	-	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FSMC_INT3	-	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_RTS	-	-	ETH _PPS_OUT	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FSMC_NE2/ FSMC_NCE3	-	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NCE4_1/ FSMC_NE3	-	-	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_TX_EN ETH _RMII_TX_EN	FSMC_NCE4_2	-	-	EVENTOUT
	PG12	-	-	-	-	-	-	-	-	USART6_RTS	-	-	-	FSMC_NE4	-	-	EVENTOUT
	PG13	-	-	-	-	-	-	-	-	UART6_CTS	-	-	ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	-	-	-	USART6_TX	-	-	ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	-	DCMI_D13	-	EVENTOUT

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	120	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	120	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	–5/+0	
	Injected current on any other pin(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	30	
f_{PCLK2}	Internal APB2 clock frequency	-	0	60	

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8(1)	3.6	V
V_{DDA}(2)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(3)	1.8(1)	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP64	-	444	mW
		WLCSP64+2	-	392	
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 26. Peripheral current consumption (continued)

Peripheral[1]		Typical consumption at 25 °C	Unit
APB2	SDIO	0.69	mA
	TIM1	1.06	
	TIM8	1.03	
	TIM9	0.58	
	TIM10	0.37	
	TIM11	0.39	
	ADC1[4]	2.13	
	ADC2[4]	2.04	
	ADC3[4]	2.12	
	SPI1	1.20	
	USART1	0.38	
	USART6	0.37	

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC_CR register.
3. EN2 bit is set in DAC_CR register.
4. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

6.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Unit
$t_{WUSLEEP}$[2]	Wakeup from Sleep mode	-	1	-	µs
t_{WUSTOP}[2]	Wakeup from Stop mode (regulator in Run mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}$[2][3]	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

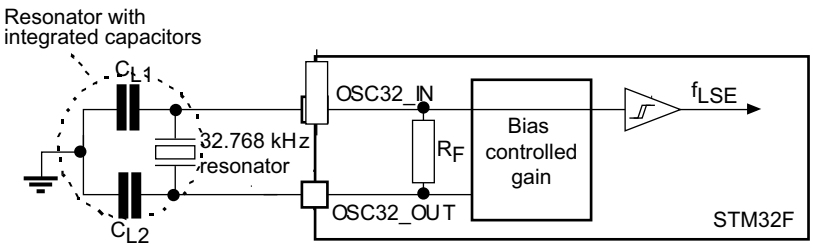
Table 31. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	-	-	-	1	µA
g_m	Oscillator Transconductance	-	2.8	-	-	µA/V
$t_{SU(LSE)}$ (2)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 33. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in *Table 32* and *Table 33* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

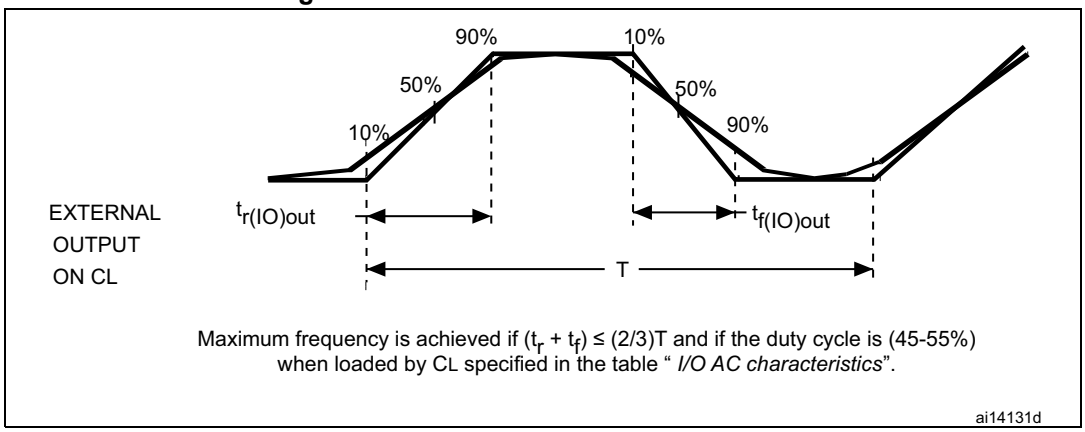
High-speed internal (HSI) RC oscillator

Table 32. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user-trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	– 8	-	4.5	%
		T_A = –10 to 85 °C(3)	– 4	-	4	%
		T_A = 25 °C(4)	– 1	-	1	%
$t_{su(HSI)}$ (2)	HSI oscillator startup time	-	-	2.2	4.0	µs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 39. I/O AC characteristics definition



6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 49*).

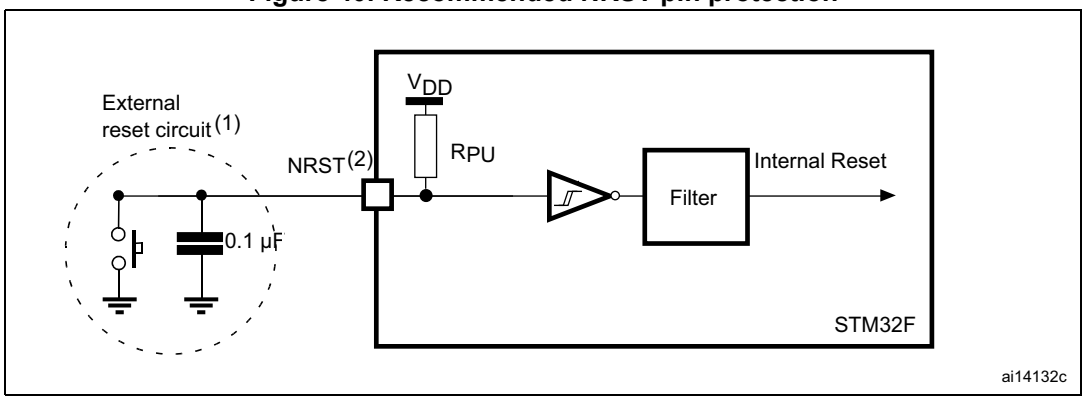
Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design, not tested in production.

Figure 40. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 49*. Otherwise the reset is not taken into account by the device.

Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}– 0.5	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}- 1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK}+2	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}– 0.5	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 61 through *Figure 64* represent synchronous waveforms, and *Table 77* through *Table 79* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 70. PC Card/CompactFlash controller waveforms for I/O space write access

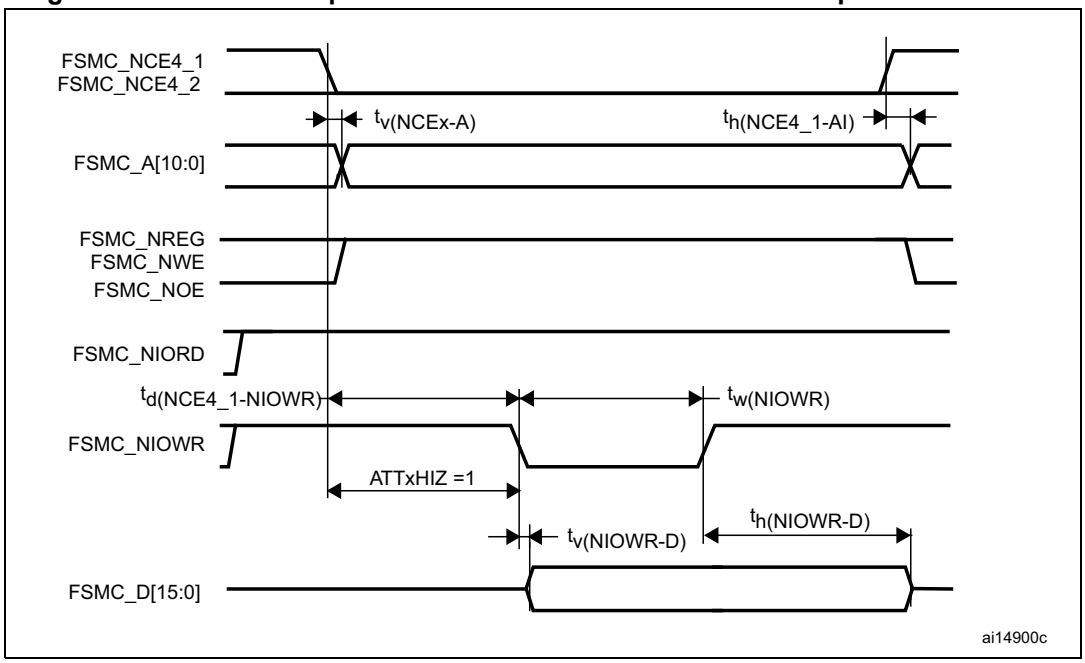


Table 80. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_Ncex low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FSMC_NCEx high to FSMC_Ax invalid	4	-	ns
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	3.5	ns
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	T_{HCLK}+ 4	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK}$+ 1	ns
$t_{d(NCEx-NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5T_{HCLK}$	ns
$t_{w(NOE)}$	FSMC_NOE low width	$8T_{HCLK}$– 0.5	$8T_{HCLK}$+ 1	ns
$t_{d(NOE\_NCEx)}$	FSMC_NOE high to FSMC_NCEx high	$5T_{HCLK}$+ 2.5	-	ns
$t_{su\ (D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	4	-	ns
$t_{h\ (N0E-D)}$	FSMC_N0E high to FSMC_D[15:0] invalid	2	-	ns
$t_{w(NWE)}$	FSMC_NWE low width	$8T_{HCLK}$- 1	$8T_{HCLK}$+ 4	ns
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5T_{HCLK}$+ 1.5	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	5HCLK+ 1	ns
$t_{v\ (NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h\ (NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$8T_{HCLK}$	-	ns
$t_{d\ (D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13T_{HCLK}$	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 71. NAND controller waveforms for read access

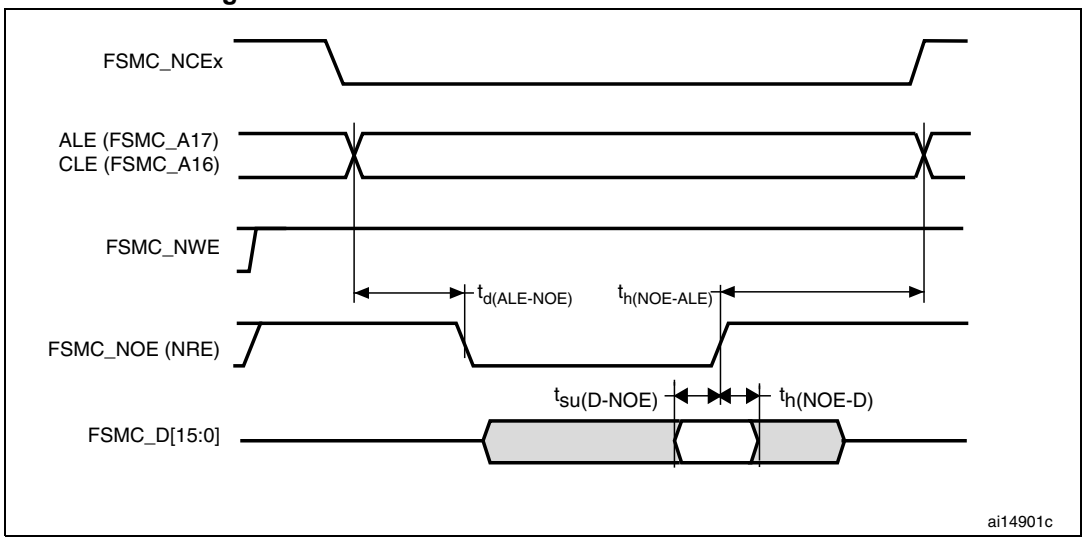


Figure 72. NAND controller waveforms for write access

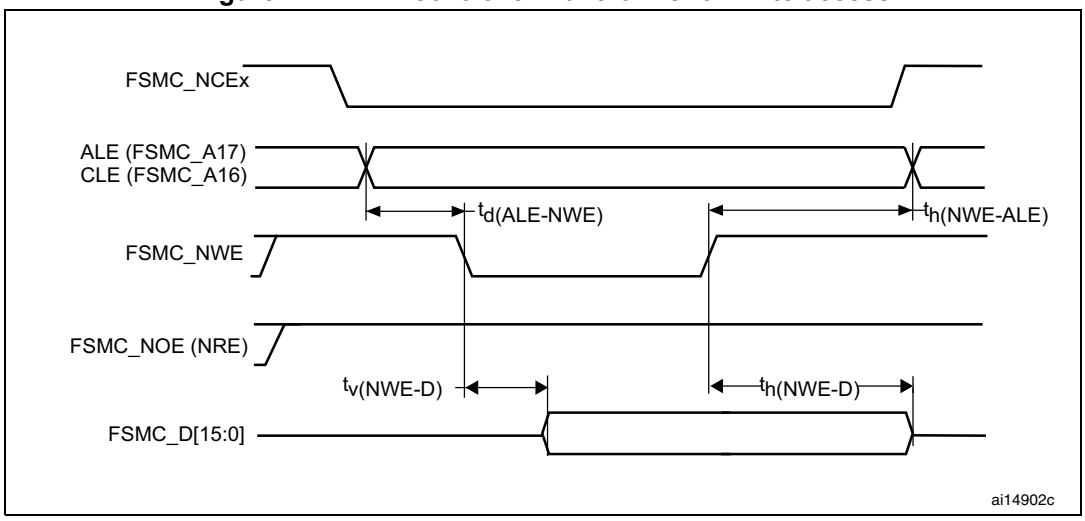
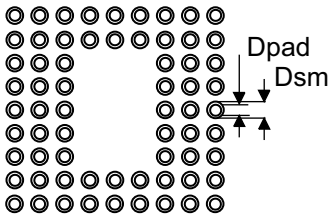


Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.220	-	-	0.0087	-
G	-	0.386	-	-	0.0152	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 80. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



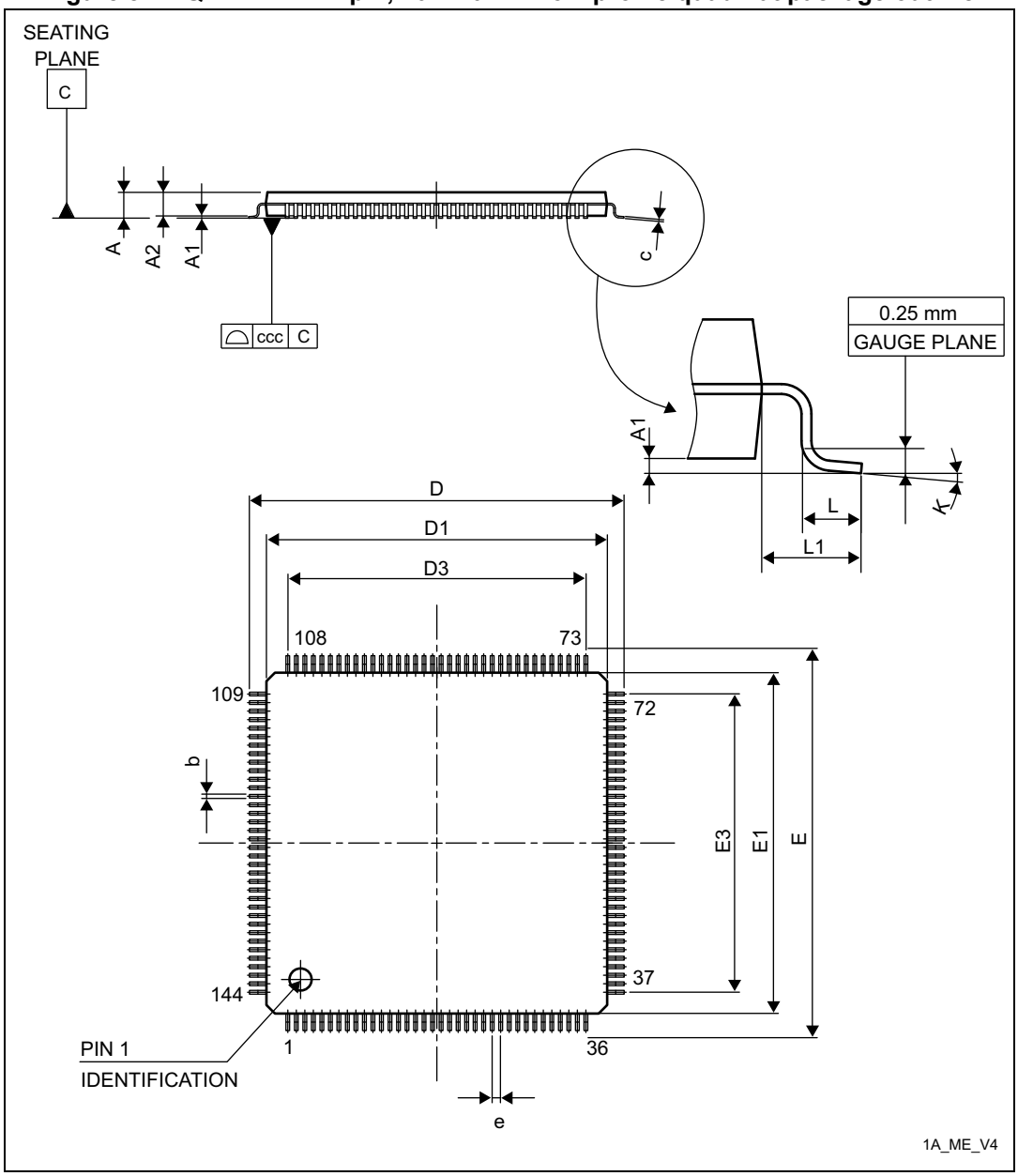
A0FX_FP_V1

Table 89. WLCSP64 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

7.4 LQFP144 package information

Figure 84. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.