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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	100K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vct7

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

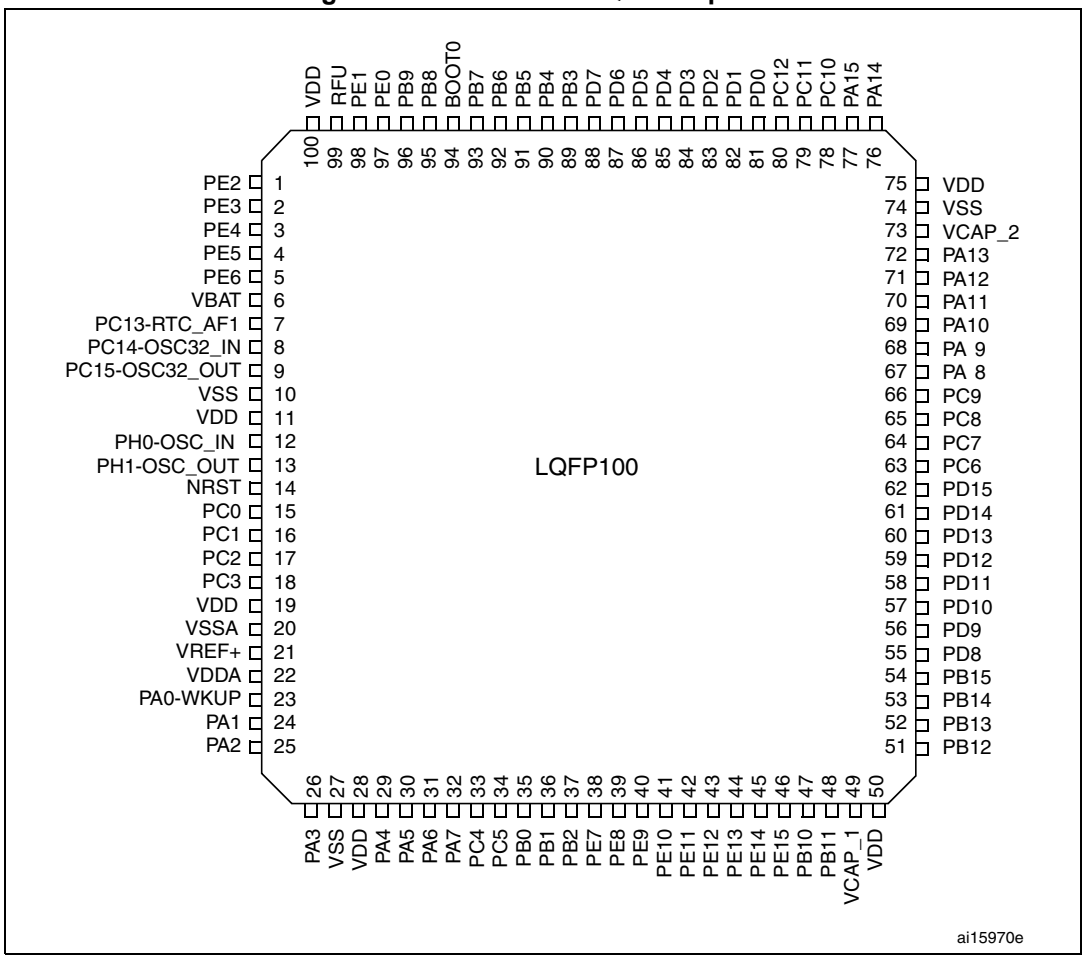
The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

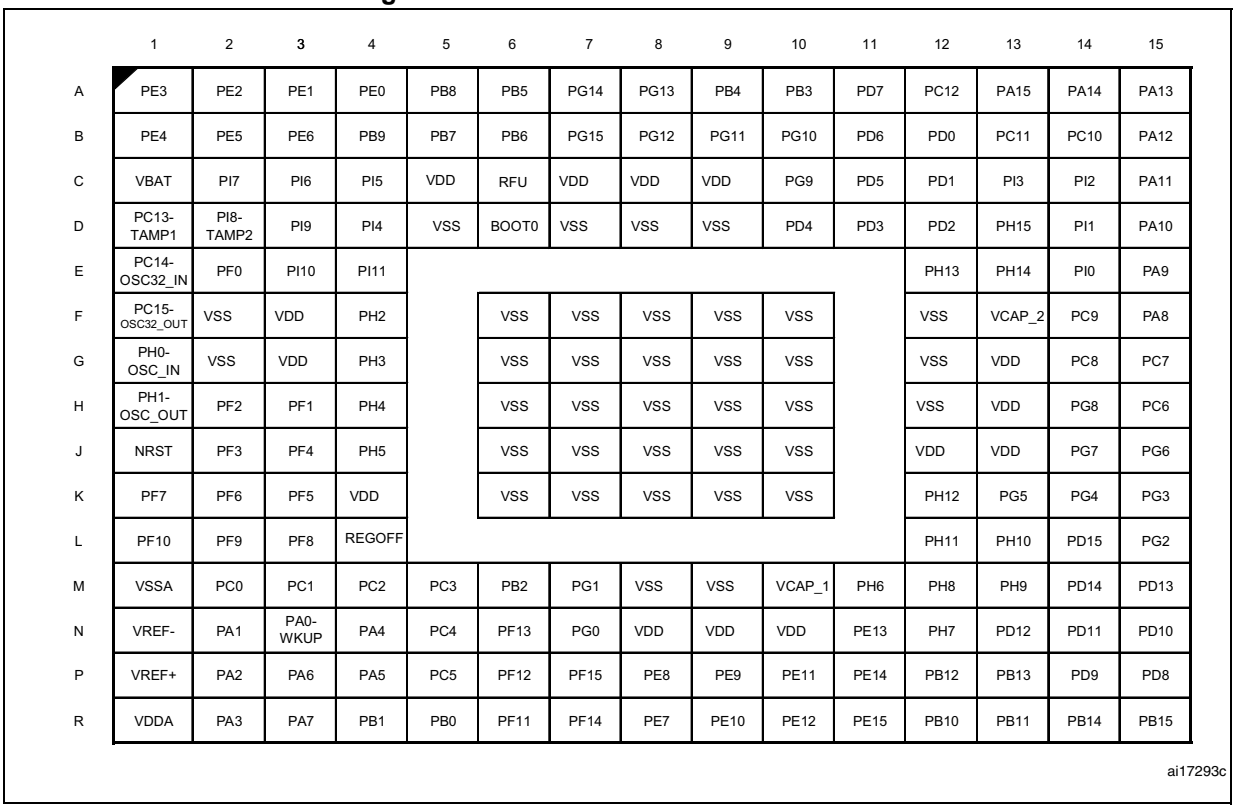
For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

Figure 12. STM32F20x LQFP100 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Figure 15. STM32F20x UFBGA176 ballout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	RFU	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13-TAMP1	PI8-TAMP2	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP_2	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	REGOFF								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0-WKUP	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

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1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

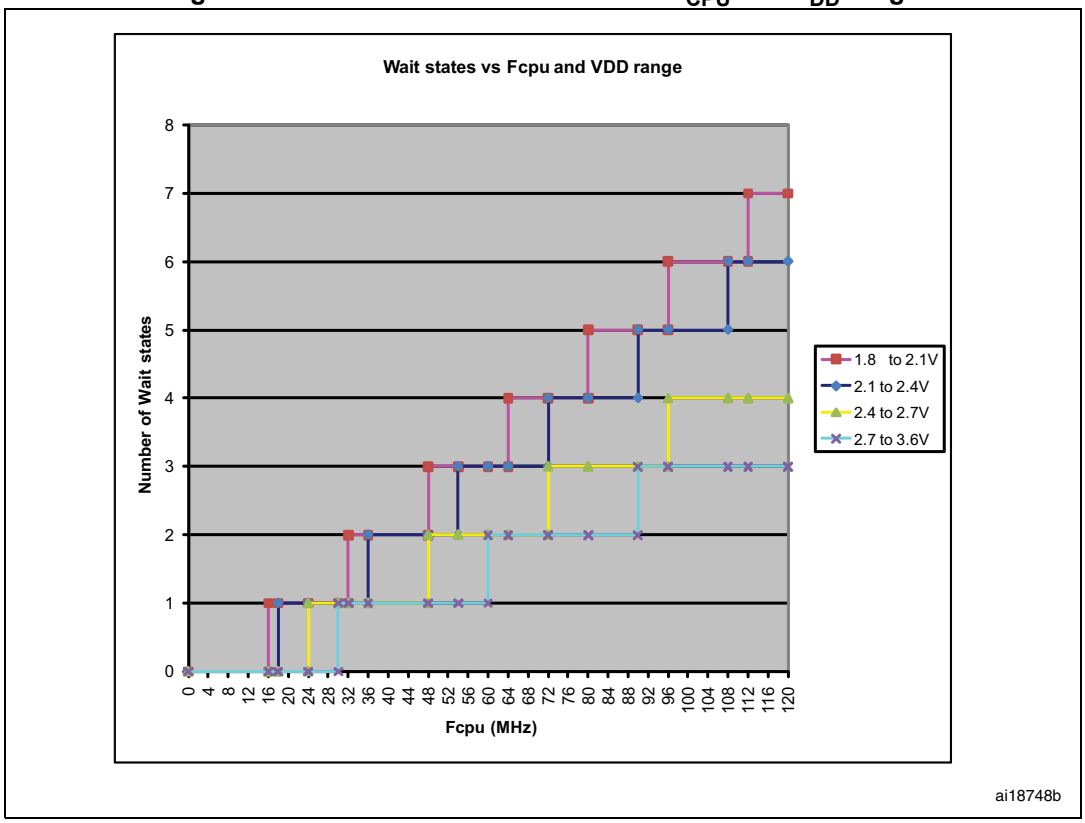
Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)(1)	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(2)	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4(3)	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(3)	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

Figure 21. Number of wait states versus f_{CPU} and V_{DD} range

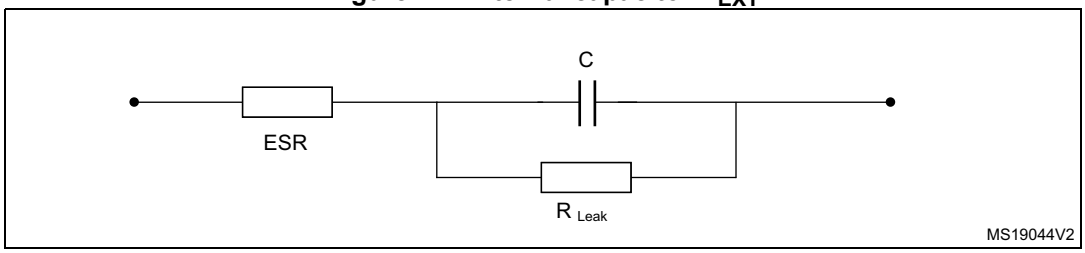


1. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V_{DD}.

6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 16*.

Figure 22. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 16. VCAP1/VCAP2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

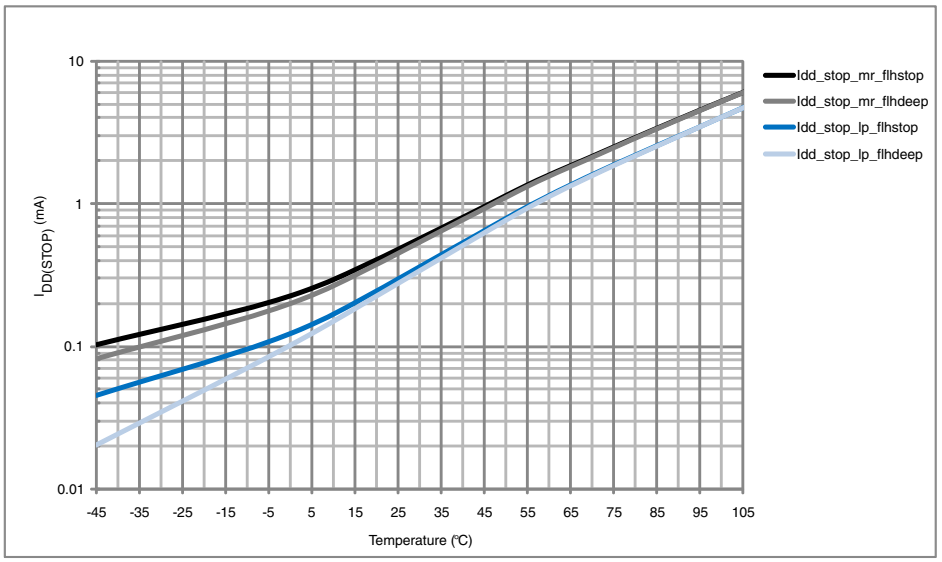
Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled(3)	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz(4)	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock(2), all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz(4)	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Figure 29. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Table 37. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 38. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-2	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 44. SPI timing diagram - master mode

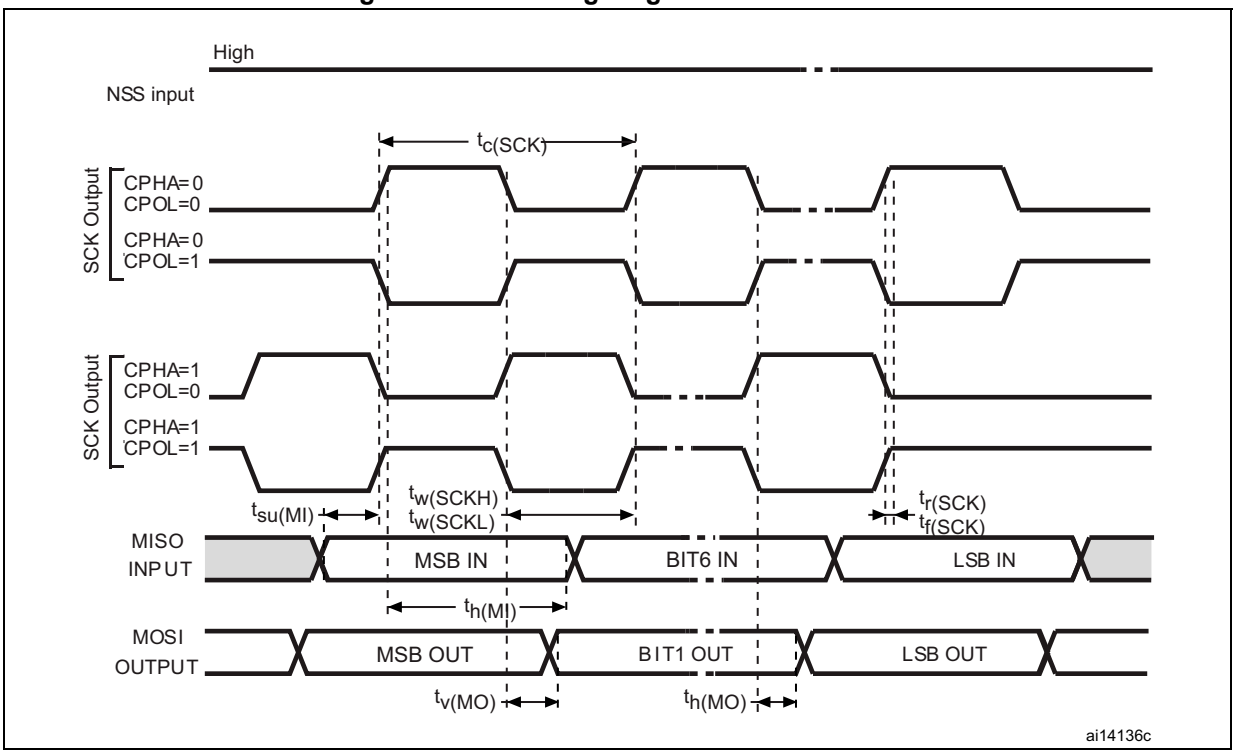


Figure 48. ULPI timing diagram

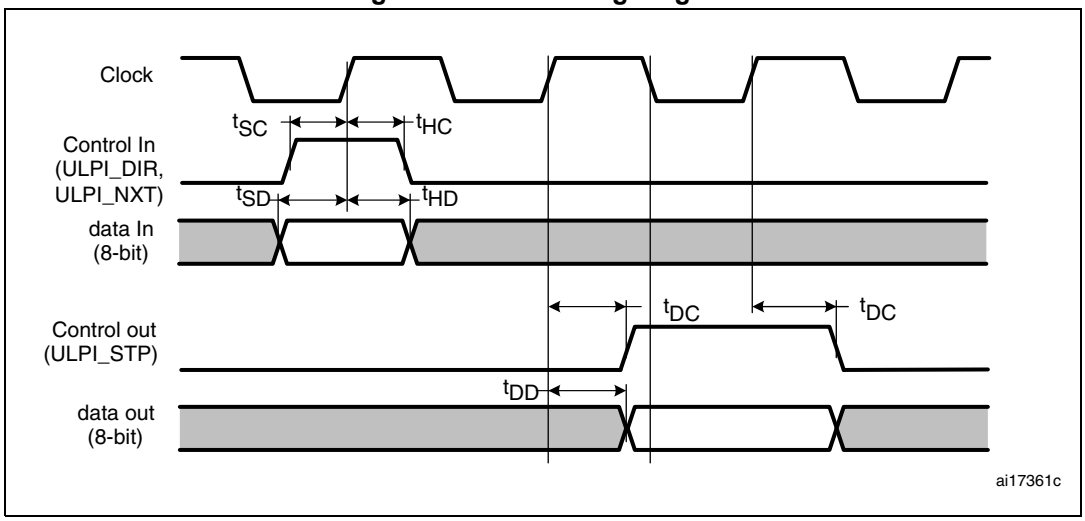


Table 61. ULPI timing

Symbol	Parameter	Value(1)		Unit
		Min.	Max.	
t_{SC}	Control in (ULPI_DIR) setup time	-	2.0	ns
	Control in (ULPI_NXT) setup time	-	1.5	
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0	-	
t_{SD}	Data in setup time	-	2.0	
t_{HD}	Data in hold time	0	-	
t_{DC}	Control out (ULPI_STP) setup time and hold time	-	9.2	
t_{DD}	Data out available from clock rising edge	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Ethernet characteristics

Table 62 shows the Ethernet operating voltage.

Table 62. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 63 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 49* shows the corresponding timing diagram.

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8(1)	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)(2)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(1) to 2.4 V	0.6	-	15	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	-	30	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 30 MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(4)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(3)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(3)(5)	Sampling switch resistance	-	1.5	-	6	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	4	-	pF
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(6)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(6)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	2	3	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.5	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.3	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}– 0.5	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}- 1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK}+2	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}– 0.5	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 61 through *Figure 64* represent synchronous waveforms, and *Table 77* through *Table 79* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 64. Synchronous non-multiplexed PSRAM write timings

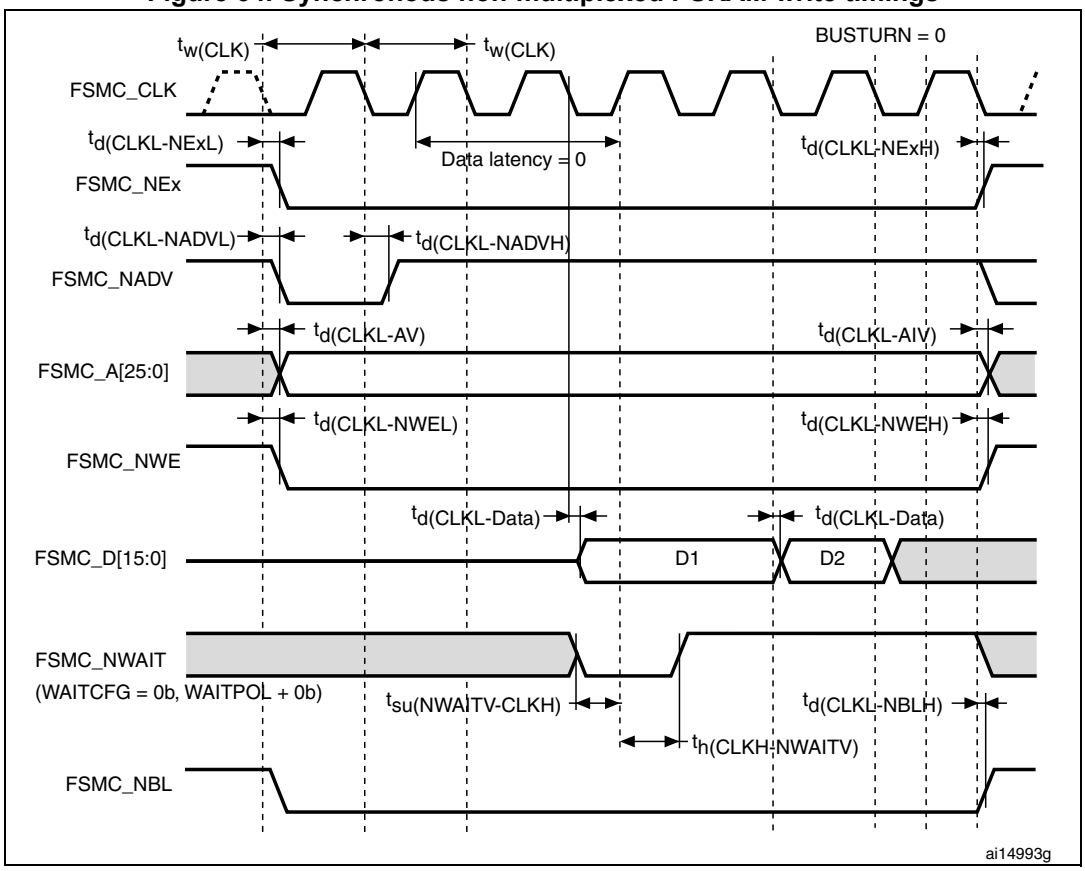
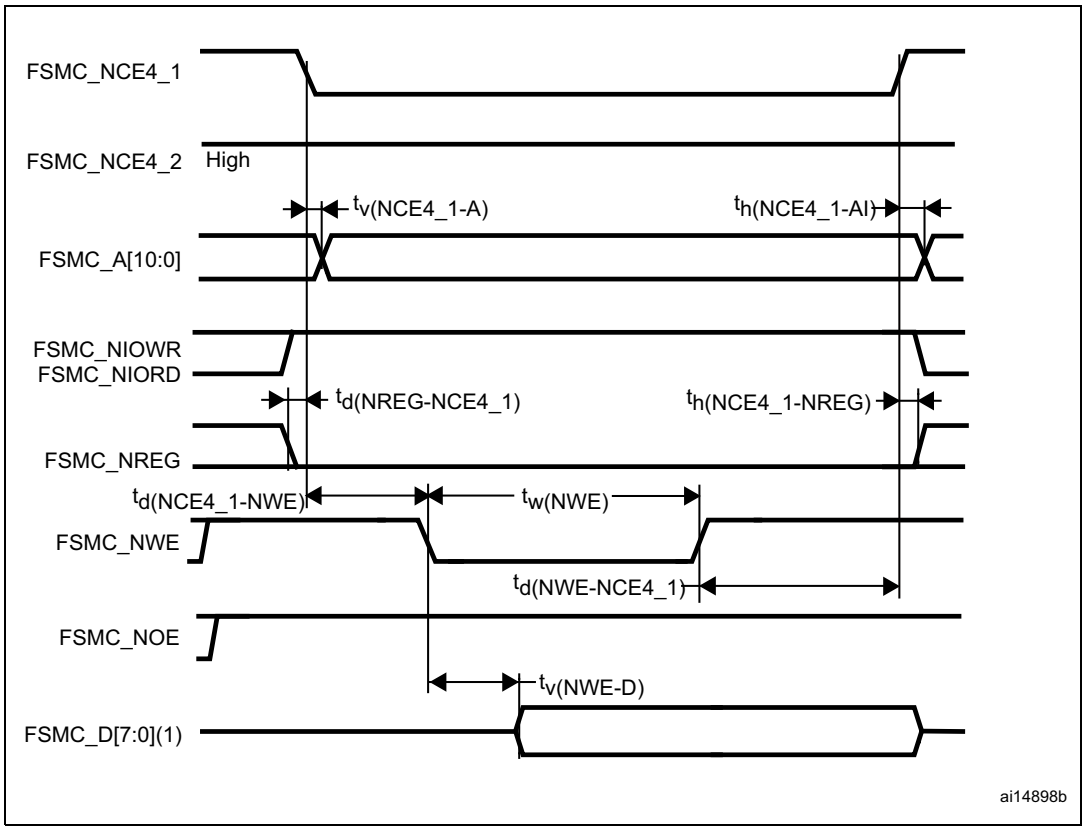


Table 79. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns

Figure 68. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Figure 69. PC Card/CompactFlash controller waveforms for I/O space read access

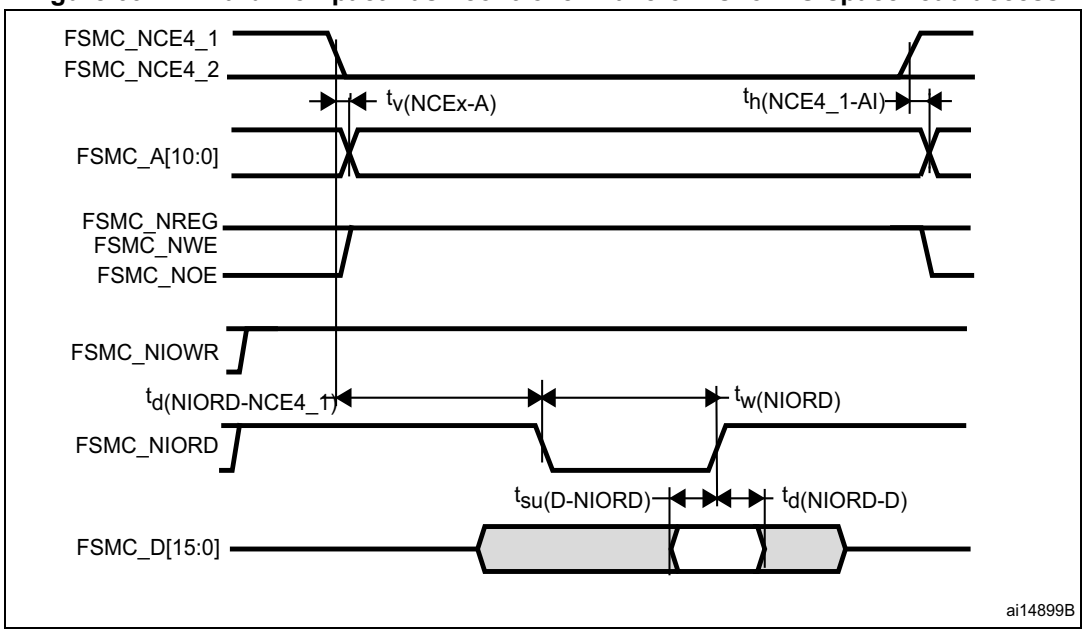


Table 97. Document revision history (continued)

Date	Revision	Changes
20-Dec-2011	8 (continued)	Added maximum power consumption at T_A=25 °C in *Table 23: Typical and maximum current consumptions in Stop mode*. Updated md minimum value in *Table 36: SSCG parameters constraint*. Added examples in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Updated *Table 54: SPI characteristics* and *Table 55: I2S characteristics*. Updated *Figure 48: ULPI timing diagram* and *Table 61: ULPI timing*. Updated *Table 63: Dynamics characteristics: Ethernet MAC signals for SMI*, *Table 64: Dynamics characteristics: Ethernet MAC signals for RMII*, and *Table 65: Dynamics characteristics: Ethernet MAC signals for MII*. *Section 6.3.25: FSMC characteristics*: updated *Table 72* to*Table 83*, changed C_L value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated *Figure 62: Synchronous multiplexed PSRAM write timings*. Updated*Table 84: DCMI characteristics*. Updated *Table 92: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data*. Updated *Table 96: Ordering information scheme*. Appendix *A.2: USB OTG full speed (FS) interface solutions*: updated *Figure 87: USB OTG FS (full speed) host-only connection* and added *Note 2*, updated *Figure 88: OTG FS (full speed) connection dual-role with internal PHY* and added *Note 3* and *Note 4*, modified *Figure 89: OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY* and added *Note 2*. Appendix *A.3: USB OTG high speed (HS) interface solutions*: removed figures *USB OTG HS device-only connection in FS mode* and *USB OTG HS host-only connection in FS mode,* updated *Figure 89: OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY*. Added Appendix *A.4: Ethernet interface solutions*. Updated disclaimer on last page.
24-Apr-2012	9	Updated V_{DD} minimum value in *Section 2: Description*. Updated number of USB OTG HS and FS, modified packages for STM32F207Ix part numbers, added *Note 1* related to FSMC and *Note 2* related to SPI/I2S, and updated *Note 3* in *Table 2: STM32F205xx features and peripheral counts* and *Table 3: STM32F207xx features and peripheral counts*. Added *Note 2* and update TIM5 in *Figure 4: STM32F20x block diagram*. Updated maximum number of maskable interrupts in *Section 3.10: Nested vectored interrupt controller (NVIC)*. Updated V_{DD} minimum value in *Section 3.14: Power supply schemes*. Updated *Note a* in *Section 3.16.1: Regulator ON*. Removed STM32F205xx in *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)*.

Table 97. Document revision history (continued)

Date	Revision	Changes
24-Apr-2012	9 (continued)	Removed support of I2C for OTG PHY in *Section 3.29: Universal serial bus on-the-go high-speed (OTG_HS)*. Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in *Table 8: STM32F20x pin and ball definitions* and *Table 10: Alternate function mapping*. Renamed PH10 alternate function into TIM5_CH1 in *Table 10: Alternate function mapping*. Added *Table 9: FSMC pin definition*. Updated *Note 1* in *Table 14: General operating conditions*, *Note 2* in *Table 15: Limitations depending on the operating power supply range*, and *Note 1* below *Figure 21: Number of wait states versus fCPU and VDD range*. Updated $V_{POR/PDR}$ in *Table 19: Embedded reset and power control block characteristics*. Updated typical values in *Table 24: Typical and maximum current consumptions in Standby mode* and *Table 25: Typical and maximum current consumptions in VBAT mode*. Updated *Table 30: HSE 4-26 MHz oscillator characteristics* and *Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Updated *Table 37: Flash memory characteristics*, *Table 38: Flash memory programming*, and *Table 39: Flash memory programming with VPP*. Updated *Section : Output driving current*. Updated *Note 3* and removed note related to minimum hold time value in *Table 52: I2C characteristics*. Updated *Table 64: Dynamics characteristics: Ethernet MAC signals for RMII*. Updated *Note 1*, C_{ADC}, I_{VREF+}, and I_{VDDA} in *Table 66: ADC characteristics*. Updated *Note 3* and note concerning ADC accuracy vs. negative injection current in *Table 67: ADC accuracy*. Updated *Note 1* in *Table 68: DAC characteristics*. Updated *Section Figure 88.: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*. Appendix *A.1: Main applications versus package*: removed number of address lines for FSMC/NAND in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Appendix *A.4: Ethernet interface solutions*: updated *Figure 92: Complete audio player solution 1* and *Figure 93: Complete audio player solution 2*.