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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vet6

3 Functional overview

3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM® core, the STM32F20x family is compatible with all ARM® tools and software.

Figure 4 shows the general block diagram of the STM32F20x family.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M3 processors. It balances the inherent performance advantage of the ARM® Cortex®-M3 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher operating frequencies.

To release the processor full 150 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.26 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F207xx devices.

The STM32F207xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F207xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F207xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F207xx.

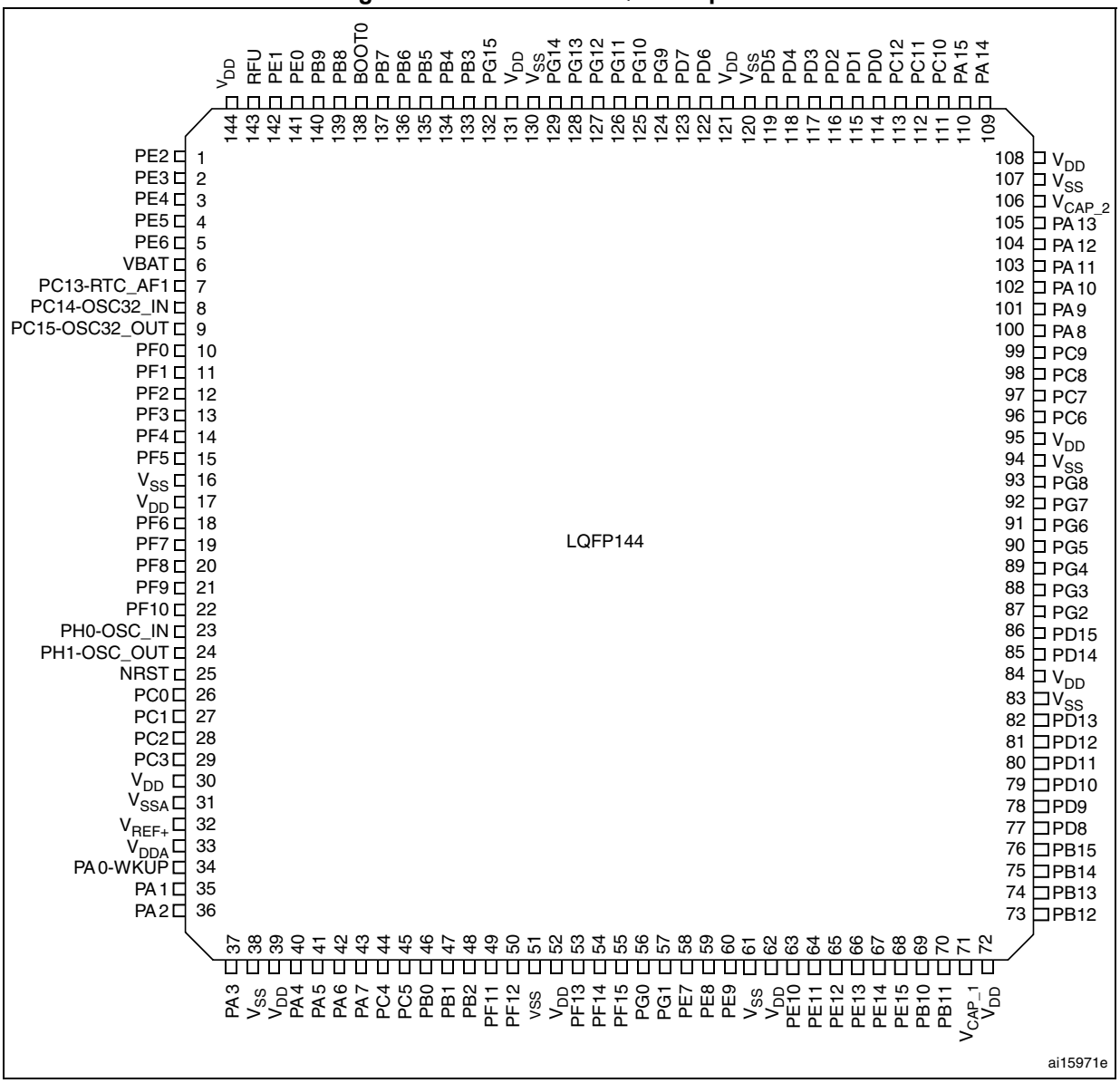
The STM32F207xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.27 Controller area network (CAN)

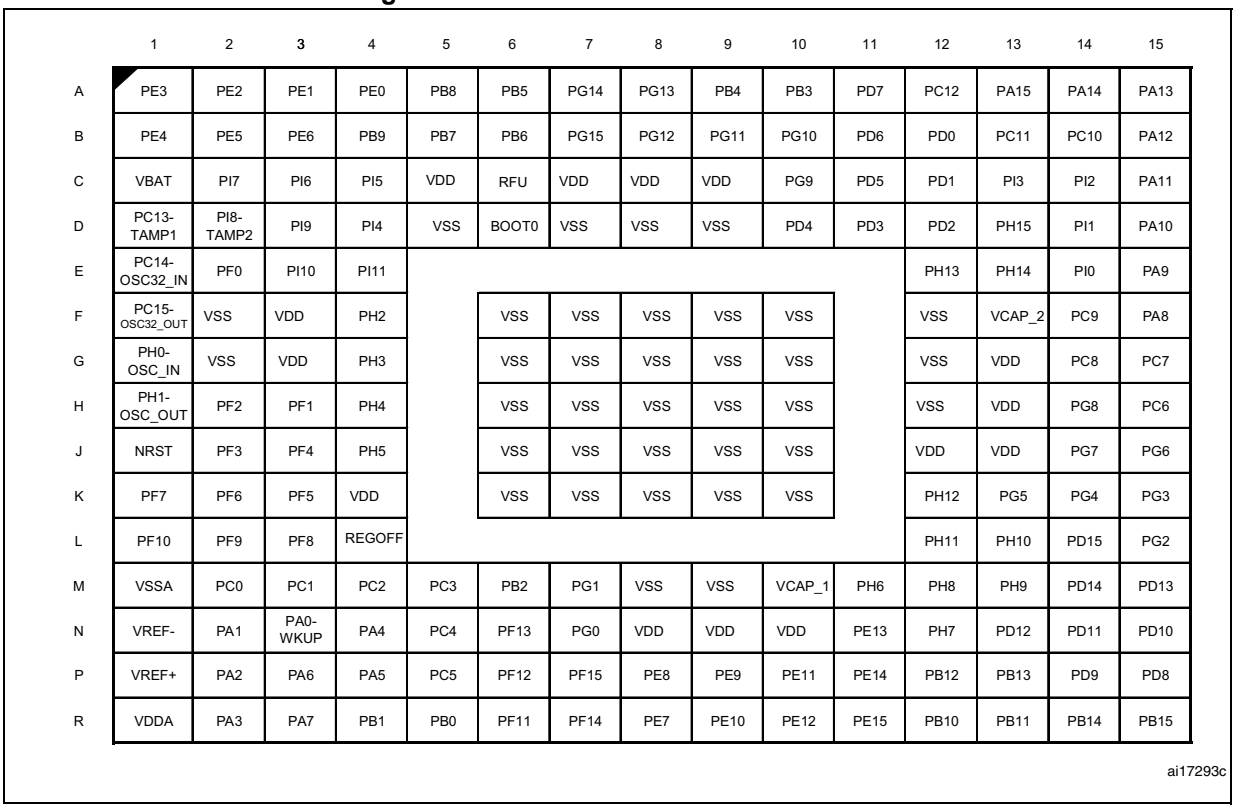
The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one

Figure 13. STM32F20x LQFP144 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Figure 15. STM32F20x UFBGA176 ballout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	RFU	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13-TAMP1	PI8-TAMP2	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP_2	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	REGOFF								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0-WKUP	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

ai17293c

1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	14	20	J3	PF4	I/O	FT	(4)	FSMC_A4, EVENTOUT	ADC3_IN14
-	-	-	15	21	K3	PF5	I/O	FT	(4)	FSMC_A5, EVENTOUT	ADC3_IN15
-	H9	10	16	22	G2	V_{SS}	S	-	-	-	-
-	-	11	17	23	G3	V_{DD}	S	-	-	-	-
-	-	-	18	24	K2	PF6	I/O	FT	(4)	TIM10_CH1, FSMC_NIORD, EVENTOUT	ADC3_IN4
-	-	-	19	25	K1	PF7	I/O	FT	(4)	TIM11_CH1,FSMC_NREG, EVENTOUT	ADC3_IN5
-	-	-	20	26	L3	PF8	I/O	FT	(4)	TIM13_CH1, FSMC_NIOWR, EVENTOUT	ADC3_IN6
-	-	-	21	27	L2	PF9	I/O	FT	(4)	TIM14_CH1, FSMC_CD, EVENTOUT	ADC3_IN7
-	-	-	22	28	L1	PF10	I/O	FT	(4)	FSMC_INTR, EVENTOUT	ADC3_IN8
5	E9	12	23	29	G1	PH0/OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN(4)
6	F9	13	24	30	H1	PH1/OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT(4)
7	E8	14	25	31	J1	NRST	I/O		-	-	-
8	G9	15	26	32	M2	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP, EVENTOUT	ADC123_ IN10
9	F8	16	27	33	M3	PC1	I/O	FT	(4)	ETH_MDC, EVENTOUT	ADC123_ IN11
10	D7	17	28	34	M4	PC2	I/O	FT	(4)	SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, EVENTOUT	ADC123_ IN12
11	G8	18	29	35	M5	PC3	I/O	FT	(4)	SPI2_MOSI, I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT	ADC123_ IN13
-	-	19	30	36	-	V_{DD}	S	-	-	-	-
12	-	20	31	37	M1	V_{SSA}	S	-	-	-	-
-	-	-	-	-	N1	V_{REF-}	S	-	-	-	-
-	F7	21	32	38	P1	V_{REF+}	S	-	-	-	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
54	C7	83	116	144	D12	PD2	I/O	FT	-	TIM3_ETR,UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	-	84	117	145	D11	PD3	I/O	FT	-	FSMC_CLK,USART2_CTS, EVENTOUT	-
-	-	85	118	146	D10	PD4	I/O	FT	-	FSMC_NOE, USART2_RTS, EVENTOUT	-
-	-	86	119	147	C11	PD5	I/O	FT	-	FSMC_NWE,USART2_TX, EVENTOUT	-
-	-	-	120	148	D8	V_{SS}	S	-	-	-	-
-	-	-	121	149	C8	V_{DD}	S	-	-	-	-
-	-	87	122	150	B11	PD6	I/O	FT	-	FSMC_NWAIT, USART2_RX, EVENTOUT	-
-	-	88	123	151	A11	PD7	I/O	FT	-	USART2_CK,FSMC_NE1, FSMC_NCE2, EVENTOUT	-
-	-	-	124	152	C10	PG9	I/O	FT	-	USART6_RX, FSMC_NE2,FSMC_NCE3, EVENTOUT	-
-	-	-	125	153	B10	PG10	I/O	FT	-	FSMC_NCE4_1, FSMC_NE3, EVENTOUT	-
-	-	-	126	154	B9	PG11	I/O	FT	-	FSMC_NCE4_2, ETH_MII_TX_EN , ETH _RMII_TX_EN, EVENTOUT	-
-	-	-	127	155	B8	PG12	I/O	FT	-	FSMC_NE4, USART6_RTS, EVENTOUT	-
-	-	-	128	156	A8	PG13	I/O	FT	-	FSMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-
-	-	-	129	157	A7	PG14	I/O	FT	-	FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT	-
-	-	-	130	158	D7	V_{SS}	S	-	-	-	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 17*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 18*.

Figure 17. Pin loading conditions

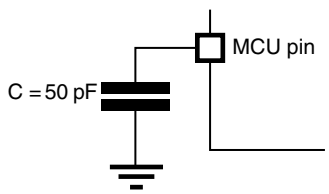


Figure 18. Pin input voltage

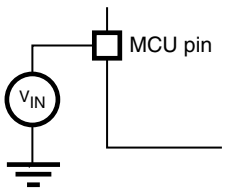
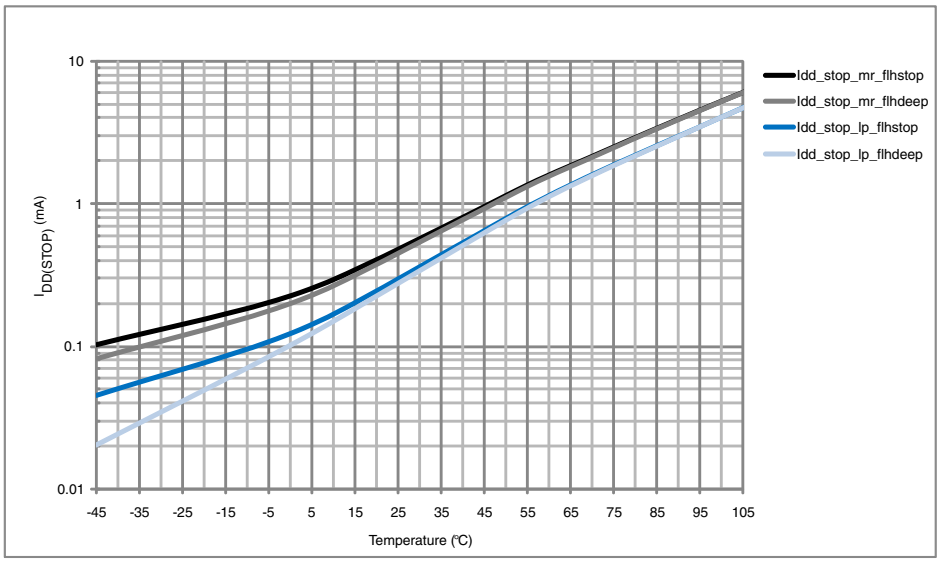


Table 23. Typical and maximum current consumptions in Stop mode

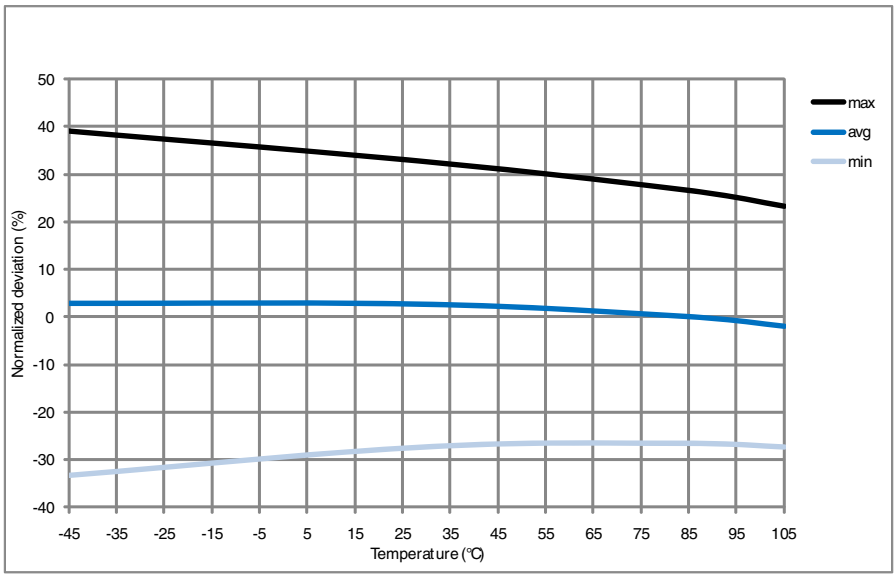
Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Figure 29. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Figure 35. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 34. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10(2)	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	120	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	-	48	MHz
f_{VCO_OUT}	PLL VCO output	-	192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 37. Flash memory characteristics

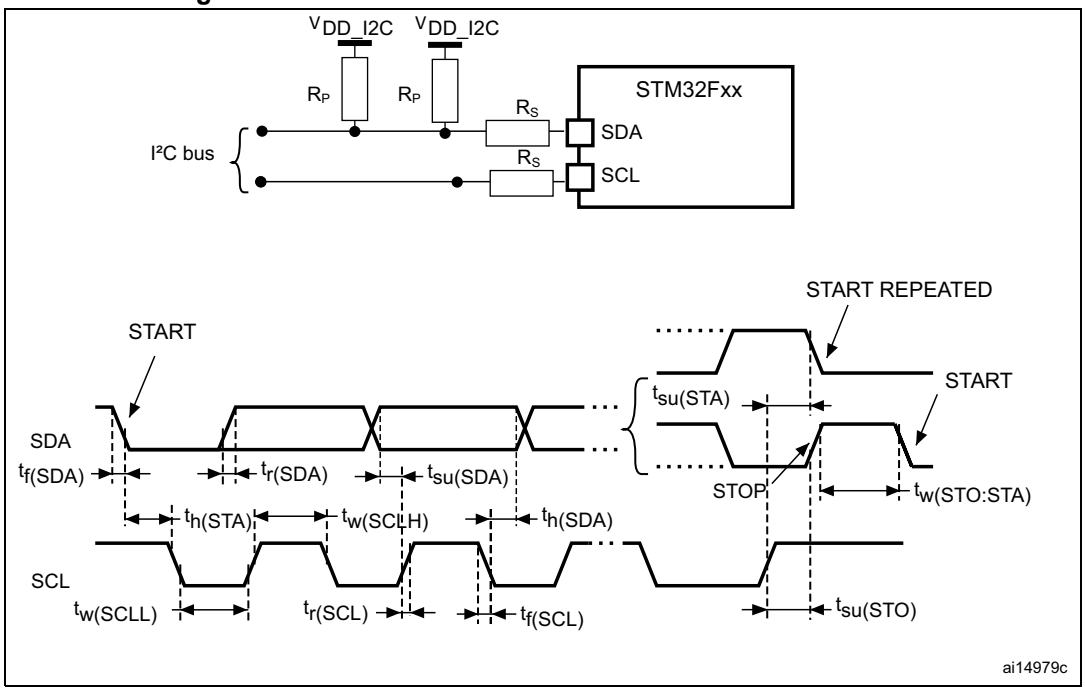
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 38. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Figure 41. I²C bus AC waveforms and measurement circuit



1. R_S= series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I²C bus power supply.

Table 53. SCL frequency (f_{PCLK1}= 30 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

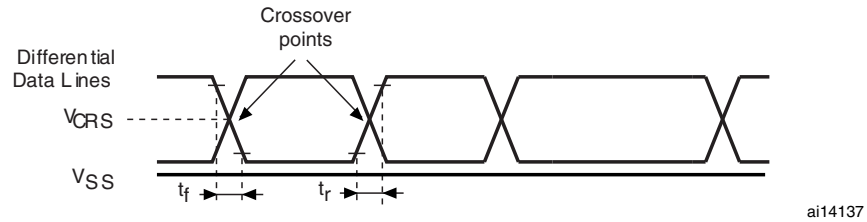


Table 58. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Table 59 shows the USB HS operating voltage.

Table 59. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 60. Clock timing parameters

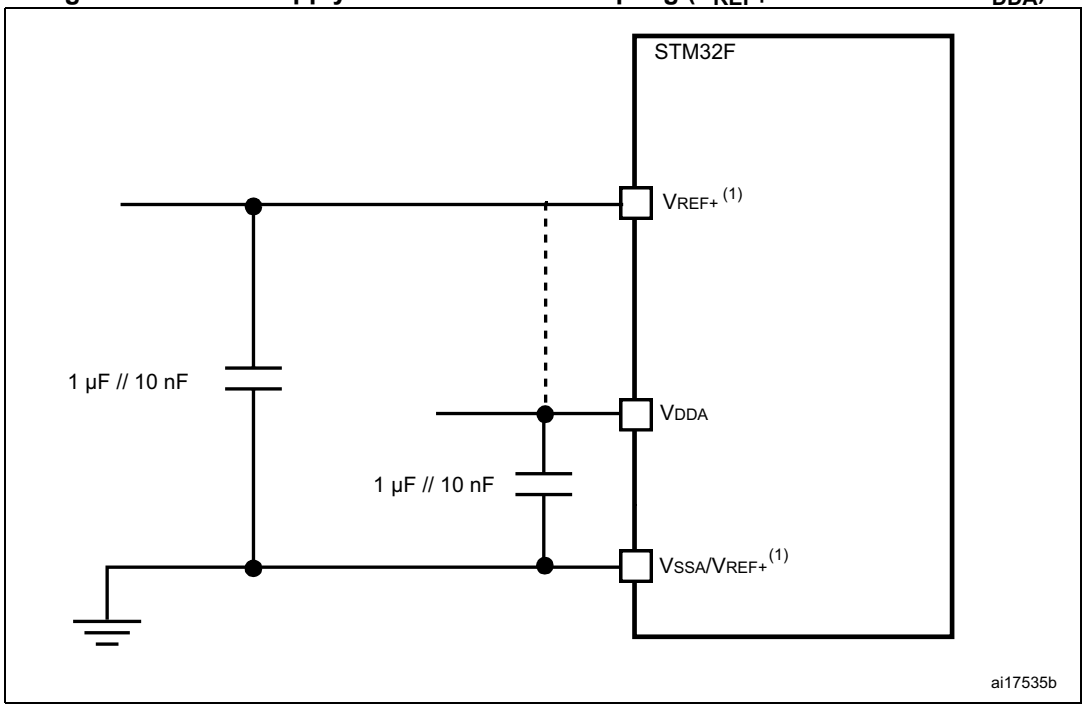
Parameter(1)		Symbol	Min	Nominal	Max	Unit
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design, not tested in production.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 54* or *Figure 55*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 54. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 64. Synchronous non-multiplexed PSRAM write timings

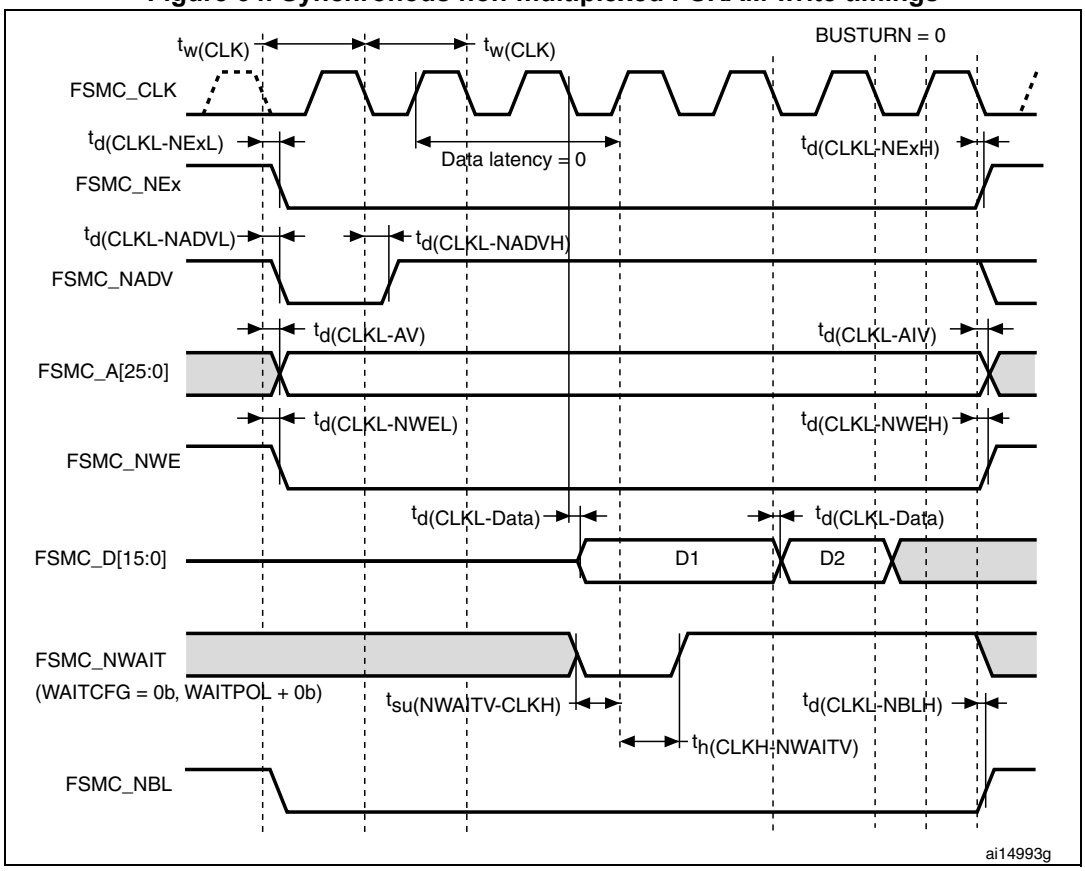


Table 79. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns

Figure 76. SD default mode

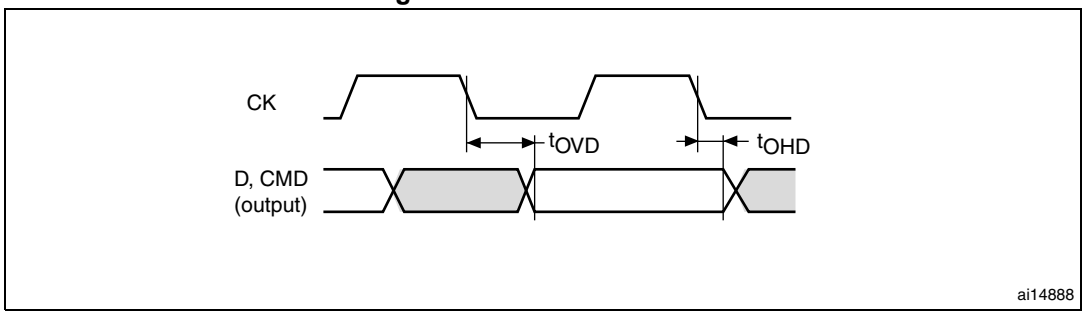


Table 85. SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	8/3	-
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	32	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	31	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	3.5	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0.3	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

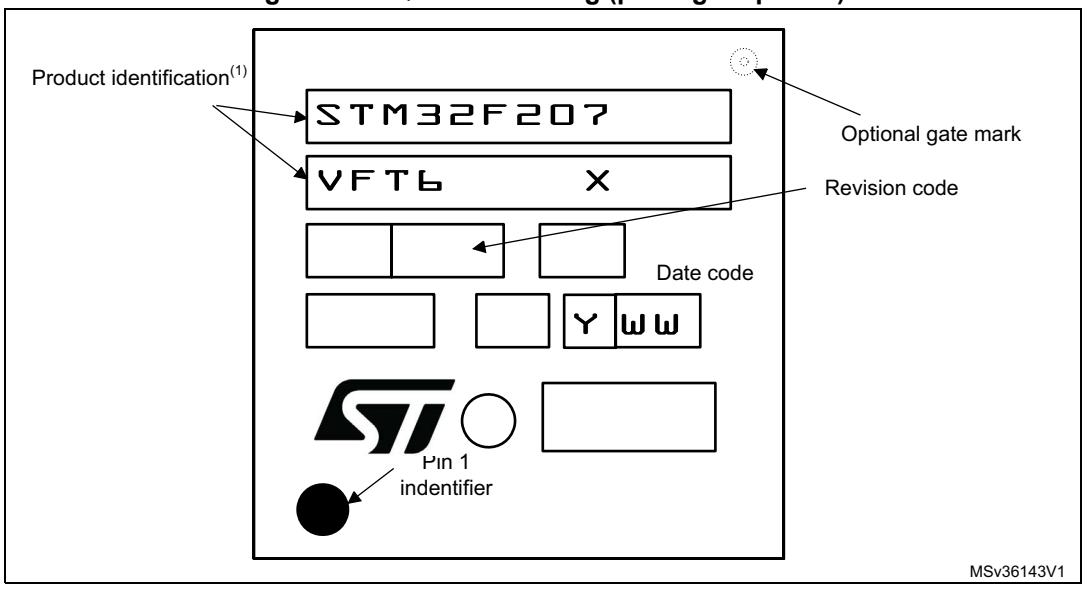
6.3.28 RTC characteristics

Table 86. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Device marking

Figure 83. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 95. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch	51	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 97. Document revision history (continued)

Date	Revision	Changes
13-Jul-2010	4 (continued)	Added USB OTG_FS features in *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)*. Updated V_{CAP_1} and V_{CAP_2} capacitor value to 2.2 µF in *Figure 19: Power supply scheme*. Removed DAC, modified ADC limitations, and updated I/O compensation for 1.8 to 2.1 V range in *Table 15: Limitations depending on the operating power supply range*. Added V_{BORL}, V_{BORM}, V_{BORH} and I_{RUSH} in *Table 19: Embedded reset and power control block characteristics*. Removed table Typical current consumption in Sleep mode with Flash memory in Deep power down mode. Merged typical and maximum current consumption sections and added *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*, *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM, Table 22: Typical and maximum current consumption in Sleep mode, Table 23: Typical and maximum current consumptions in Stop mode, Table 24: Typical and maximum current consumptions in Standby mode*, and *Table 25: Typical and maximum current consumptions in VBAT mode*. Update *Table 34: Main PLL characteristics* and added *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Added *Note 8* for CIO in *Table 48: I/O AC characteristics*. Updated *Section 6.3.18: TIM timer characteristics*. Added T_{NRST_OUT} in *Table 49: NRST pin characteristics*. Updated *Table 52: I2C characteristics*. Removed 8-bit data in and data out waveforms from *Figure 48: ULPI timing diagram*. Removed note related to ADC calibration in *Table 67*. *Section 6.3.20: 12-bit ADC characteristics*: ADC characteristics tables merged into one single table; tables ADC conversion time and ADC accuracy removed. Updated *Table 68: DAC characteristics*. Updated *Section 6.3.22: Temperature sensor characteristics* and *Section 6.3.23: VBAT monitoring characteristics*. Update *Section 6.3.26: Camera interface (DCMI) timing specifications*. Added *Section 6.3.27: SD/SDIO MMC card host interface (SDIO) characteristics*, and *Section 6.3.28: RTC characteristics*. Added *Section 7.7: Thermal characteristics*. Updated *Table 91: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data* and *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Changed tape and reel code to TX in *Table 96: Ordering information scheme*. Added *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Updated figures in Appendix *A.2: USB OTG full speed (FS) interface solutions* and *A.3: USB OTG high speed (HS) interface solutions*. Updated *Figure 94: Audio player solution using PLL, PLLI2S, USB and 1 crystal* and *Figure 95: Audio PLL (PLLI2S) providing accurate I2S clock*.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6	Changed datasheet status to “Full Datasheet”. Introduced concept of SRAM1 and SRAM2. LQFP176 package now in production and offered only for 256 Kbyte and 1 Mbyte devices. Availability of WLCSP64+2 package limited to 512 Kbyte and 1 Mbyte devices. Updated *Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package* and *Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package*. Added camera interface for STM32F207Vx devices in *Table 2: STM32F205xx features and peripheral counts*. Removed 16 MHz internal RC oscillator accuracy in *Section 3.12: Clocks and startup*. Updated *Section 3.16: Voltage regulator*. Modified I^2S sampling frequency range in *Section 3.12: Clocks and startup*, *Section 3.24: Inter-integrated sound (I2S)*, and *Section 3.30: Audio PLL (PLLI2S)*. Updated *Section 3.17: Real-time clock (RTC), backup SRAM and backup registers* and description of TIM2 and TIM5 in *Section 3.20.2: General-purpose timers (TIMx)*. Modified maximum baud rate (oversampling by 16) for USART1 in *Table 6: USART feature comparison*. Updated note related to RFU pin below *Figure 12: STM32F20x LQFP100 pinout*, *Figure 13: STM32F20x LQFP144 pinout*, *Figure 14: STM32F20x LQFP176 pinout*, *Figure 15: STM32F20x UFBGA176 ballout*, and *Table 8: STM32F20x pin and ball definitions*. In *Table 8: STM32F20x pin and ball definitions*,:changed I2S2_CK and I2S3_CK to I2S2_SCK and I2S3_SCK, respectively; added PA15 and TT (3.6 V tolerant I/O). Added RTC_50Hz as PB15 alternate function in *Table 8: STM32F20x pin and ball definitions* and *Table 10: Alternate function mapping*. Removed ETH _RMII_TX_CLK for PC3/AF11 in *Table 10: Alternate function mapping*. Updated *Table 11: Voltage characteristics* and *Table 12: Current characteristics*. T_{STG} updated to –65 to +150 in *Table 13: Thermal characteristics*. Added CEXT, ESL, and ESR in *Table 14: General operating conditions* as well as *Section 6.3.2: VCAP1/VCAP2 external capacitor*. Modified *Note 4* in *Table 15: Limitations depending on the operating power supply range*. Updated *Table 17: Operating conditions at power-up / power-down (regulator ON)*, and *Table 18: Operating conditions at power-up / power-down (regulator OFF)*. Added OSC_OUT pin in *Figure 17: Pin loading conditions*. and *Figure 18: Pin input voltage*. Updated *Figure 19: Power supply scheme* to add IRROFF and REGOFF pins and modified notes. Updated V_{PVD}, V_{BOR1}, V_{BOR2}, V_{BOR3}, $T_{RSTTEMPO}$ typical value, and I_{RUSH}, added E_{RUSH} and *Note 2* in *Table 19: Embedded reset and power control block characteristics*.