Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vet7

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

The DMA can be used with the main peripherals:
- SPI and I^2S
- I^2C
- USART and UART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC.

3.9 Flexible static memory controller (FSMC)

The FSMC is embedded in all STM32F20x devices. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- Maximum frequency (f_{HCLK}) for external access is 60 MHz

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.10 Nested vectored interrupt controller (NVIC)

The STM32F20x devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M3.

The NVIC main features are the following:
- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

The devices embed a dedicate PLL (PLLI2S) which allow to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

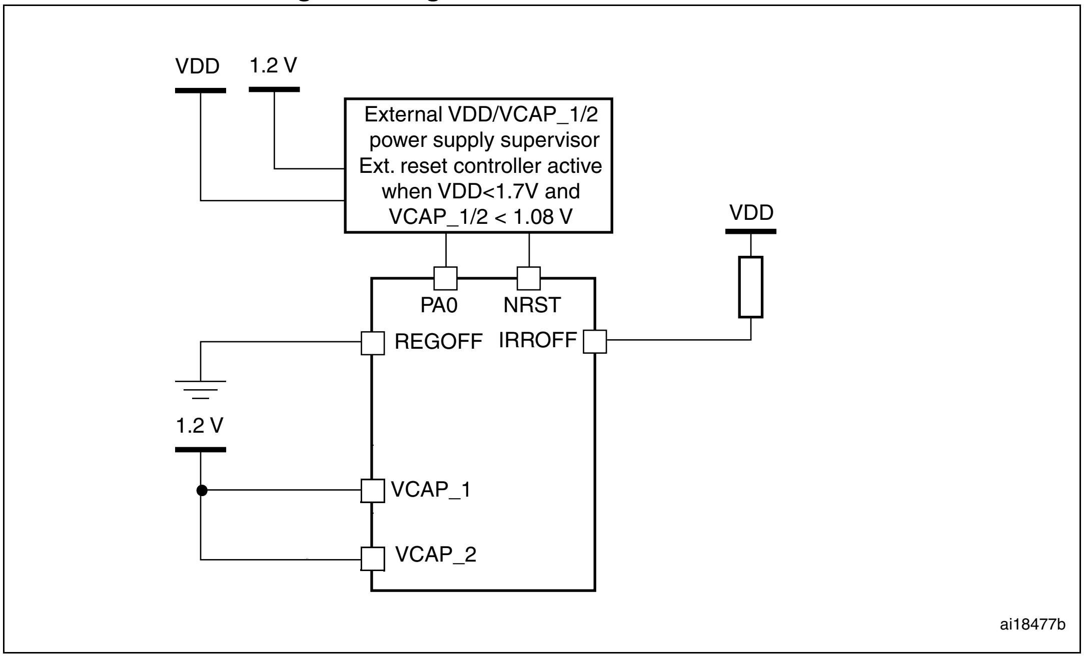
- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

3.14 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates

Figure 7. Regulator OFF/internal reset OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains (see *Figure 8*).
- PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V, and until V_{DD} reaches 1.7 V.
- NRST should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.7 V (see *Figure 9*).

In this mode, when the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry is disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see *Table 5* for differences).

TIM2, TIM3, TIM4, TIM5

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

3.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

3.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F20x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024× 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
38	F2	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	-
39	F3	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	D1	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	E2	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	E3	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_VBUS
43	D3	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	D2	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4,OTG_FS_DM, EVENTOUT	-
45	C1	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	B2	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	C2	73	106	125	F13	V_{CAP_2}	S	-	-	-	-
-	B1	74	107	126	F12	V_{SS}	S	-	-	-	-
48	A8	75	108	127	G13	V_{DD}	S	-	-	-	-
-	-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

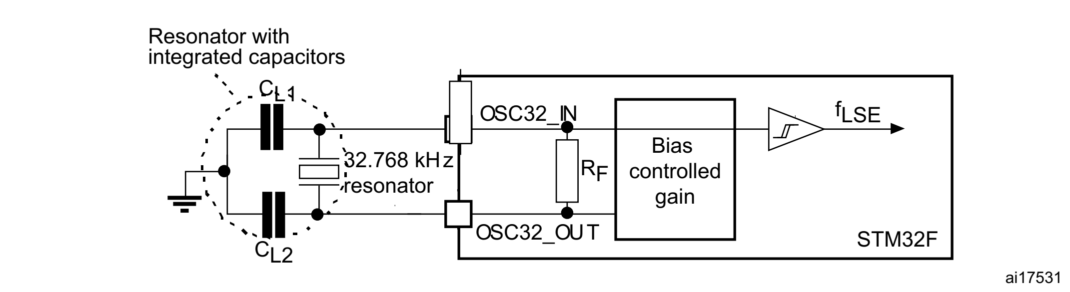
Table 31. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	-	-	-	1	µA
g_m	Oscillator Transconductance	-	2.8	-	-	µA/V
$t_{SU(LSE)}$(2)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For information on electing the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 33. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in Table 32 and Table 33 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 14.

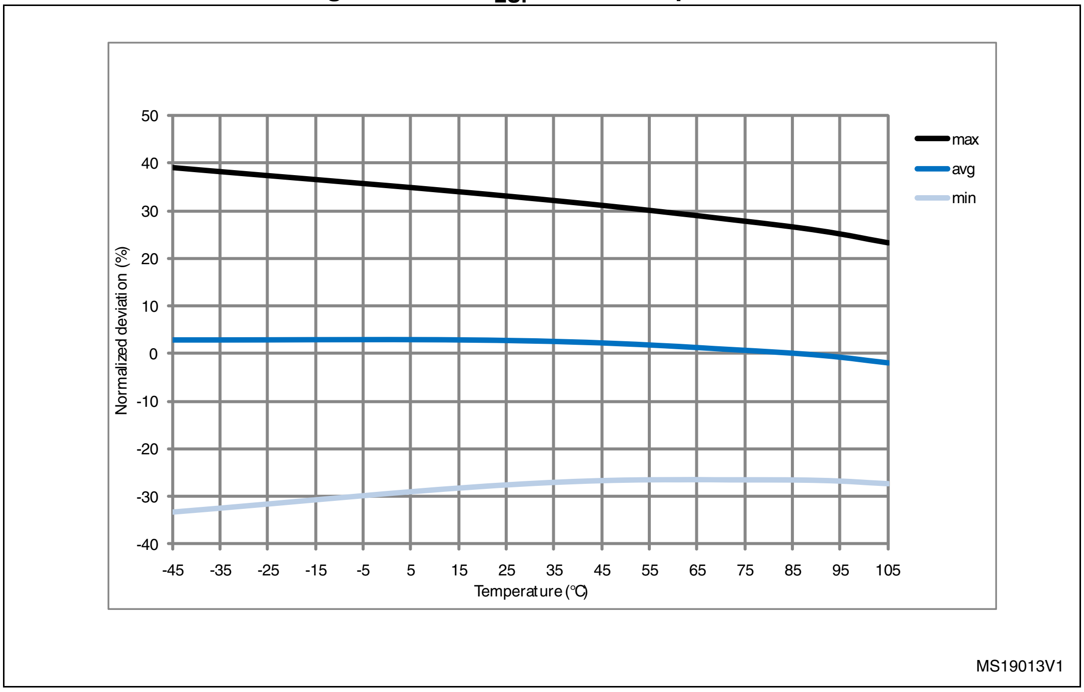
High-speed internal (HSI) RC oscillator

Table 32. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user-trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	– 8	-	4.5	%
		T_A = –10 to 85 °C(3)	– 4	-	4	%
		T_A = 25 °C(4)	– 1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4.0	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 35. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 34. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10(2)	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	120	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	-	48	MHz
f_{VCO_OUT}	PLL VCO output	-	192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 37. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 38. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC® code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 42. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. $[f_{HSE}/f_{CPU}]$ 25/120 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, peripheral clock disabled	0.1 to 30 MHz	25	dBµV
			30 to 130 MHz		
			130 MHz to 1GHz		
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, PLL spread spectrum enabled, peripheral clock disabled	0.1 to 30 MHz	28	dBµV
			30 to 130 MHz	26	
			130 MHz to 1GHz	22	
			SAE EMI level	4	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

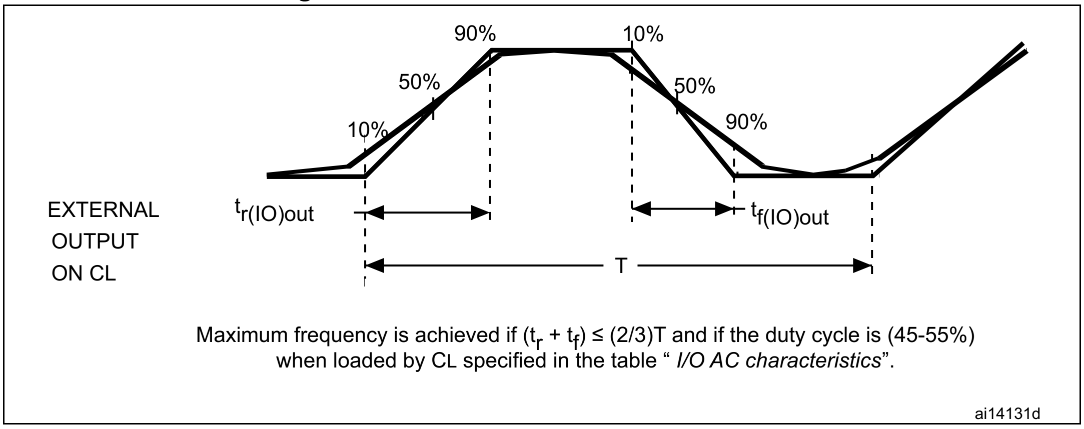
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Guaranteed by characterization results, not tested in production.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Figure 39. I/O AC characteristics definition



6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 49*).

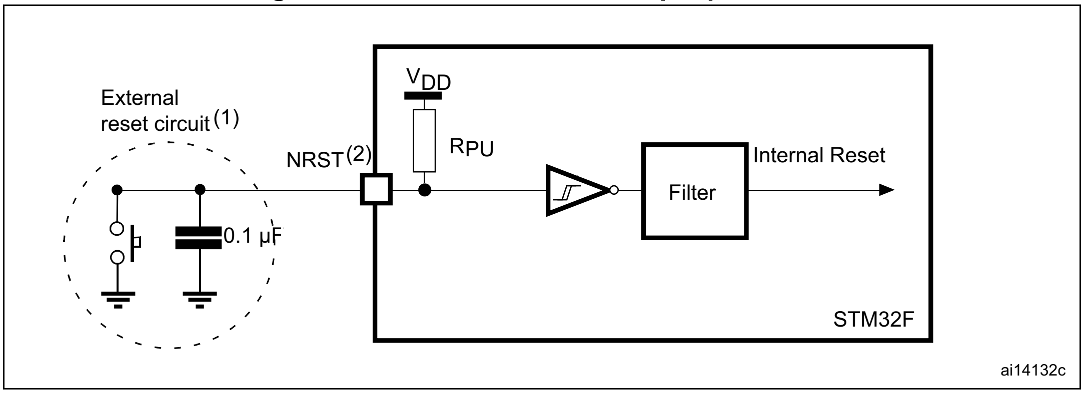
Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design, not tested in production.

Figure 40. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 49*. Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in *Table 50* and *Table 51* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 50. Characteristics of TIMx connected to the APB1 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK}$ = 60 MHz	1	-	$t_{TIMxCLK}$
			16.7	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK}$ = 30 MHz	1	-	$t_{TIMxCLK}$
			33.3	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 60 MHz APB1= 30 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	30	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0167	1092	µs
	32-bit counter clock period when internal clock is selected		1	-	$t_{TIMxCLK}$
			0.0167	71582788	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	71.6	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

Figure 42. SPI timing diagram - slave mode and CPHA = 0

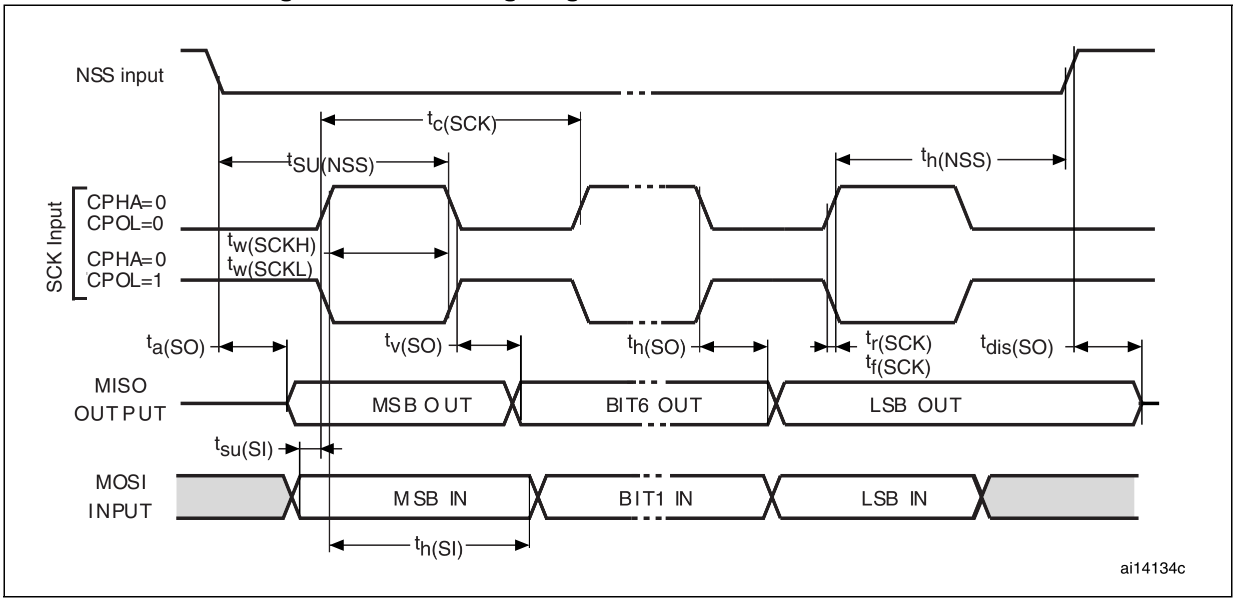


Figure 43. SPI timing diagram - slave mode and CPHA = 1

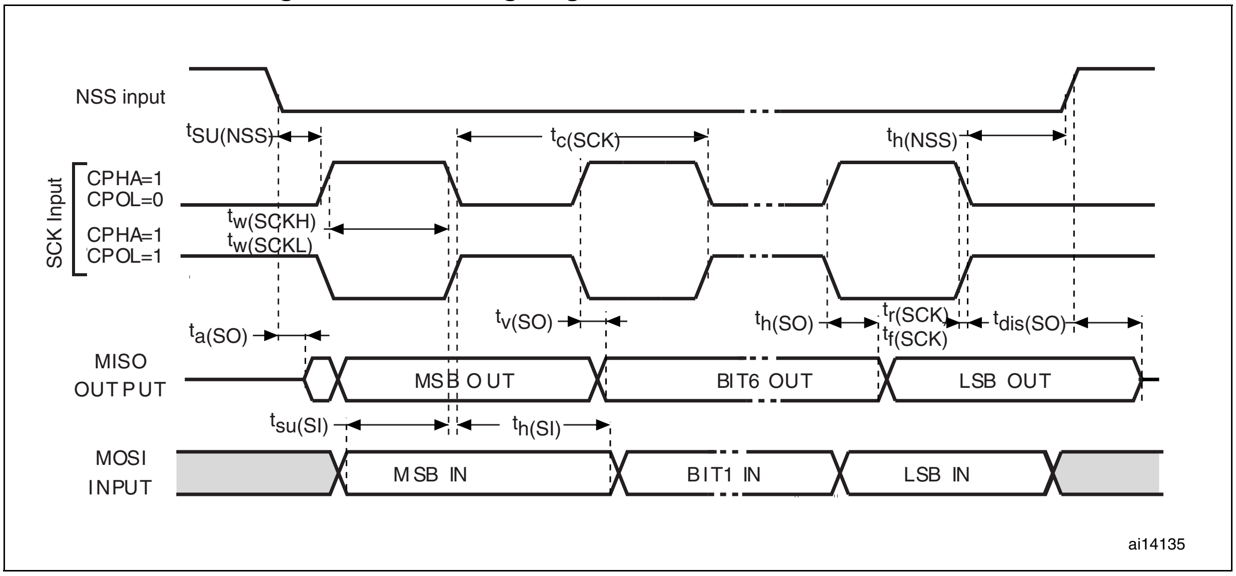


Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 64. Synchronous non-multiplexed PSRAM write timings

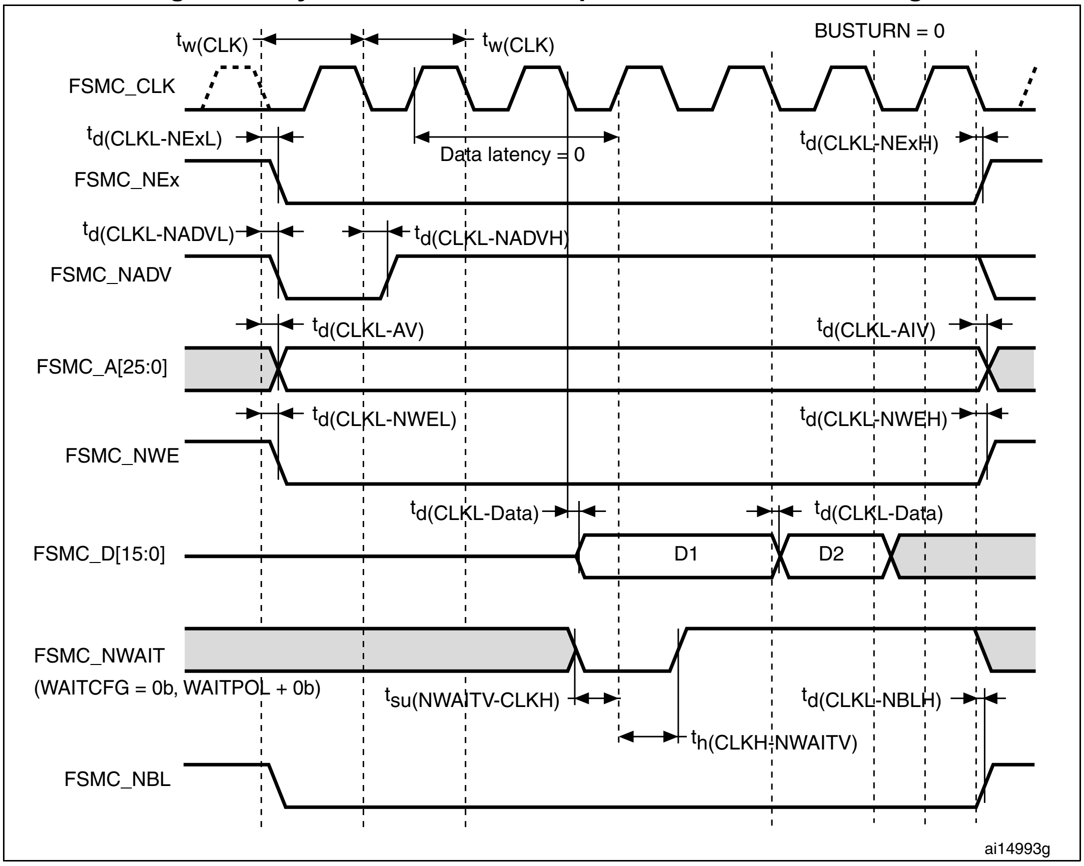


Table 79. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns

Table 83. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}$- 1	$4T_{HCLK}$+ 3	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$+ 2	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}$- 2	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

6.3.26 Camera interface (DCMI) timing specifications

Table 84. DCMI characteristics

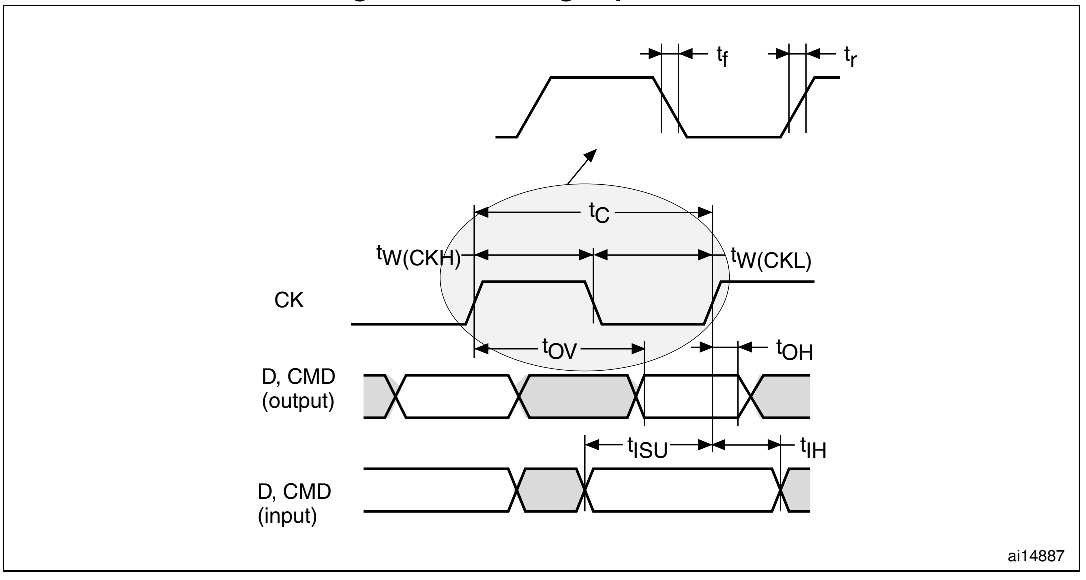
Symbol	Parameter	Conditions	Min	Max
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	DCMI_PIXCLK= 48 MHz	-	0.4

6.3.27 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 85* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

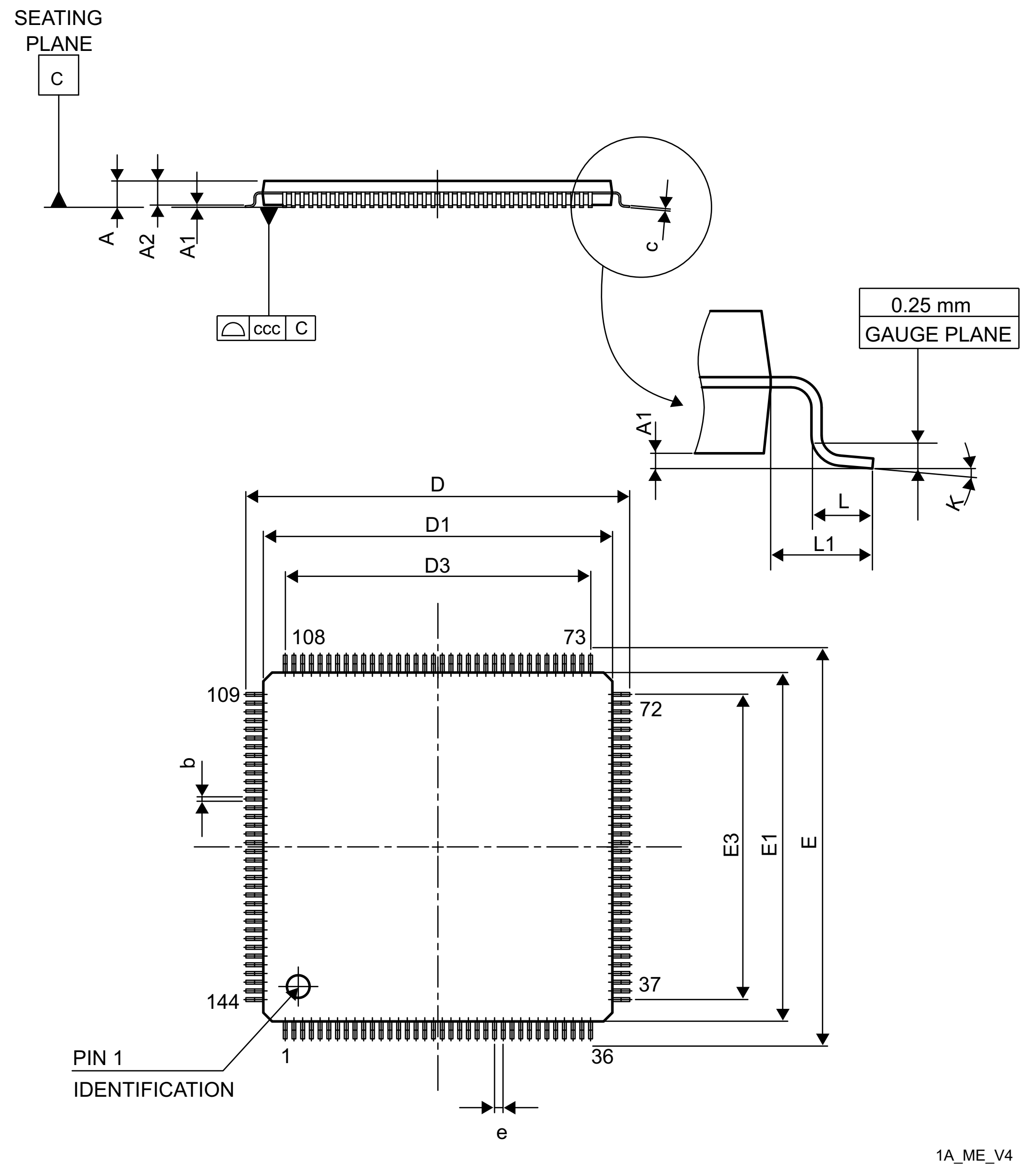
Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 75. SDIO high-speed mode



7.4 LQFP144 package information

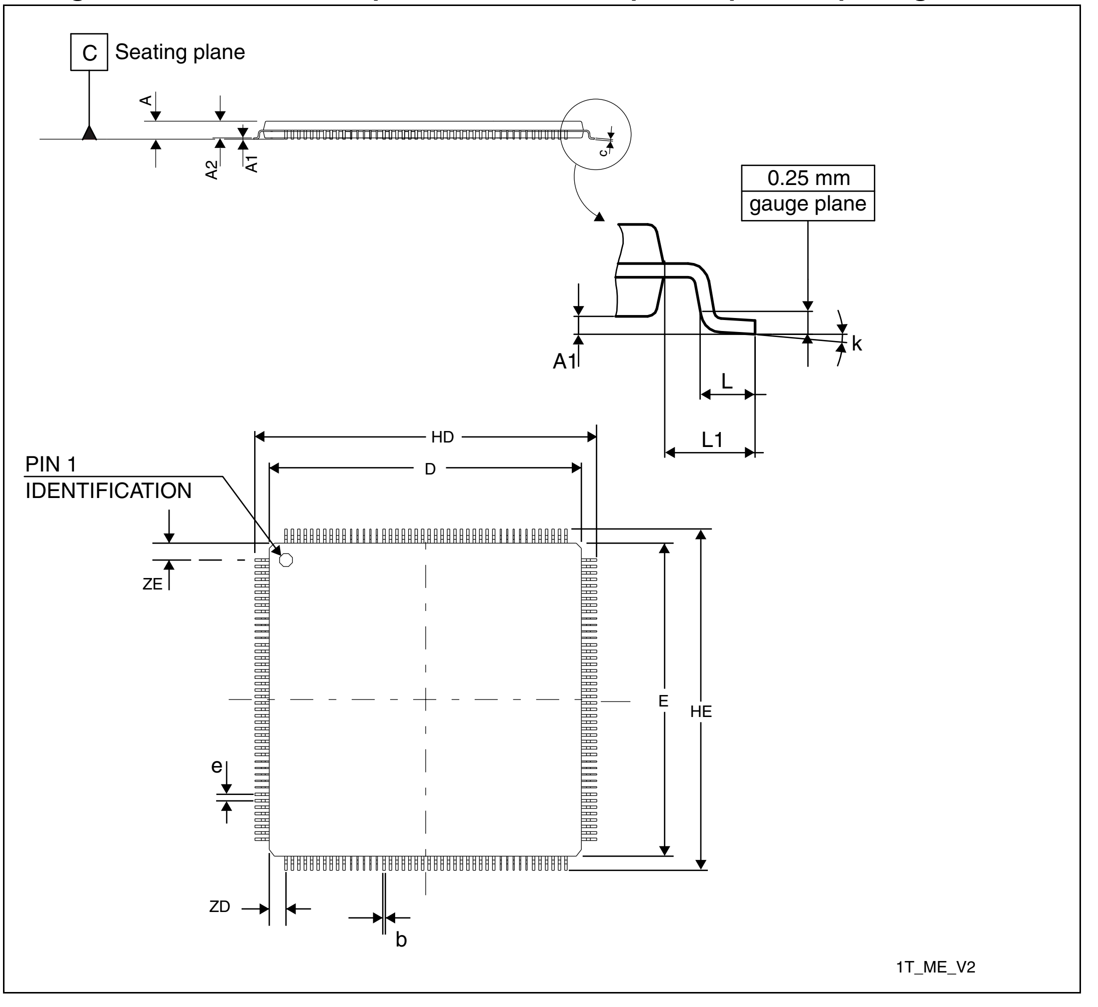
Figure 84. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.5 LQFP176 package information

Figure 87. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline

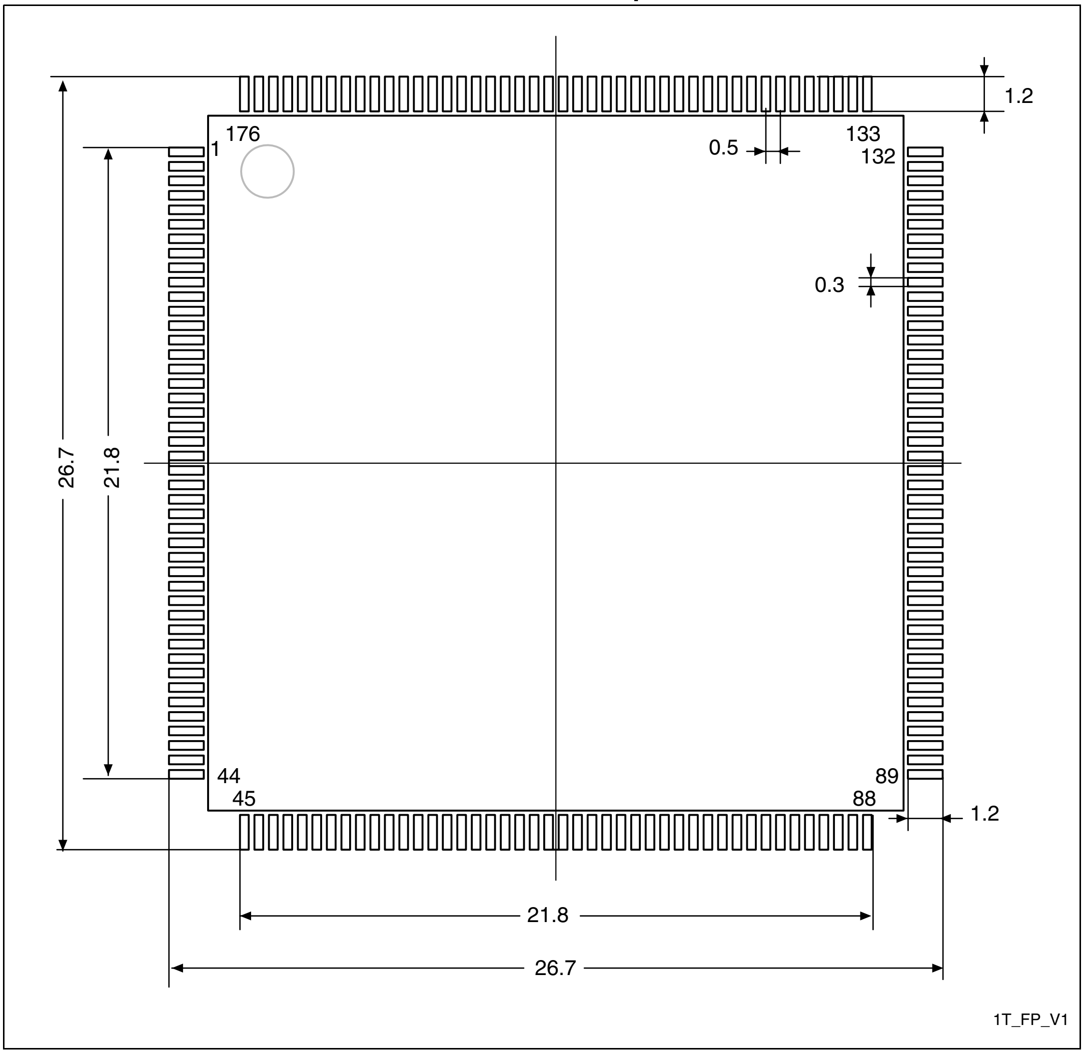


1. Drawing is not to scale.

Table 92. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

Symbol	Dimensions					
	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Figure 88. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 97. Document revision history (continued)

Date	Revision	Changes
25-Nov-2010	5	Update I/Os in *Section : Features*. Added WLCSP64+2 package. Added note 1 related to LQFP176 on cover page. Added trademark for ART accelerator. Updated *Section 3.2: Adaptive real-time memory accelerator (ART Accelerator™)*. Updated *Figure 5: Multi-AHB matrix*. Added case of BOR inactivation using IRROFF on WLCSP devices in *Section 3.15: Power supply supervisor*. Reworked *Section 3.16: Voltage regulator* to clarify regulator off modes. Renamed PDROFF, IRROFF in the whole document. Added *Section 3.19: VBAT operation*. Updated LIN and IrDA features for UART4/5 in *Table 6: USART feature comparison*. *Table 8: STM32F20x pin and ball definitions*: Modified V_{DD_3} pin, and added note related to the FSMC_NL pin; renamed BYPASS-REG REGOFF, and add IRROFF pin; renamed USART4/5 UART4/5. USART4 pins renamed UART4. Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use. Updated maximum HSE crystal frequency to 26 MHz. *Section 6.2: Absolute maximum ratings*: Updated V_{IN} minimum and maximum values and note related to five-volt tolerant inputs in *Table 11: Voltage characteristics*. Updated $I_{INJ(PIN)}$ maximum values and related notes in *Table 12: Current characteristics*. Updated V_{DDA} minimum value in *Table 14: General operating conditions*. Added Note 2 and updated Maximum CPU frequency in *Table 15: Limitations depending on the operating power supply range*, and added *Figure 21: Number of wait states versus fCPU and VDD range*. Added brownout level 1, 2, and 3 thresholds in *Table 19: Embedded reset and power control block characteristics*. Changed f_{OSC_IN} maximum value in *Table 30: HSE 4-26 MHz oscillator characteristics*. Changed f_{PLL_IN} maximum value in *Table 34: Main PLL characteristics*, and updated jitter parameters in *Table 35: PLLI2S (audio PLL) characteristics*. *Section 6.3.16: I/O port characteristics*: updated V_{IH} and V_{IL} in *Table 48: I/O AC characteristics*. Added *Note 1* below *Table 47: Output voltage characteristics*. Updated R_{PD} and R_{PU} parameter description in *Table 57: USB OTG FS DC electrical characteristics*. Updated V_{REF+} minimum value in *Table 66: ADC characteristics*. Updated *Table 71: Embedded internal reference voltage*. Removed Ethernet and USB2 for 64-pin devices in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Added *A.2: USB OTG full speed (FS) interface solutions*, removed “OTG FS connection with external PHY” figure, updated *Figure 87*, *Figure 88*, and *Figure 90* to add STULPI01B.