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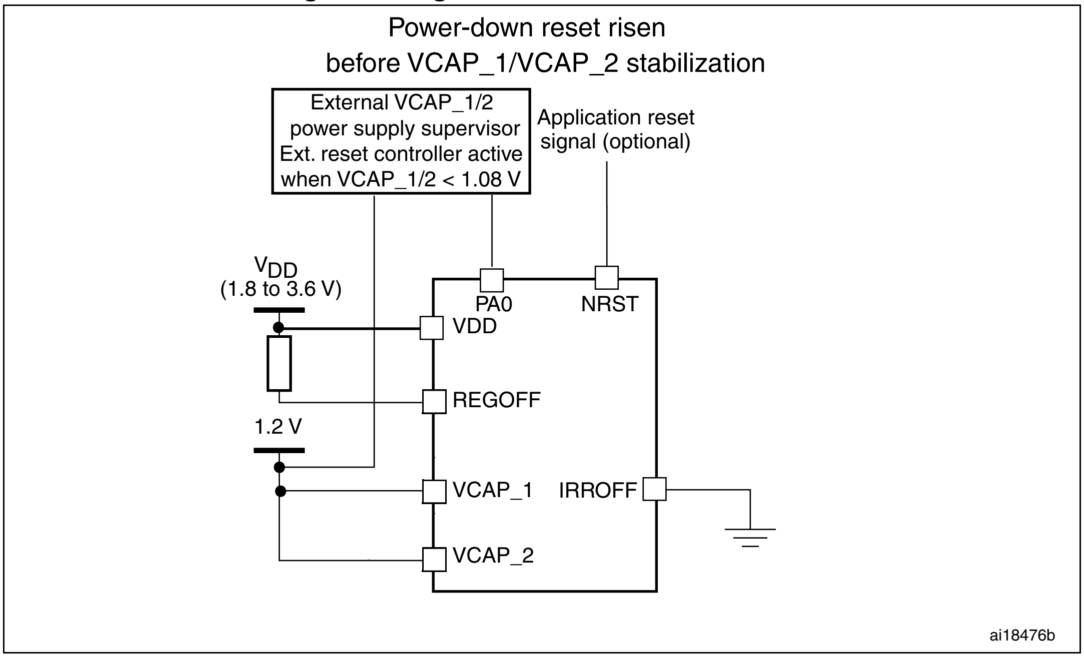
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vft6

Figure 6. Regulator OFF/internal reset ON



The following conditions must be respected:

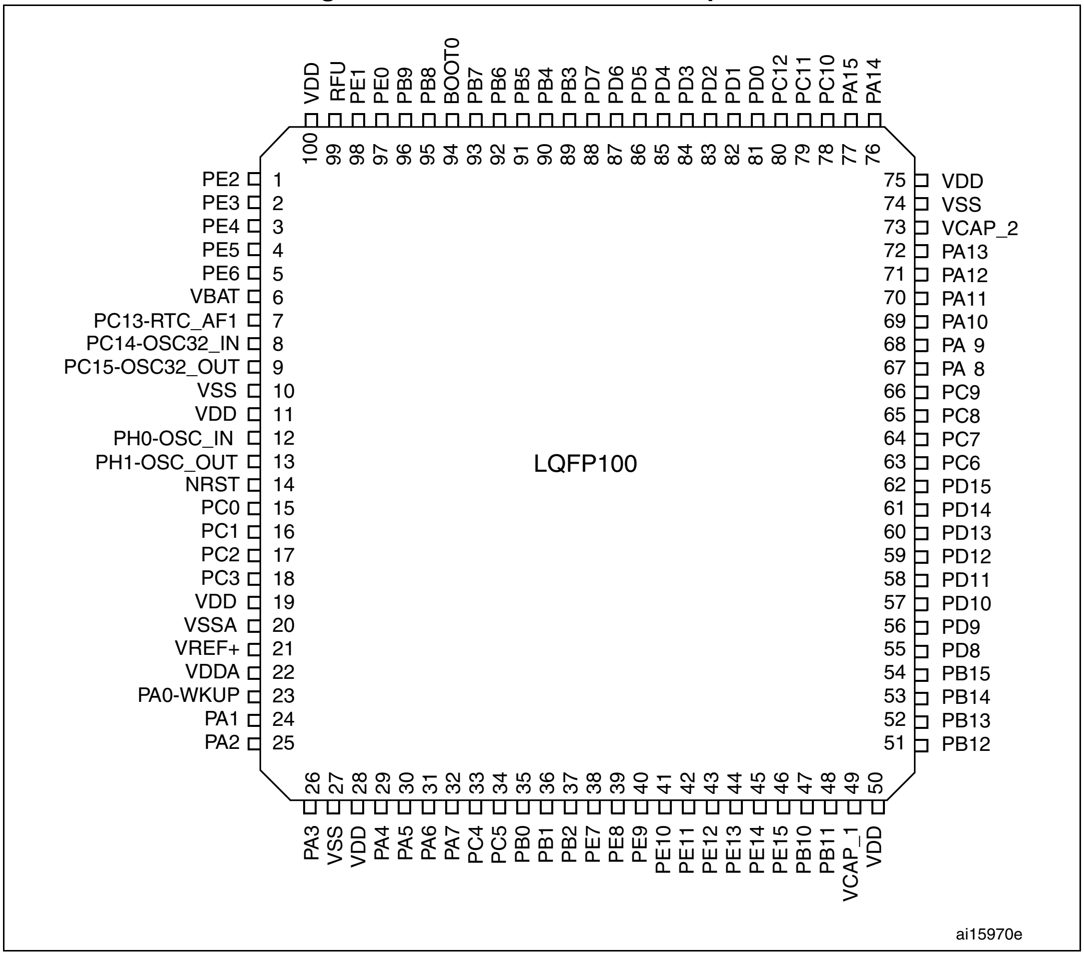
- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 8*).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD}. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

Figure 12. STM32F20x LQFP100 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 9. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD13	-	A18	A18	-	Yes
PD14	D0	D0	DA0	D0	Yes
PD15	D1	D1	DA1	D1	Yes
PG2	-	A12	-	-	-
PG3	-	A13	-	-	-
PG4	-	A14	-	-	-
PG5	-	A15	-	-	-
PG6	-	-	-	INT2	-
PG7	-	-	-	INT3	-
PD0	D2	D2	DA2	D2	Yes
PD1	D3	D3	DA3	D3	Yes
PD3	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	NE1	NE1	NCE2	Yes
PG9	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	-	-	-	-
PG12	-	NE4	NE4	-	-
PG13	-	A24	A24	-	-
PG14	-	A25	A25	-	-
PB7	-	NADV	NADV	-	Yes
PE0	-	NBL0	NBL0	-	Yes
PE1	-	NBL1	NBL1	-	Yes

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FSMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FSMC_D3	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	-	-	FSMC_CLK	-	-	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FSMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	FSMC_NWAIT	-	-	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FSMC_NE1/ FSMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FSMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FSMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FSMC_D15	-	-	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	FSMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	FSMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FSMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FSMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FSMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	-	FSMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	-	-	-	-	-	-	ETH _MII_TXD3	FSMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	-	FSMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	-	-	-	-	-	-	-	FSMC_A20	DCMI_D4	-	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	-	-	-	-	-	-	-	FSMC_A21	DCMI_D6	-	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	-	-	-	-	-	-	-	FSMC_A22	DCMI_D7	-	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FSMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	FSMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	FSMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	FSMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	FSMC_D8	-	-	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-	-	FSMC_D9	-	-	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	FSMC_D10	-	-	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	-	-	-	-	-	-	-	FSMC_D11	-	-	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FSMC_D12	-	-	EVENTOUT

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	120	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	120	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	–5/+0	
	Injected current on any other pin(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
4. A positive injection is induced by V_{IN}>V_{DD} while a negative injection is induced by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	30	
f_{PCLK2}	Internal APB2 clock frequency	-	0	60	

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8(1)	3.6	V
V_{DDA}(2)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(3)	1.8(1)	3.6	V
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	V
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	Input voltage on RST and FT pins	$2\ V \leq V_{DD} \leq 3.6\ V$	–0.3	5.5	V
		$1.7\ V \leq V_{DD} \leq 2\ V$	–0.3	5.2	V
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	V
	Input voltage on BOOT0 pin	-	0	9	V
V_{CAP1} / V_{CAP2}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP64	-	444	mW
		WLCSP64+2	-	392	mW
		LQFP100	-	434	mW
		LQFP144	-	500	mW
		LQFP176	-	526	mW
		UFBGA176	-	513	mW
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(5)	–40	125	°C
TJ	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	°C

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Figure 27. Typical current consumption vs. temperature in Sleep mode, peripherals ON

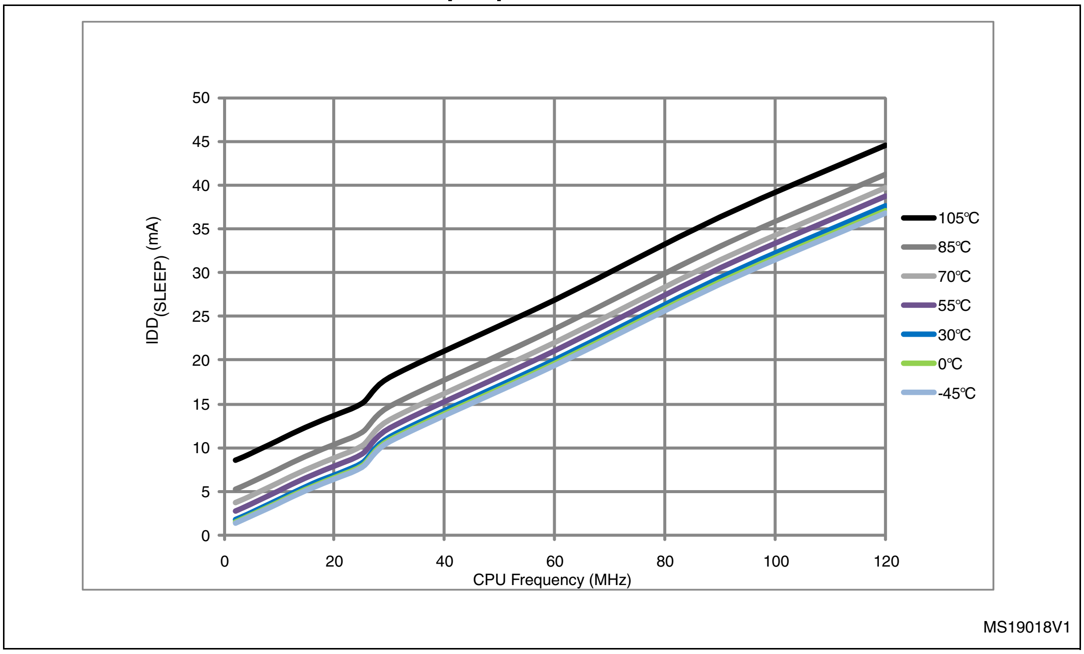


Figure 28. Typical current consumption vs. temperature in Sleep mode, peripherals OFF

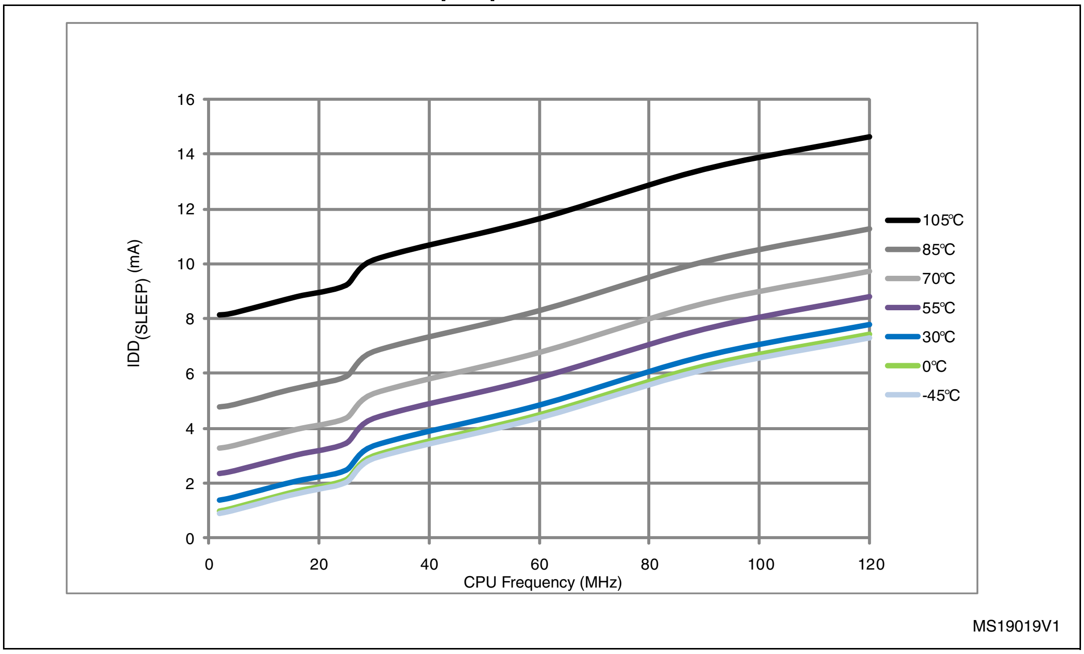


Table 26. Peripheral current consumption (continued)

Peripheral(1)		Typical consumption at 25 °C	Unit
APB2	SDIO	0.69	mA
	TIM1	1.06	
	TIM8	1.03	
	TIM9	0.58	
	TIM10	0.37	
	TIM11	0.39	
	ADC1(4)	2.13	
	ADC2(4)	2.04	
	ADC3(4)	2.12	
	SPI1	1.20	
	USART1	0.38	
	USART6	0.37	

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC_CR register.
3. EN2 bit is set in DAC_CR register.
4. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

6.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	1	-	µs
t_{WUSTOP}(2)	Wakeup from Stop mode (regulator in Run mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 42: EMI characteristics*). It is available only on the main PLL.

Table 36. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max[1]	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%(peak)$$

Figure 36 and *Figure 37* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 36. PLL output clock waveforms in center spread mode

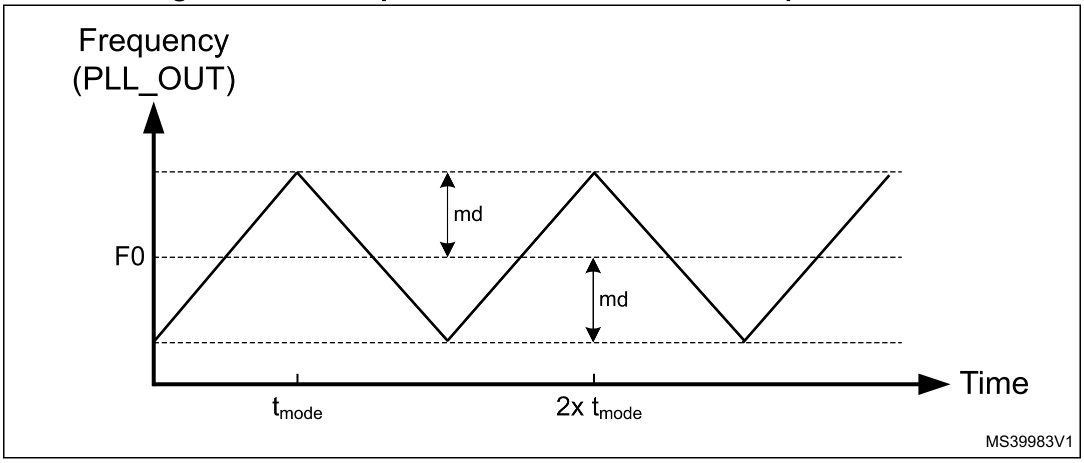
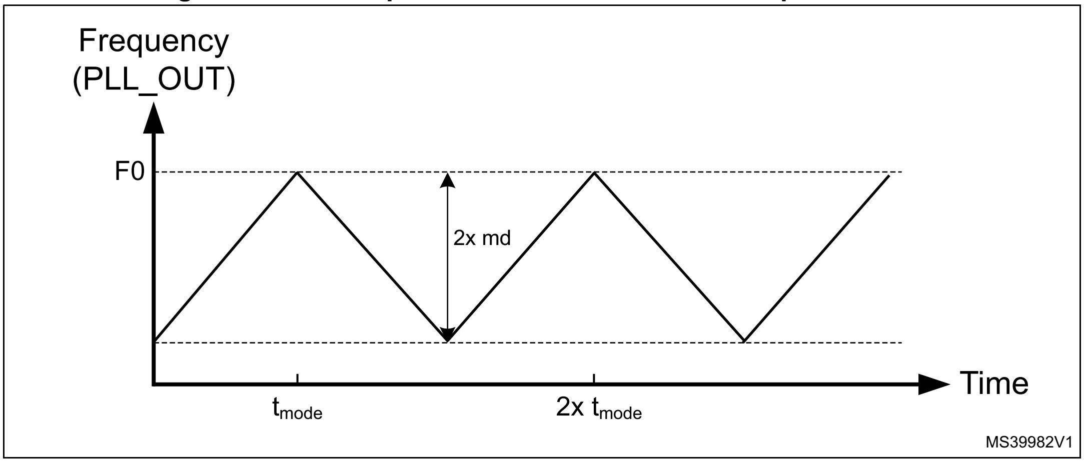


Figure 37. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 47. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS ports I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL ports I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 48. I/O AC characteristics(1)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns

Table 65 gives the list of Ethernet MAC signals for MII and *Figure 50* shows the corresponding timing diagram.

Figure 51. Ethernet MII timing diagram

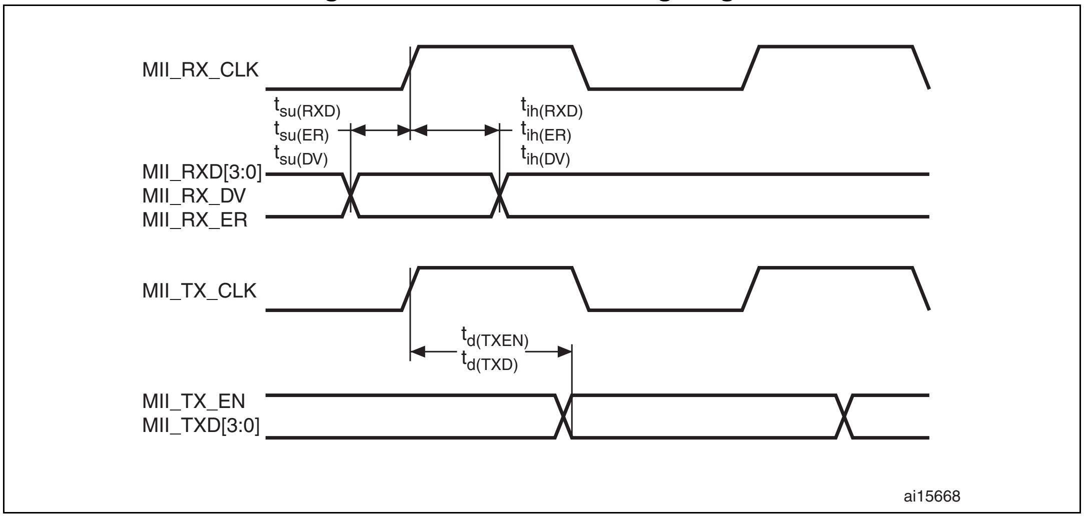


Table 65. Dynamics characteristics: Ethernet MAC signals for MII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	7.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	ns
$t_{su(DV)}$	Data valid setup time	4	-	-	ns
$t_{ih(DV)}$	Data valid hold time	0	-	-	ns
$t_{su(ER)}$	Error setup time	3.5	-	-	ns
$t_{ih(ER)}$	Error hold time	0	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	-	11	14	ns
$t_{d(TXD)}$	Transmit data valid delay time	-	11	14	ns

CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

6.3.23 V_{BAT} monitoring characteristics

Table 70. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} (1 mV accuracy)	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Embedded reference voltage

The parameters given in *Table 71* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 71. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

6.3.25 FSMC characteristics

Asynchronous waveforms and timings

Figure 57 through *Figure 60* represent asynchronous waveforms and *Table 72* through *Table 75* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 1
- DataSetupTime = 1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 64. Synchronous non-multiplexed PSRAM write timings

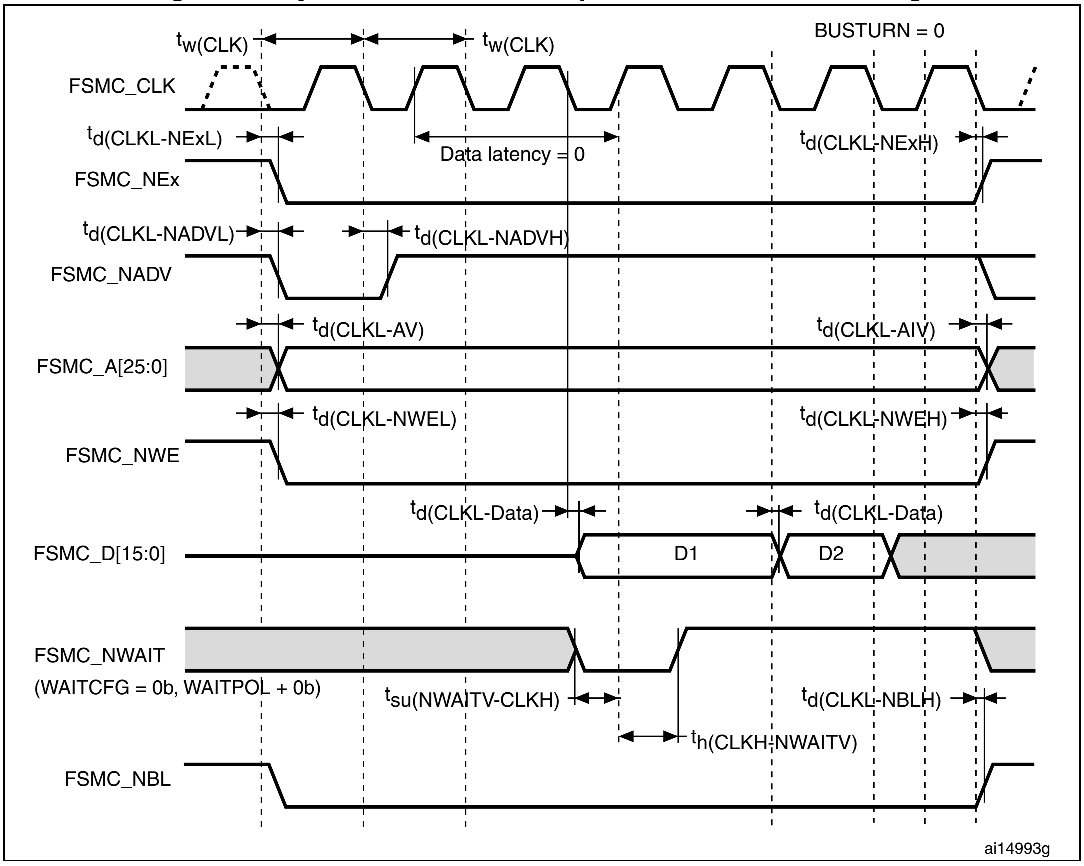


Table 79. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns

Figure 70. PC Card/CompactFlash controller waveforms for I/O space write access

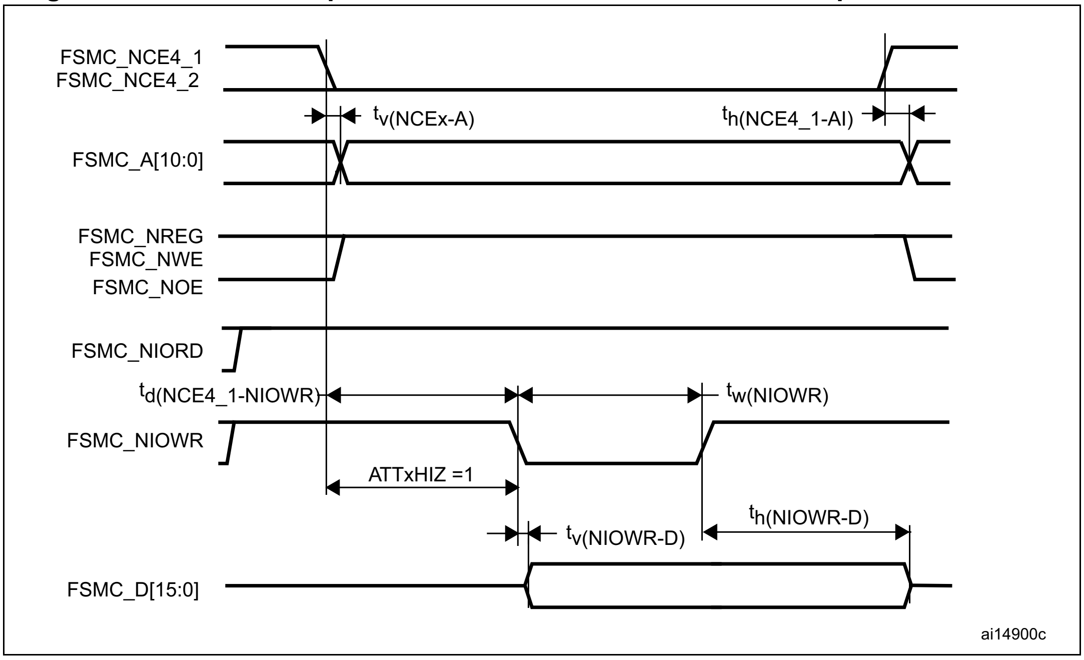


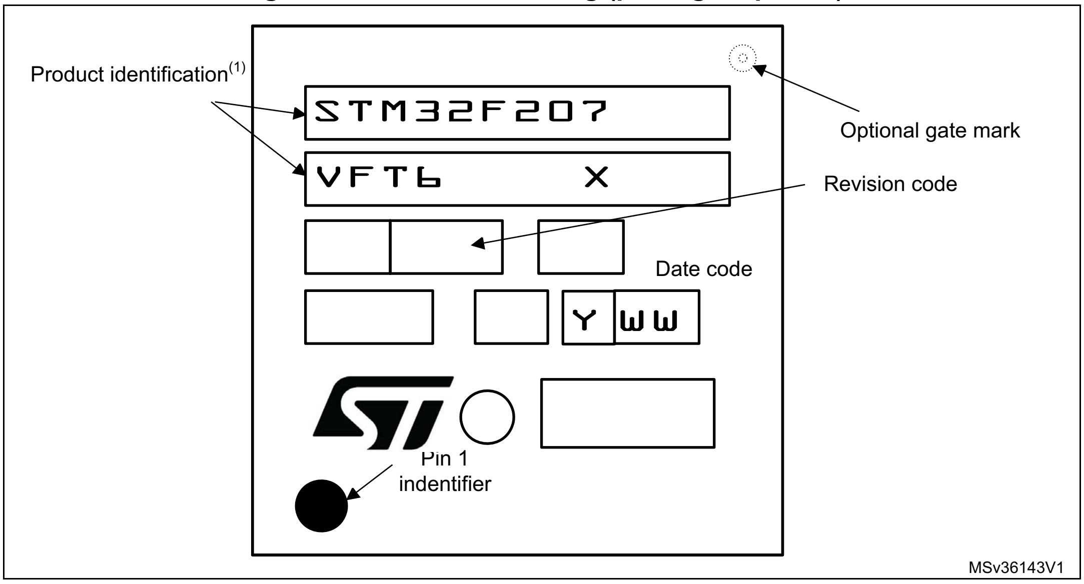
Table 80. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_Ncex low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FSMC_NCEx high to FSMC_Ax invalid	4	-	ns
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	3.5	ns
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	T_{HCLK}+ 4	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	5T_{HCLK}+ 1	ns
$t_{d(NCEx-NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	5T_{HCLK}	ns
$t_{w(NOE)}$	FSMC_NOE low width	8T_{HCLK}– 0.5	8T_{HCLK}+ 1	ns
$t_{d(NOE\_NCEx)}$	FSMC_NOE high to FSMC_NCEx high	5T_{HCLK}+ 2.5	-	ns
$t_{su\ (D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	4	-	ns
$t_{h\ (N0E-D)}$	FSMC_N0E high to FSMC_D[15:0] invalid	2	-	ns
$t_{w(NWE)}$	FSMC_NWE low width	8T_{HCLK}- 1	8T_{HCLK}+ 4	ns
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	5T_{HCLK}+ 1.5	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	5HCLK+ 1	ns
$t_{v\ (NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h\ (NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	8T_{HCLK}	-	ns
$t_{d\ (D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	13T_{HCLK}	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Device marking

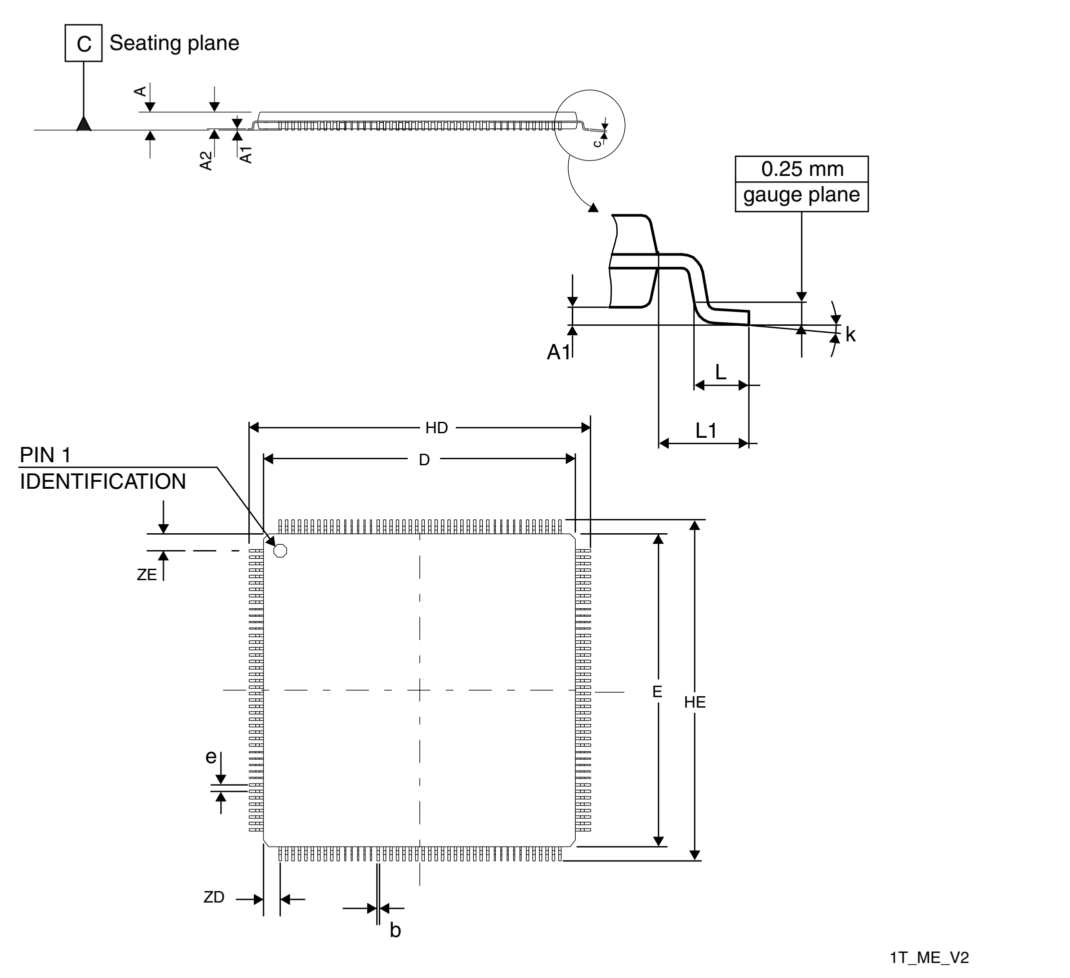
Figure 83. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 LQFP176 package information

Figure 87. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 92. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

Symbol	Dimensions					
	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 97. Document revision history (continued)

Date	Revision	Changes
13-Jul-2010	4 (continued)	Added USB OTG_FS features in *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)*. Updated V_{CAP_1} and V_{CAP_2} capacitor value to 2.2 µF in *Figure 19: Power supply scheme*. Removed DAC, modified ADC limitations, and updated I/O compensation for 1.8 to 2.1 V range in *Table 15: Limitations depending on the operating power supply range*. Added V_{BORL}, V_{BORM}, V_{BORH} and I_{RUSH} in *Table 19: Embedded reset and power control block characteristics*. Removed table Typical current consumption in Sleep mode with Flash memory in Deep power down mode. Merged typical and maximum current consumption sections and added *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*, *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM, Table 22: Typical and maximum current consumption in Sleep mode, Table 23: Typical and maximum current consumptions in Stop mode, Table 24: Typical and maximum current consumptions in Standby mode*, and *Table 25: Typical and maximum current consumptions in VBAT mode*. Update *Table 34: Main PLL characteristics* and added *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Added *Note 8* for CIO in *Table 48: I/O AC characteristics*. Updated *Section 6.3.18: TIM timer characteristics*. Added T_{NRST_OUT} in *Table 49: NRST pin characteristics*. Updated *Table 52: I2C characteristics*. Removed 8-bit data in and data out waveforms from *Figure 48: ULPI timing diagram*. Removed note related to ADC calibration in *Table 67*. *Section 6.3.20: 12-bit ADC characteristics*: ADC characteristics tables merged into one single table; tables ADC conversion time and ADC accuracy removed. Updated *Table 68: DAC characteristics*. Updated *Section 6.3.22: Temperature sensor characteristics* and *Section 6.3.23: VBAT monitoring characteristics*. Update *Section 6.3.26: Camera interface (DCMI) timing specifications*. Added *Section 6.3.27: SD/SDIO MMC card host interface (SDIO) characteristics*, and *Section 6.3.28: RTC characteristics*. Added *Section 7.7: Thermal characteristics*. Updated *Table 91: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data* and *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Changed tape and reel code to TX in *Table 96: Ordering information scheme*. Added *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Updated figures in Appendix *A.2: USB OTG full speed (FS) interface solutions* and *A.3: USB OTG high speed (HS) interface solutions*. Updated *Figure 94: Audio player solution using PLL, PLLI2S, USB and 1 crystal* and *Figure 95: Audio PLL (PLLI2S) providing accurate I2S clock*.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Updated *Typical and maximum current consumption* conditions, as well as *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure 23*, *Figure 24*, *Figure 25*, and *Figure 26*. Updated *Table 22: Typical and maximum current consumption in Sleep mode*, and added *Figure 27* and *Figure 28*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Added *Figure 29: Typical current consumption vs. temperature in Stop mode*. Updated *Table 24: Typical and maximum current consumptions in Standby mode* and *Table 25: Typical and maximum current consumptions in VBAT mode*. Updated *On-chip peripheral current consumption* conditions and *Table 26: Peripheral current consumption*. Updated $t_{WUSTDBY}$ and t_{WUSTOP}, and added *Note 3* in *Table 27: Low-power mode wakeup timings*. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in *Table 28: High-speed external user clock characteristics*. Updated C and g_m in *Table 30: HSE 4-26 MHz oscillator characteristics*. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in *Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added *Note 1* and updated ACC_{HSI}, $IDD_{(HSI)}$, and $t_{su(HSI)}$ in *Table 32: HSI oscillator characteristics*. Added *Figure 34: ACCHSI versus temperature*. Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in *Table 33: LSI oscillator characteristics*. Added *Figure 35: ACCLSI versus temperature* *Table 34: Main PLL characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added *Note 2* for f_{PLL_IN} minimum and maximum values. *Table 35: PLLI2S (audio PLL) characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added *Note 2* for f_{PLLI2S_IN} minimum and maximum values. Added *Note 1* in *Table 36: SSCG parameters constraint*. Updated *Table 37: Flash memory characteristics*. Modified *Table 38: Flash memory programming* and added *Note 2* for t_{prog}. Updated t_{prog} and added *Note 1* in *Table 39: Flash memory programming with VPP*. Modified *Figure 40: Recommended NRST pin protection*. Updated *Table 42: EMI characteristics* and EMI monitoring conditions in *Section : Electromagnetic Interference (EMI)*. Added *Note 2* related to $V_{ESD(HBM)}$in *Table 43: ESD absolute maximum ratings*. Updated *Table 48: I/O AC characteristics*. Added *Section 6.3.15: I/O current injection characteristics*. Modified maximum frequency values and conditions in *Table 48: I/O AC characteristics*. Updated $t_{res(TIM)}$ in *Table 50: Characteristics of TIMx connected to the APB1 domain*. Modified $t_{res(TIM)}$ and f_{EXT} *Table 51: Characteristics of TIMx connected to the APB2 domain*.

Table 97. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	11 (continued)	Removed Appendix A Application block diagrams. Updated *Figure 77: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 87: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 80: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 83: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*.
27-Oct-2014	12	Updated V_{BAT} voltage range in *Figure 19: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 14: General operating conditions*. Removed note 1 in *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Table 45: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 69: Temperature sensor characteristics*. Updated *Figure 79: WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline* and *Table 88: WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data*. Added *Figure 83: LQFP100 marking (package top view)* and *Figure 86: LQFP144 marking (package top view)*.
2-Feb-2016	13	Updated *Section 1: Introduction*. Updated *Table 32: HSI oscillator characteristics* and its footnotes. Updated *Figure 36: PLL output clock waveforms in center spread mode*, *Figure 37: PLL output clock waveforms in down spread mode*, *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.