STMicroelectronics - STM32F205VFT6TR Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vft6tr

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1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

3.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All STM32F20x products embed:

- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Table 8. STM32F20x pin and ball definitions (continued)

Pins: LQFP64	Pins: WLCSP64+2	Pins: LQFP100	Pins: LQFP144	Pins: LQFP176	Pins: UFBGA176	Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	-	131	159	C7	V_{DD}	S	-	-	-	-
-	-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCMI_D13, EVENTOUT	-
55	A4	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/ TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	B4	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	A5	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	-
58	B5	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL,, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT	-
59	A6	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL(6), DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	B6	94	138	166	D6	BOOT0	I	B	-	-	V_{PP}
61	B7	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	A7	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT	-

Table 9. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD13	-	A18	A18	-	Yes
PD14	D0	D0	DA0	D0	Yes
PD15	D1	D1	DA1	D1	Yes
PG2	-	A12	-	-	-
PG3	-	A13	-	-	-
PG4	-	A14	-	-	-
PG5	-	A15	-	-	-
PG6	-	-	-	INT2	-
PG7	-	-	-	INT3	-
PD0	D2	D2	DA2	D2	Yes
PD1	D3	D3	DA3	D3	Yes
PD3	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	NE1	NE1	NCE2	Yes
PG9	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	-	-	-	-
PG12	-	NE4	NE4	-	-
PG13	-	A24	A24	-	-
PG14	-	A25	A25	-	-
PB7	-	NADV	NADV	-	Yes
PE0	-	NBL0	NBL0	-	Yes
PE1	-	NBL1	NBL1	-	Yes

Table 10. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port A	PA0-WKUP	-	TIM2_CH1_ETR	TIM 5_CH1	TIM8_ETR	-	-		USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
Port A	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-		USART2_RTS	UART4_RX	-	-	ETH_MII _RX_CLK ETH_RMII _REF_CLK	-	-	-	EVENTOUT
Port A	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-		USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
Port A	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-		USART2_RX	-	-	OTG_HS_ULPI_D0	ETH _MII_COL	-	-	-	EVENTOUT
Port A	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-		-	OTG_HS_SOF	DCMI_HSYNC	-	EVENTOUT
Port A	PA5	-	TIM2_CH1_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_C K	-	-	-	-	EVENTOUT
Port A	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	EVENTOUT
Port A	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV ETH_RMII _CRS_DV	-	-	-	EVENTOUT
Port A	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
Port A	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-		-	-	DCMI_D0	-	EVENTOUT
Port A	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
Port A	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
Port A	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
Port A	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port A	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port A	PA15	JTDI	TIM 2_CH1 TIM 2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-	-	-	-	-	-	-	-	EVENTOUT

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port H	PH0 - OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1 - OSC_OUT	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-				-	-	-	-	-	-	ETH _MII_CRS	-	-	-	EVENTOUT
	PH3	-	-				-	-	-	-	-	-	ETH _MII_COL	-	-	-	EVENTOUT
	PH4	-	-			I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-			I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH6	-	-			I2C2_SMBA	-	-	-	-	TIM12_CH1	-	ETH _MII_RXD2	-	-	-	EVENTOUT
	PH7	-	-			I2C3_SCL	-	-	-	-	-	-	ETH _MII_RXD3	-	-	-	EVENTOUT
	PH8	-	-			I2C3_SDA	-	-	-	-	-	-	-	-	DCMI_HSYNC	-	EVENTOUT
	PH9	-	-			I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	-	DCMI_D0	-	EVENTOUT
	PH10	-	-	TIM5_CH1			-	-	-	-	-	-	-	-	DCMI_D1	-	EVENTOUT
	PH11	-	-	TIM5_CH2			-	-	-	-	-	-	-	-	DCMI_D2	-	EVENTOUT
	PH12	-	-	TIM5_CH3			-	-	-	-	-	-	-	-	DCMI_D3	-	EVENTOUT
	PH13	-	-		TIM8_CH1N		-	-	-	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-		TIM8_CH2N		-	-	-	-	-	-	-	-	DCMI_D4	-	EVENTOUT
	PH15	-	-		TIM8_CH3N		-	-	-	-	-	-	-	-	DCMI_D11	-	EVENTOUT
Port I	PI0	-	-	TIM5_CH4			SPI2_NSS I2S2_WS	-	-	-	-	-	-	-	DCMI_D13	-	EVENTOUT
	PI1	-	-				SPI2_SCK I2S2_SCK	-	-	-	-	-	-	-	DCMI_D8	-	EVENTOUT
	PI2	-	-		TIM8_CH4		SPI2_MISO	-	-	-	-	-	-	-	DCMI_D9	-	EVENTOUT
	PI3	-	-		TIM8_ETR		SPI2_MOSI I2S2_SD	-	-	-	-	-	-	-	DCMI_D10	-	EVENTOUT
	PI4	-	-		TIM8_BKIN		-	-	-	-	-	-	-	-	DCMI_D5	-	EVENTOUT
	PI5	-	-		TIM8_CH1		-	-	-	-	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	PI6	-	-		TIM8_CH2		-	-	-	-	-	-	-	-	DCMI_D6	-	EVENTOUT
	PI7	-	-		TIM8_CH3		-	-	-	-	-	-	-	-	DCMI_D7	-	EVENTOUT
	PI8	-	-				-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-				-	-	-	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-				-	-	-	-	-	-	ETH _MII_RX_ER	-	-	-	EVENTOUT
	PI11	-	-				-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

Figure 23. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals ON

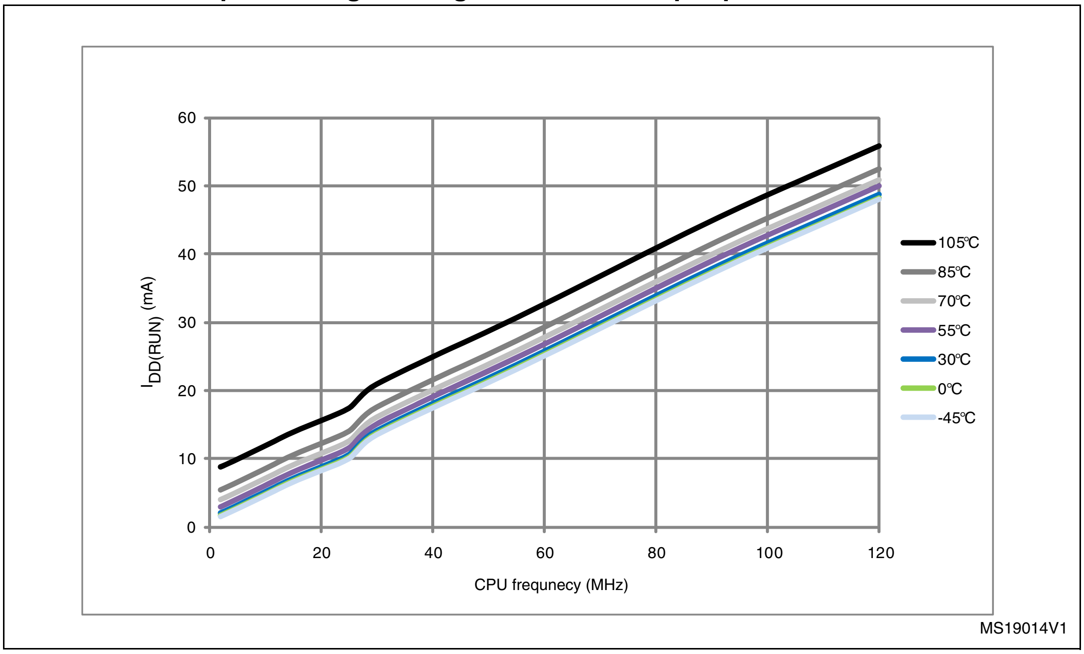


Figure 24. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals OFF

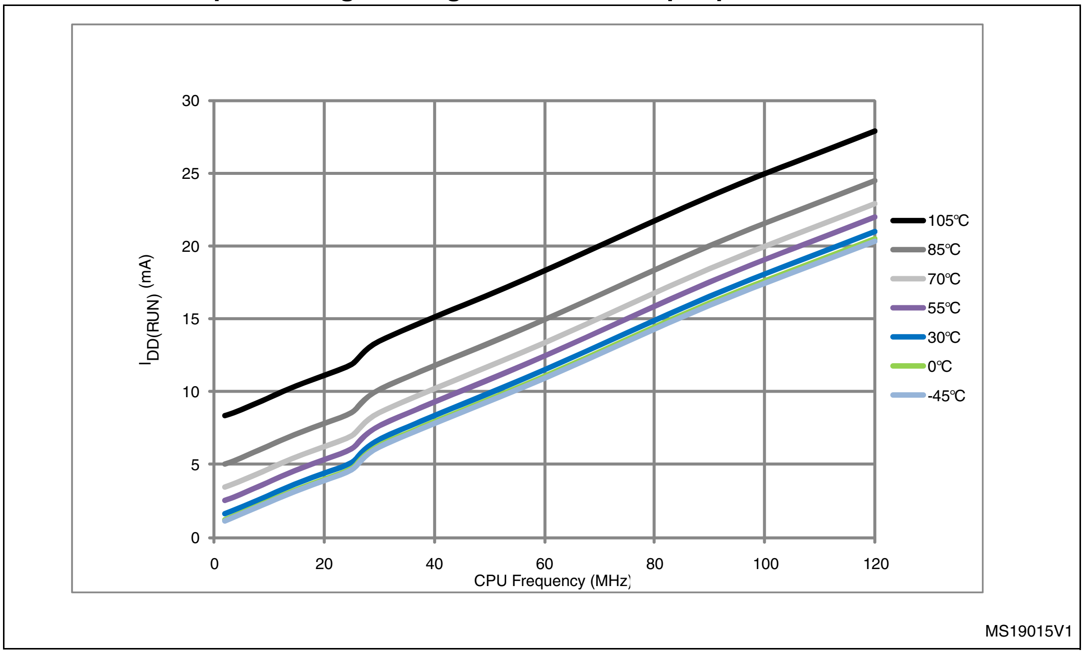


Table 34. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results, not tested in production.

Table 35. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-	0.95(2)	1	2.10(2)	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-	-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output	-	192	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Figure 42. SPI timing diagram - slave mode and CPHA = 0

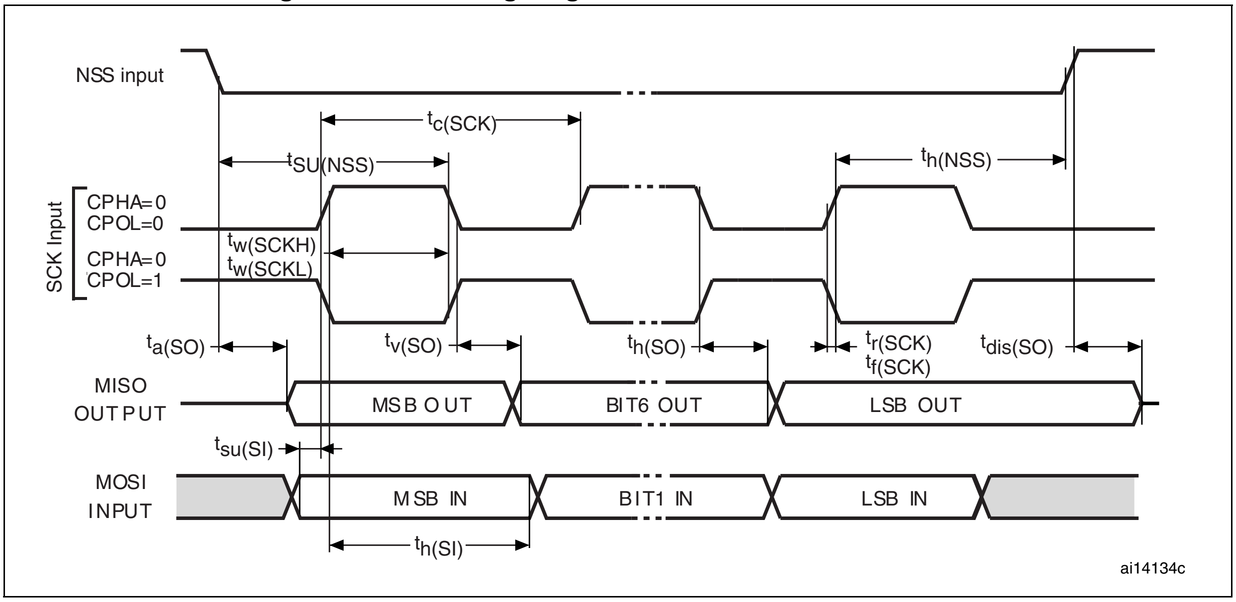


Figure 43. SPI timing diagram - slave mode and CPHA = 1

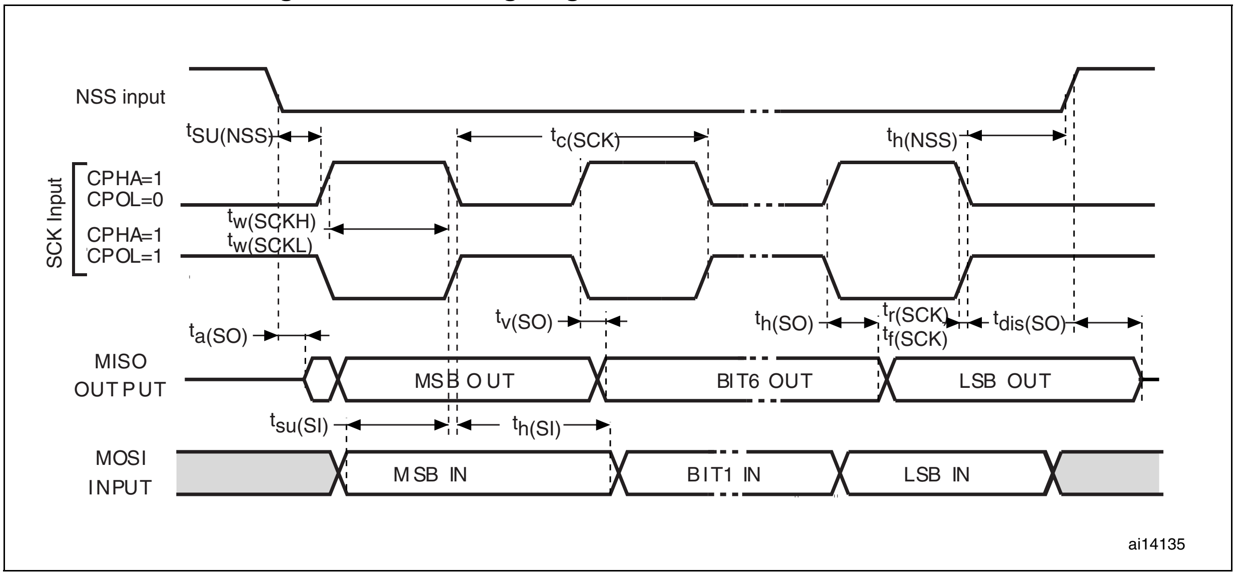


Table 55. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master, 16-bit data, audio frequency = 48 kHz, main clock disabled	1.23	1.24	MHz
		Slave	0	$64F_S$(1)	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF	-	(2)	ns
$t_{v(WS)}$ (3)	WS valid time	Master	0.3	-	
$t_{h(WS)}$ (3)	WS hold time	Master	0	-	
$t_{su(WS)}$ (3)	WS setup time	Slave	3	-	
$t_{h(WS)}$ (3)	WS hold time	Slave	0	-	
$t_{w(CKH)}$ (3) $t_{w(CKL)}$ (3)	CK high and low time	Master f_{PCLK}= 30 MHz	396	-	
$t_{su(SD\_MR)}$ (3) $t_{su(SD\_SR)}$ (3)	Data input setup time	Master receiver Slave receiver	45 0	-	
$t_{h(SD\_MR)}$ (3)(4) $t_{h(SD\_SR)}$ (3)(4)	Data input hold time	Master receiver: f_{PCLK}= 30 MHz, Slave receiver: f_{PCLK}= 30 MHz	13 0	-	
$t_{v(SD\_ST)}$ (3)(4)	Data output valid time	Slave transmitter (after enable edge)	-	30	
$t_{h(SD\_ST)}$ (3)	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_MT)}$ (3)(4)	Data output valid time	Master transmitter (after enable edge)	-	6	
$t_{h(SD\_MT)}$ (3)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. F_S is the sampling frequency. Refer to the I2S section of the STM32F20xxx/21xxx reference manual for more details. f_{CK} values reflect only the digital peripheral behavior which leads to a minimum of (I2SDIV/(2*I2SDIV+ODD), a maximum of (I2SDIV+ODD)/(2*I2SDIV+ODD) and F_S maximum values for each mode/condition.
2. Refer to *Table 48: I/O AC characteristics*.
3. Guaranteed by design, not tested in production.
4. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.

Table 66. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(3)	Sampling rate (f_{ADC} = 30 MHz)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(3)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(3)	ADC VDDA DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. It is recommended to maintain the voltage difference between V_{REF+} and V_{DDA} below 1.8 V.
3. Guaranteed by characterization results, not tested in production.
4. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
5. R_{ADC} maximum value is given for V_{DD}=1.8 V, and minimum value for V_{DD}=3.3 V.
6. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 66*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

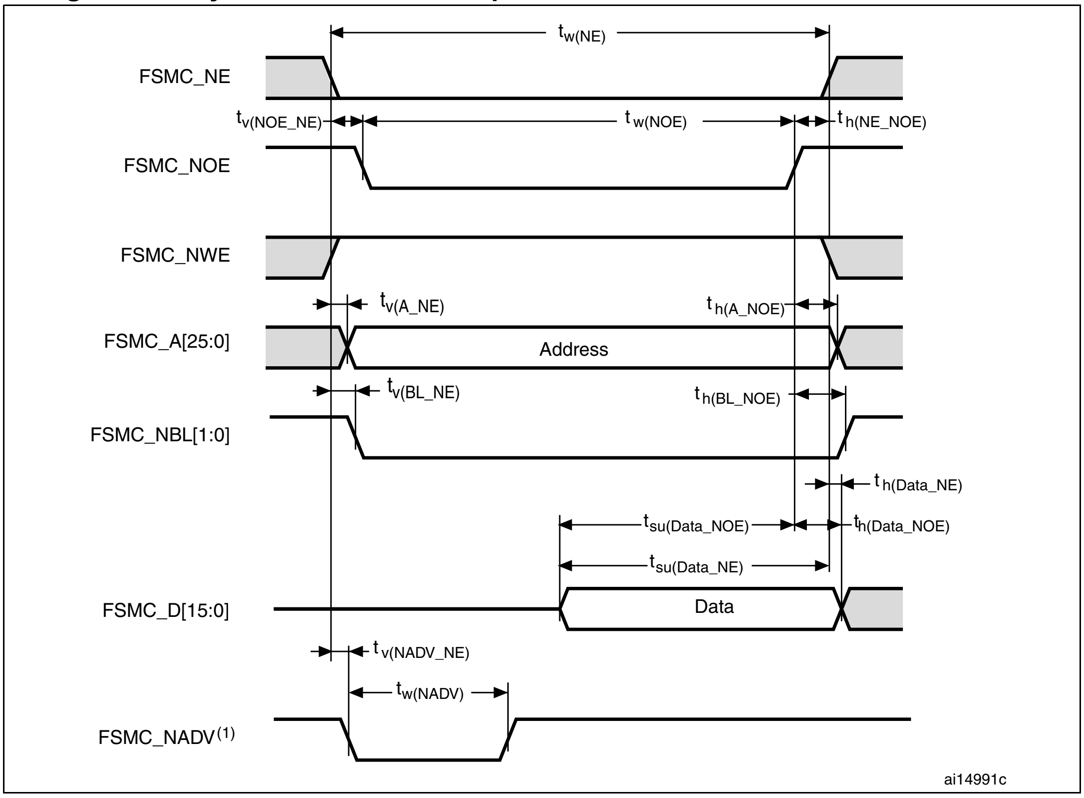
Table 67. ADC accuracy (1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{PCLK2} = 60 MHz, f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.8(3) to 3.6 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results, not tested in production.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion

Figure 57. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2T_{HCLK}$– 0.5	$2T_{HCLK}$+0.5	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	2.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$2T_{HCLK}$- 1	$2T_{HCLK}$+ 0.5	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	4	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK}+ 0.5	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	T_{HCLK}+ 2.5	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	T_{HCLK}– 0.5	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 59. Asynchronous multiplexed PSRAM/NOR read waveforms

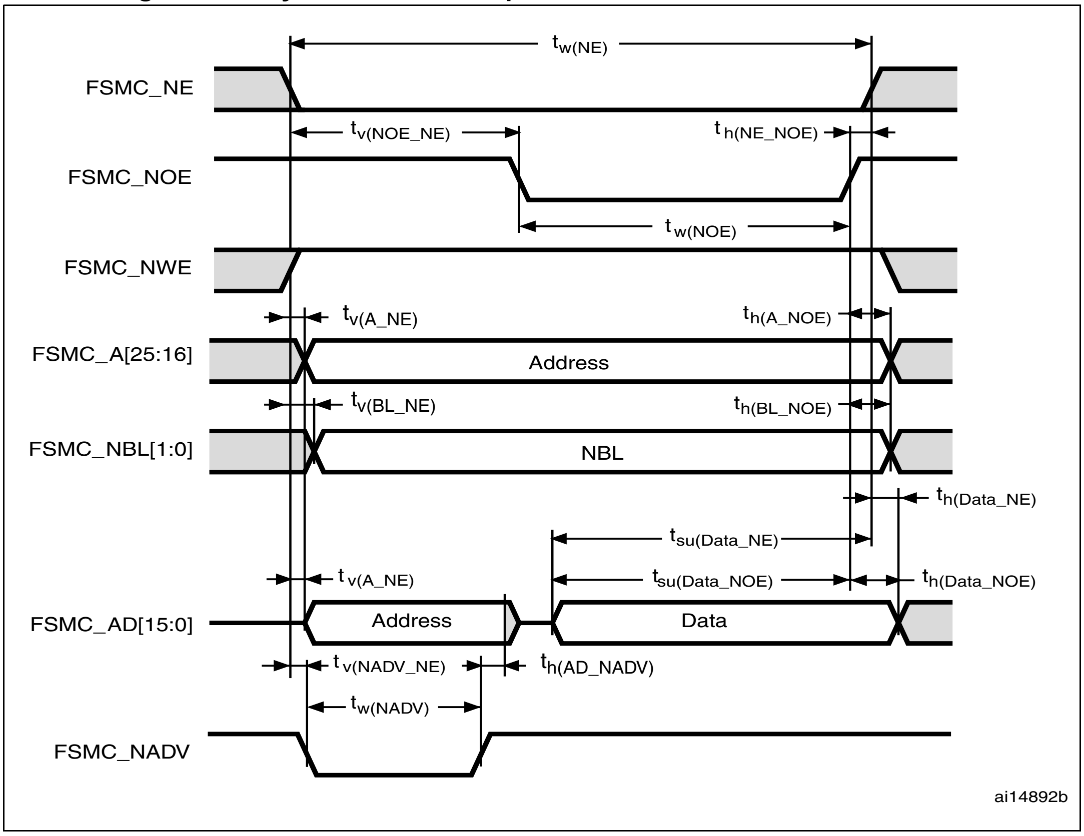


Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$-1	$3T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$2T_{HCLK}$	$2T_{HCLK}$+0.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	T_{HCLK}-1	T_{HCLK}+1	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	2	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 1.5	T_{HCLK}	ns
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	T_{HCLK}	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK}+ 2	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	T_{HCLK}+ 3	-	ns

Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK}- 0.5$	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK}- 1$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK}+2$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK}- 0.5$	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 61 through *Figure 64* represent synchronous waveforms, and *Table 77* through *Table 79* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 77. Synchronous multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	2	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0.5	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 63. Synchronous non-multiplexed NOR/PSRAM read timings

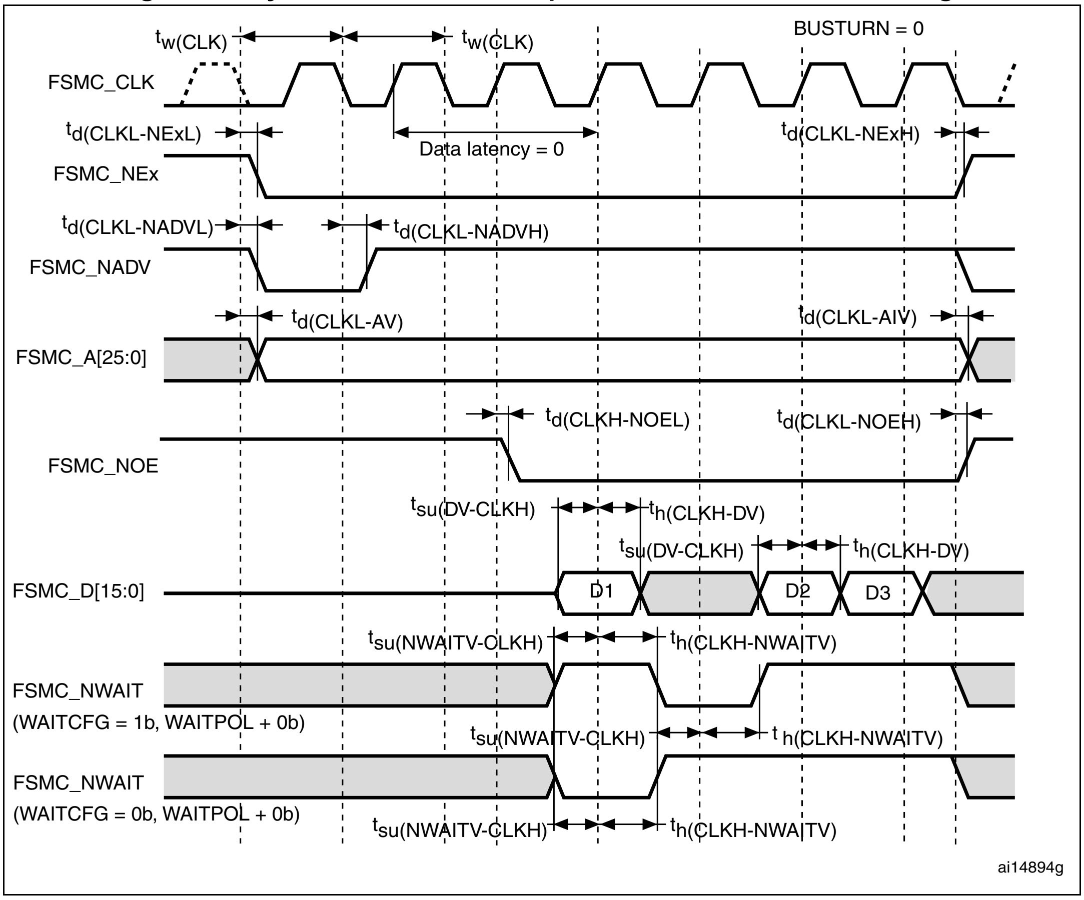


Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2.5	ns

Figure 73. NAND controller waveforms for common memory read access

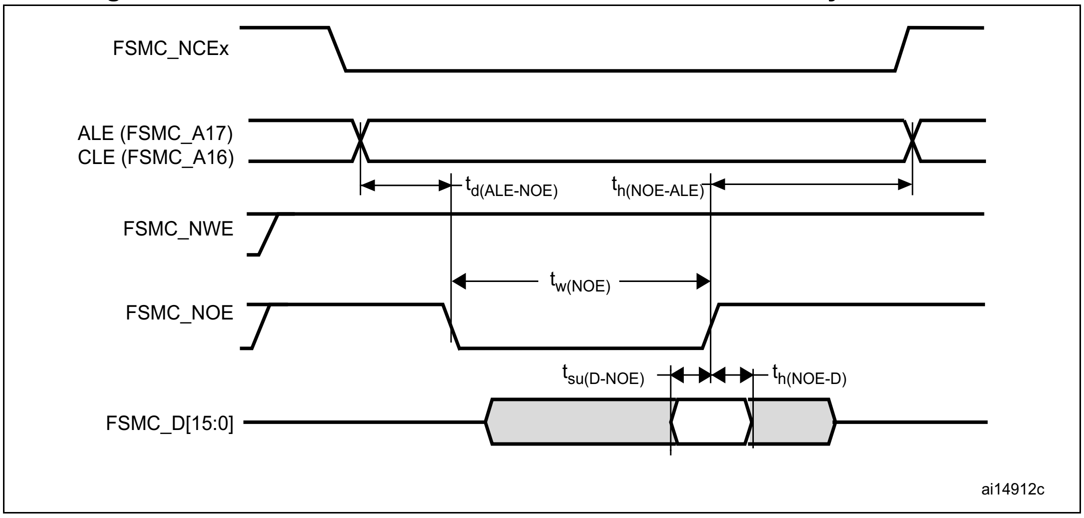


Figure 74. NAND controller waveforms for common memory write access

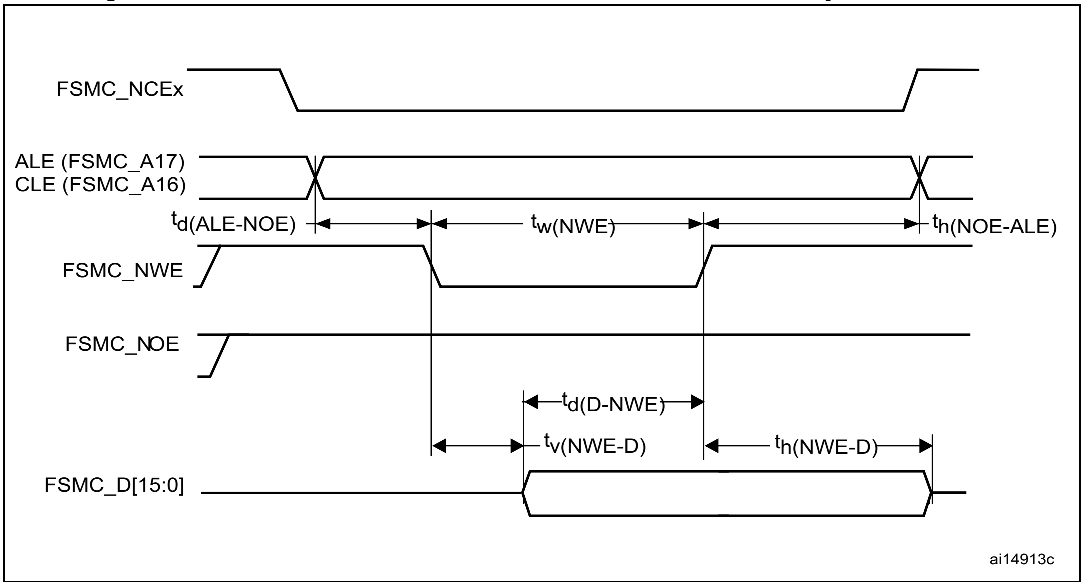


Table 82. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FSMC_NOE low width	$4T_{HCLK}$- 1	$4T_{HCLK}$+ 2	ns
$t_{su(D-NOE)}$	FSMC_D[15-0] valid data before FSMC_NOE high	9	-	ns
$t_{h(NOE-D)}$	FSMC_D[15-0] valid data after FSMC_NOE high	3	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$3T_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}$+ 2	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.220	-	-	0.0087	-
G	-	0.386	-	-	0.0152	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 80. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

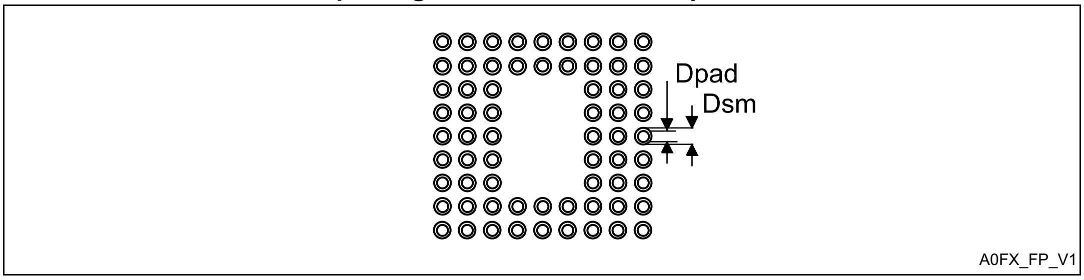
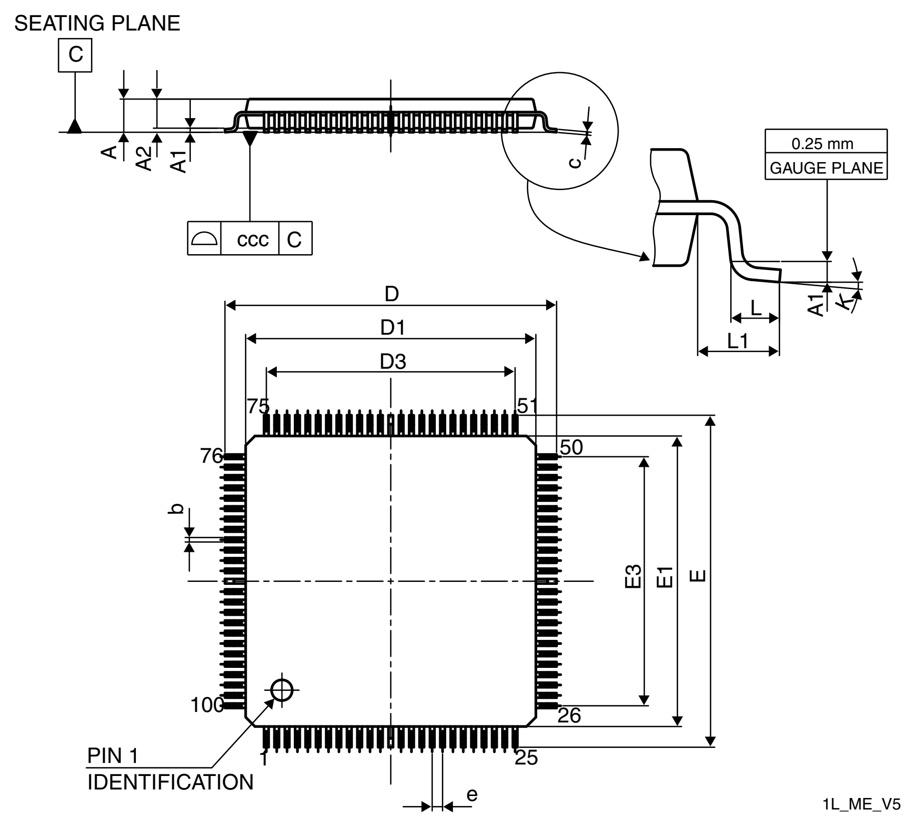


Table 89. WLCSP64 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

7.3 LQFP100 package information

Figure 81. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 90. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591