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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vgt6tr

List of tables

Table 3. STM32F207xx features and peripheral counts (continued)

Peripherals		STM32F207Vx	STM32F207Zx	STM32F207Ix
Comm. interfaces	SPI/(I^{2}S)	3/(2)[2]		
	I^{2}C	3		
	USART UART	4 2		
	USB OTG FS	Yes		
	USB OTG HS	Yes		
	CAN	2		
Camera interface		Yes		
GPIOs		82	114	140
SDIO		Yes		
12-bit ADC Number of channels		3		
		16	24	24
12-bit DAC Number of channels		Yes 2		
Maximum CPU frequency		120 MHz		
Operating voltage		1.8 V to 3.6 V[3]		
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C		
		Junction temperature: –40 to + 125 °C		
Package		LQFP100	LQFP144	LQFP176/ UFBGA176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

3 Functional overview

3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM® core, the STM32F20x family is compatible with all ARM® tools and software.

Figure 4 shows the general block diagram of the STM32F20x family.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M3 processors. It balances the inherent performance advantage of the ARM® Cortex®-M3 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher operating frequencies.

To release the processor full 150 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to *Figure 19: Power supply scheme* for more details.

3.15 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry.

At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit. On devices in WLCSP64+2 package, the BOR, POR and PDR features can be disabled by setting IRROFF pin to V_{DD}. In this mode an external power supply supervisor is required (see *Section 3.16*).

The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.16 Voltage regulator

The regulator has five operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low-power regulator (LPR)
  - Power-down
- Regulator OFF
  - Regulator OFF/internal reset ON
  - Regulator OFF/internal reset OFF

3.16.1 Regulator ON

The regulator ON modes are activated by default on LQFP packages.On WLCSP64+2 package, they are activated by connecting both REGOFF and IRROFF pins to V_{SS}, while only REGOFF must be connected to V_{SS} on UFBGA176 package (IRROFF is not available).

V_{DD} minimum value is 1.8 V.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS}. On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Figure 23. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals ON

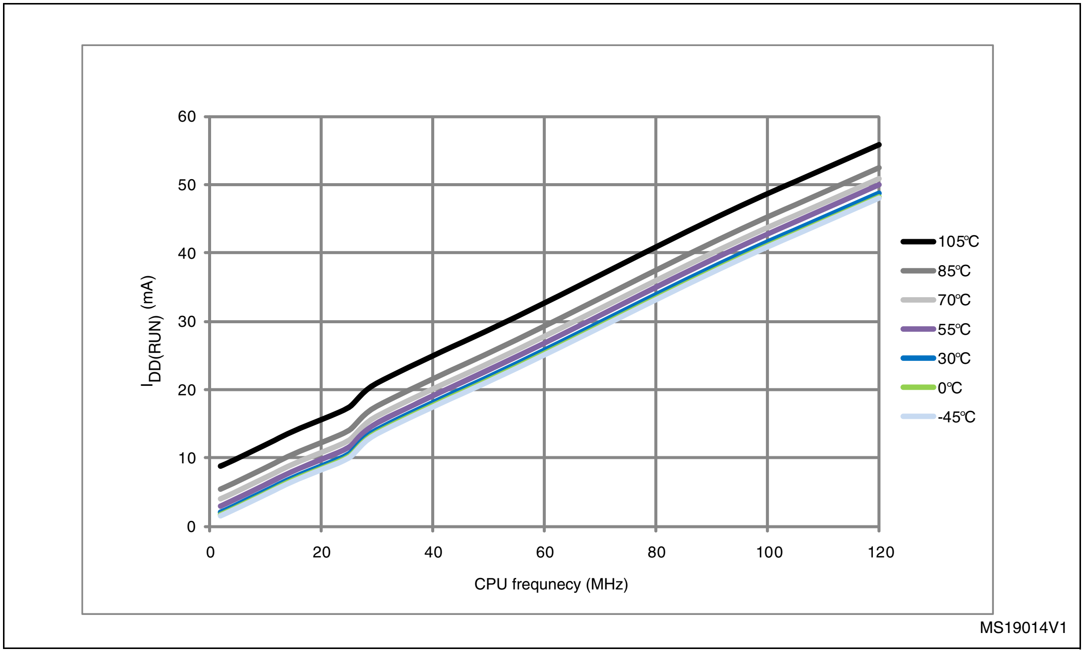
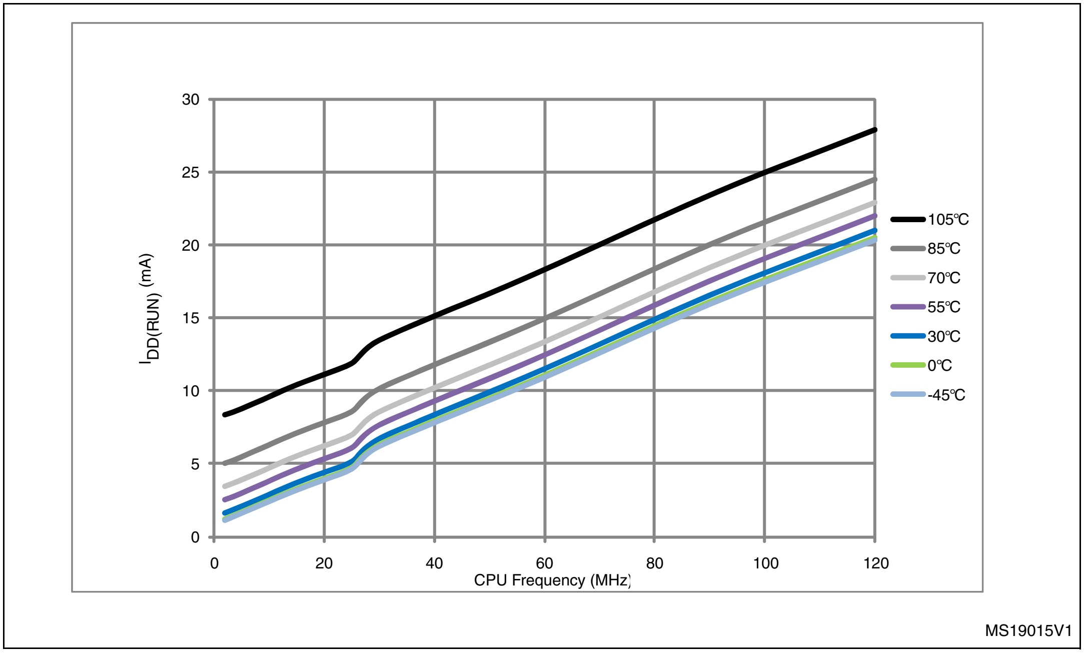


Figure 24. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals OFF



6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 42: EMI characteristics*). It is available only on the main PLL.

Table 36. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[((2^{15} - 1) \times \text{md} \times \text{PLLN}) / (100 \times 5 \times \text{MODEPER})]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126\text{md(quantitazed)}\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLLN})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%\text{(peak)}$$

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*.

Table 45. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	–0	NA	mA
	Injected current on NRST pin	–0	NA	
	Injected current on TTa pins: PA4 and PA5	–0	+5	
	Injected current on all FT pins	–5	NA	

1. NA stands for “not applicable”.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 14: General operating conditions*.

All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}–0.04$(1) $0.3V_{DD}$(2)	V
	BOOT0 I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	-	$0.1V_{DD}+0.1$(1)	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1) $0.7V_{DD}$(2)	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7$(1)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1)	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$10\%V_{DDIO}$(1)(3)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	100(1)	-	-	
I_{lkg}	I/O input leakage current (4)	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)	V_{IN} = 5 V	-	-	3	

Table 46. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor[6]	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor[7]	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
C_{IO}[8]	I/O pin capacitance		-	-	5	-	pF

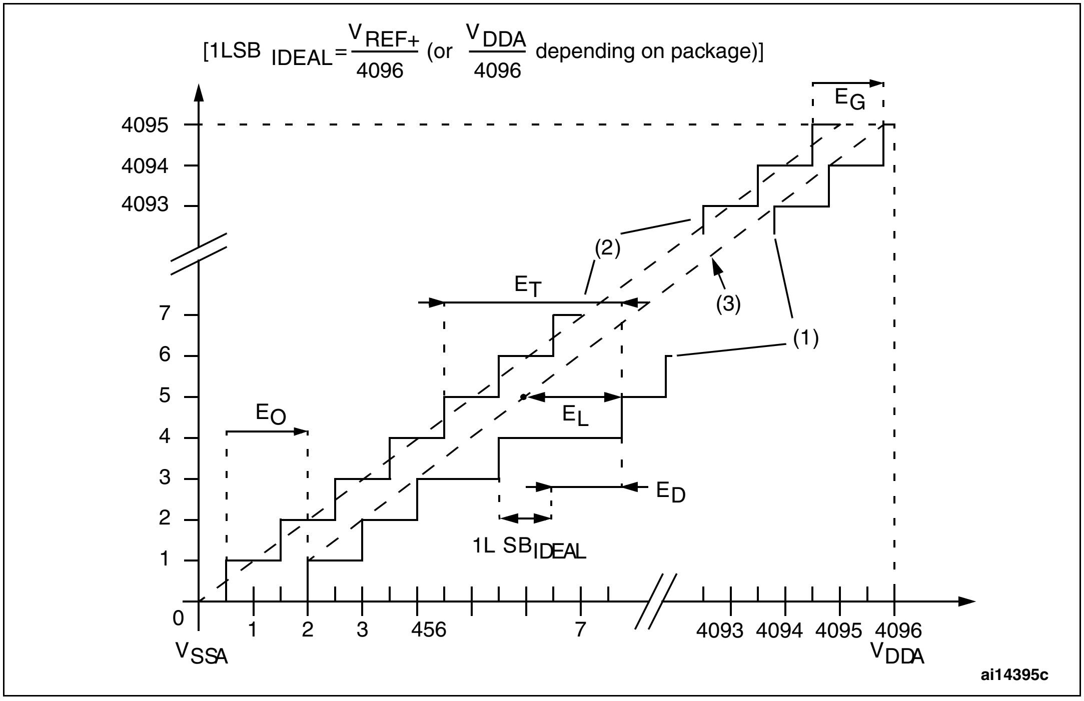
1. Guaranteed by design, not tested in production.
2. Guaranteed by tests in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 45: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 45: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.

being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

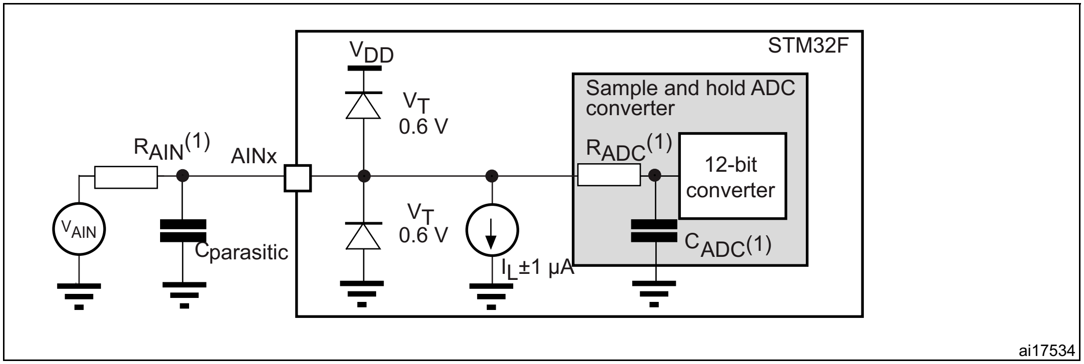
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 52. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 53. Typical connection diagram using the ADC



1. Refer to *Table 66* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 60. Asynchronous multiplexed PSRAM/NOR write waveforms

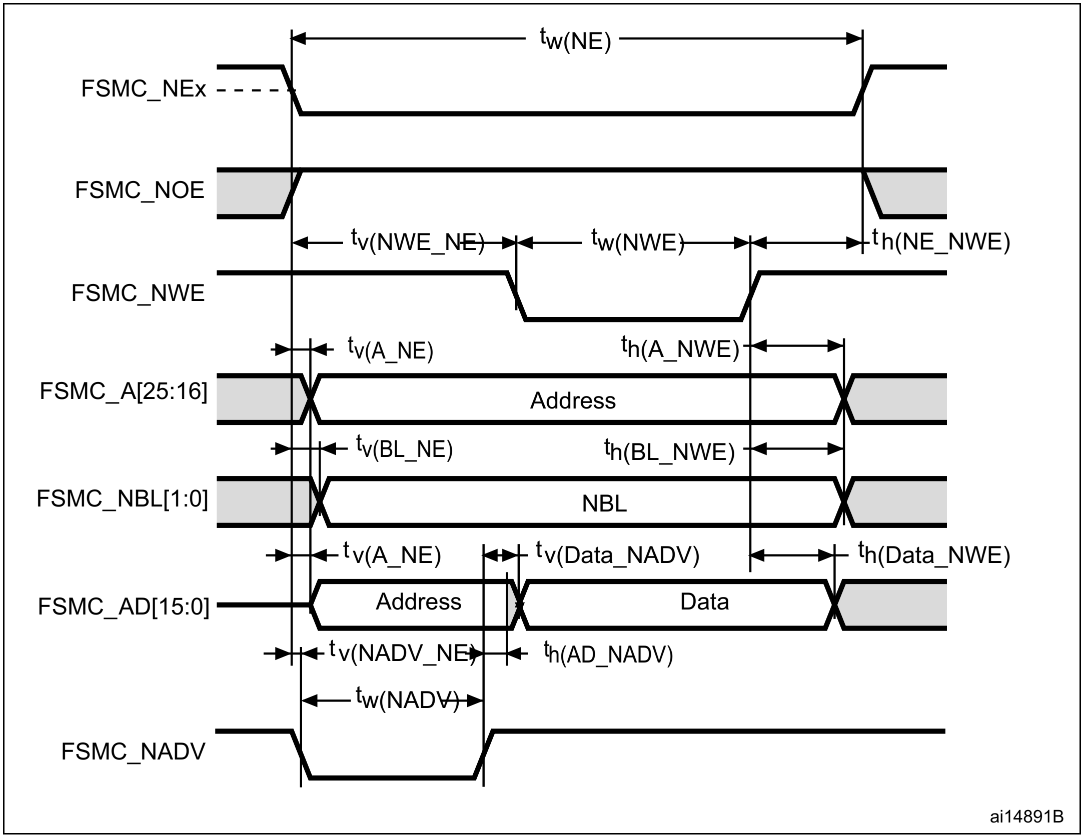


Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4T_{HCLK}$-1	$4T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}- 1	T_{HCLK}	ns
$t_{w(NWE)}$	FSMC_NWE low tim e	$2T_{HCLK}$	$2T_{HCLK}$+1	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}- 1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 2	T_{HCLK}+ 2	ns
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	ns

Table 76. Synchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	5	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 62. Synchronous multiplexed PSRAM write timings

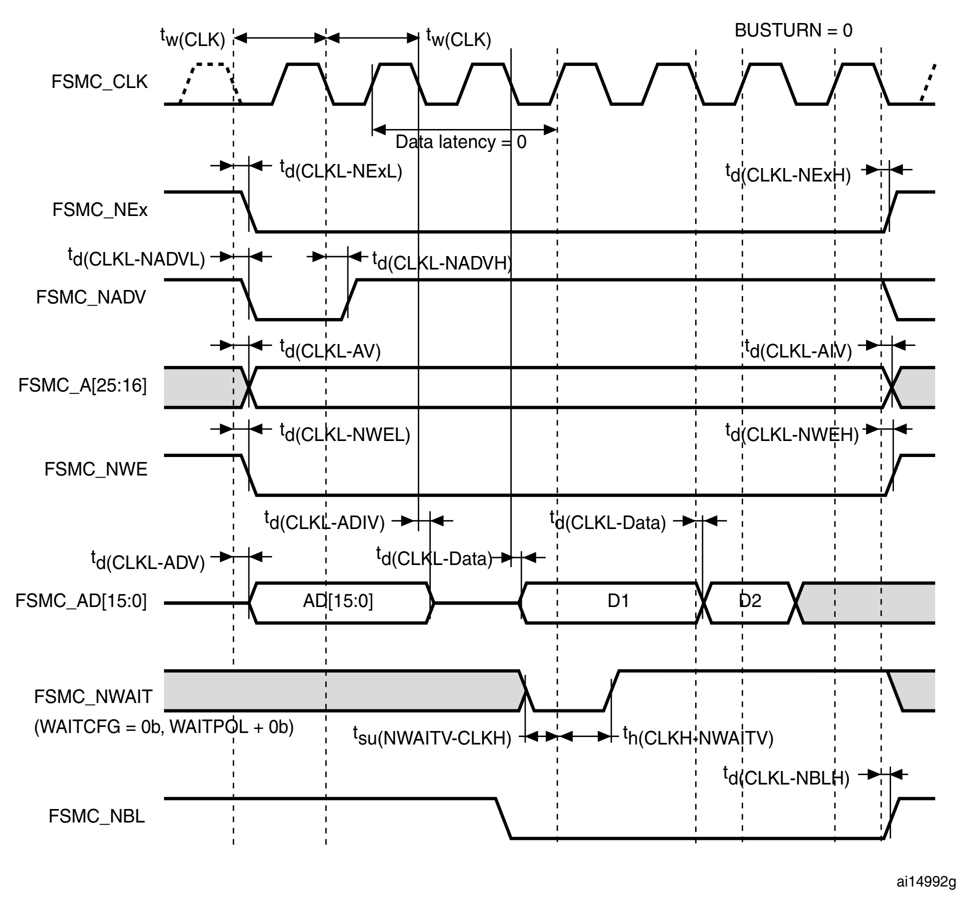


Table 77. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	7	-	ns

Figure 70. PC Card/CompactFlash controller waveforms for I/O space write access

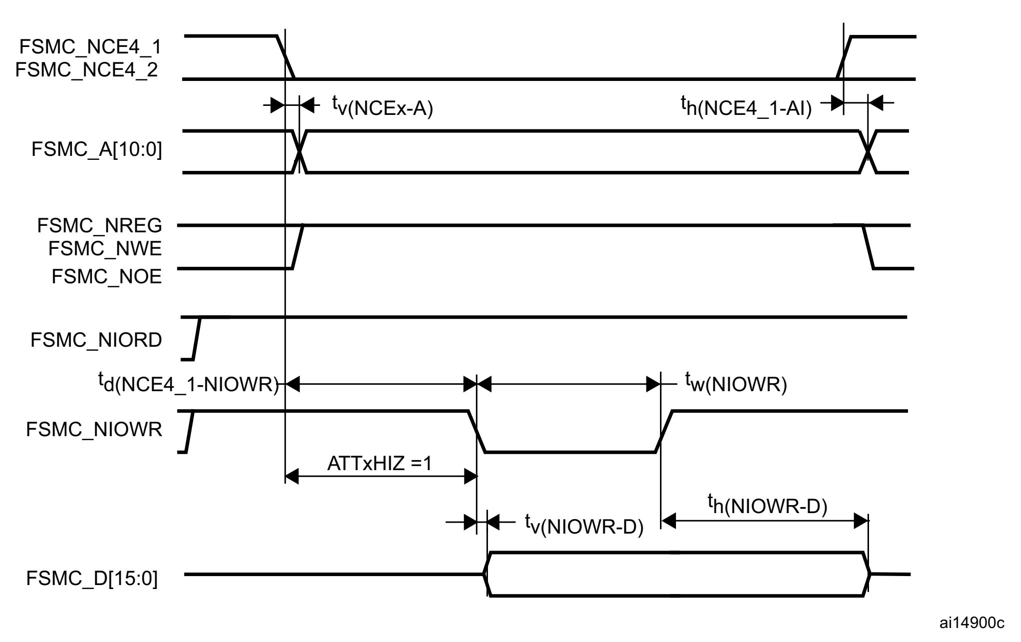


Table 80. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_Ncex low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FSMC_NCEx high to FSMC_Ax invalid	4	-	ns
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	3.5	ns
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	T_{HCLK}+ 4	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK}$+ 1	ns
$t_{d(NCEx-NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5T_{HCLK}$	ns
$t_{w(NOE)}$	FSMC_NOE low width	$8T_{HCLK}$– 0.5	$8T_{HCLK}$+ 1	ns
$t_{d(NOE\_NCEx)}$	FSMC_NOE high to FSMC_NCEx high	$5T_{HCLK}$+ 2.5	-	ns
$t_{su\ (D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	4	-	ns
$t_{h\ (N0E-D)}$	FSMC_N0E high to FSMC_D[15:0] invalid	2	-	ns
$t_{w(NWE)}$	FSMC_NWE low width	$8T_{HCLK}$- 1	$8T_{HCLK}$+ 4	ns
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5T_{HCLK}$+ 1.5	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	5HCLK+ 1	ns
$t_{v\ (NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h\ (NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$8T_{HCLK}$	-	ns
$t_{d\ (D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13T_{HCLK}$	-	ns

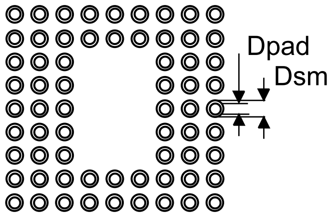
1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.220	-	-	0.0087	-
G	-	0.386	-	-	0.0152	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 80. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



A0FX_FP_V1

Table 89. WLCSP64 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in ° C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 95. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch	51	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 97. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	10 (continued)	Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in *Table 76: Synchronous multiplexed NOR/PSRAM read timings*, *Table 78: Synchronous non-multiplexed NOR/PSRAM read timings*, *Figure 61: Synchronous multiplexed NOR/PSRAM read timings* and *Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings*. Added *Figure 87: LQFP176 recommended footprint*. Added *Note 2* below *Figure 86: Regulator OFF/internal reset ON*. Updated device subfamily in *Table 96: Ordering information scheme*. Remove reference to note 2 for USB IOTG FS in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*.