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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 132K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vgt6v |

### 3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

**Table 4. Regulator ON/OFF and internal reset ON/OFF availability**

| Package | Regulator ON/internal reset ON | Regulator OFF/internal reset ON | Regulator OFF/internal reset OFF |
|---|---|---|---|
| LQFP64<br>LQFP100<br>LQFP144<br>LQFP176 | Yes | No | No |
| WLCSP 64+2 | Yes<br>REGOFF and IRROFF set to $V_{SS}$ | Yes<br>REGOFF set to $V_{DD}$ and IRROFF set to $V_{SS}$ | Yes<br>REGOFF set to $V_{SS}$ and IRROFF set to $V_{DD}$ |
| UFBGA176 | Yes<br>REGOFF set to $V_{SS}$ | Yes<br>REGOFF set to $V_{DD}$ | No |

## 3.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F20x devices includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Its main features are the following:

- Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.
- It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.
- Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.
- A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The 4-Kbyte backup SRAM is an EEPROM-like area.It can be used to store data which need to be retained in VBAT and standby mode.This memory area is disabled to minimize power consumption (see *Section 3.18: Low-power modes*). It can be enabled by software.

CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

## 3.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

## 3.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F20x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024× 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Table 8. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | 38 | 58 | 68 | R8 | PE7 | I/O | FT | - | FSMC_D4,TIM1_ETR, EVENTOUT | - |
| - | - | 39 | 59 | 69 | P8 | PE8 | I/O | FT | - | FSMC_D5,TIM1_CH1N, EVENTOUT | - |
| - | - | 40 | 60 | 70 | P9 | PE9 | I/O | FT | - | FSMC_D6,TIM1_CH1, EVENTOUT | - |
| - | - | - | 61 | 71 | M9 | $V_{SS}$ | S | | - | - | - |
| - | - | - | 62 | 72 | N9 | $V_{DD}$ | S | | - | - | - |
| - | - | 41 | 63 | 73 | R9 | PE10 | I/O | FT | - | FSMC_D7,TIM1_CH2N, EVENTOUT | - |
| - | - | 42 | 64 | 74 | P10 | PE11 | I/O | FT | - | FSMC_D8,TIM1_CH2, EVENTOUT | - |
| - | - | 43 | 65 | 75 | R10 | PE12 | I/O | FT | - | FSMC_D9,TIM1_CH3N, EVENTOUT | - |
| - | - | 44 | 66 | 76 | N11 | PE13 | I/O | FT | - | FSMC_D10,TIM1_CH3, EVENTOUT | - |
| - | - | 45 | 67 | 77 | P11 | PE14 | I/O | FT | - | FSMC_D11,TIM1_CH4, EVENTOUT | - |
| - | - | 46 | 68 | 78 | R11 | PE15 | I/O | FT | - | FSMC_D12,TIM1_BKIN, EVENTOUT | - |
| 29 | H3 | 47 | 69 | 79 | R12 | PB10 | I/O | FT | - | SPI2_SCK, I2S2_SCK, I2C2_SCL,USART3_TX,OTG_HS_ULPI_D3,ETH_MII_RX_ER,TIM2_CH3, EVENTOUT | - |
| 30 | J2 | 48 | 70 | 80 | R13 | PB11 | I/O | FT | - | I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_RMII_TX_EN, ETH_MII_TX_EN, TIM2_CH4, EVENTOUT | - |
| 31 | J3 | 49 | 71 | 81 | M10 | $V_{CAP\_1}$ | S | | - | - | - |
| 32 | - | 50 | 72 | 82 | N10 | $V_{DD}$ | S | | - | - | - |
| - | - | - | - | 83 | M11 | PH6 | I/O | FT | - | I2C2_SMBA, TIM12_CH1, ETH_MII_RXD2, EVENTOUT | - |

Table 8. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | 56 | 78 | 97 | P14 | PD9 | I/O | FT | - | FSMC_D14, USART3_RX, EVENTOUT | - |
| - | - | 57 | 79 | 98 | N15 | PD10 | I/O | FT | - | FSMC_D15, USART3_CK, EVENTOUT | - |
| - | - | 58 | 80 | 99 | N14 | PD11 | I/O | FT | - | FSMC_A16,USART3_CTS, EVENTOUT | - |
| - | - | 59 | 81 | 100 | N13 | PD12 | I/O | FT | - | FSMC_A17,TIM4_CH1, USART3_RTS, EVENTOUT | - |
| - | - | 60 | 82 | 101 | M15 | PD13 | I/O | FT | - | FSMC_A18,TIM4_CH2, EVENTOUT | - |
| - | - | - | 83 | 102 | - | $V_{SS}$ | S | - | - | - | - |
| - | - | - | 84 | 103 | J13 | $V_{DD}$ | S | - | - | - | - |
| - | - | 61 | 85 | 104 | M14 | PD14 | I/O | FT | - | FSMC_D0,TIM4_CH3, EVENTOUT | - |
| - | - | 62 | 86 | 105 | L14 | PD15 | I/O | FT | - | FSMC_D1,TIM4_CH4, EVENTOUT | - |
| - | - | - | 87 | 106 | L15 | PG2 | I/O | FT | - | FSMC_A12, EVENTOUT | - |
| - | - | - | 88 | 107 | K15 | PG3 | I/O | FT | - | FSMC_A13, EVENTOUT | - |
| - | - | - | 89 | 108 | K14 | PG4 | I/O | FT | - | FSMC_A14, EVENTOUT | - |
| - | - | - | 90 | 109 | K13 | PG5 | I/O | FT | - | FSMC_A15, EVENTOUT | - |
| - | - | - | 91 | 110 | J15 | PG6 | I/O | FT | - | FSMC_INT2, EVENTOUT | - |
| - | - | - | 92 | 111 | J14 | PG7 | I/O | FT | - | FSMC_INT3 ,USART6_CK, EVENTOUT | - |
| - | - | - | 93 | 112 | H14 | PG8 | I/O | FT | - | USART6_RTS, ETH_PPS_OUT, EVENTOUT | - |
| - | - | - | 94 | 113 | G12 | $V_{SS}$ | S | - | - | - | - |
| - | - | - | 95 | 114 | H13 | $V_{DD}$ | S | - | - | - | - |
| 37 | G2 | 63 | 96 | 115 | H15 | PC6 | I/O | FT | - | I2S2_MCK, TIM8_CH1, SDIO_D6, USART6_TX, DCMI_D0, TIM3_CH1, EVENTOUT | - |

Table 8. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 38 | F2 | 64 | 97 | 116 | G15 | PC7 | I/O | FT | - | I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT | - |
| 39 | F3 | 65 | 98 | 117 | G14 | PC8 | I/O | FT | - | TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT | - |
| 40 | D1 | 66 | 99 | 118 | F14 | PC9 | I/O | FT | - | I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT | - |
| 41 | E2 | 67 | 100 | 119 | F15 | PA8 | I/O | FT | - | MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT | - |
| 42 | E3 | 68 | 101 | 120 | E15 | PA9 | I/O | FT | - | USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT | OTG_FS_ VBUS |
| 43 | D3 | 69 | 102 | 121 | D15 | PA10 | I/O | FT | - | USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT | - |
| 44 | D2 | 70 | 103 | 122 | C15 | PA11 | I/O | FT | - | USART1_CTS, CAN1_RX, TIM1_CH4,OTG_FS_DM, EVENTOUT | - |
| 45 | C1 | 71 | 104 | 123 | B15 | PA12 | I/O | FT | - | USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT | - |
| 46 | B2 | 72 | 105 | 124 | A15 | PA13 (JTMS-SWDIO) | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| 47 | C2 | 73 | 106 | 125 | F13 | $V_{CAP\_2}$ | S | - | - | - | - |
| - | B1 | 74 | 107 | 126 | F12 | $V_{SS}$ | S | - | - | - | - |
| 48 | A8 | 75 | 108 | 127 | G13 | $V_{DD}$ | S | - | - | - | - |
| - | - | - | - | 128 | E12 | PH13 | I/O | FT | - | TIM8_CH1N, CAN1_TX, EVENTOUT | - |
| - | - | - | - | 129 | E13 | PH14 | I/O | FT | - | TIM8_CH2N, DCMI_D4, EVENTOUT | - |

## Table 10. Alternate function mapping

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| Port A | PA0-WKUP | - | TIM2_CH1_ETR | TIM 5_CH1 | TIM8_ETR | - | - | | USART2_CTS | UART4_TX | - | - | ETH_MII_CRS | - | - | - | EVENTOUT |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | | USART2_RTS | UART4_RX | - | - | ETH_MII _RX_CLK ETH_RMII _REF_CLK | - | - | - | EVENTOUT |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | | USART2_TX | - | - | - | ETH_MDIO | - | - | - | EVENTOUT |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | | USART2_RX | - | - | OTG_HS_ULPI_D0 | ETH _MII_COL | - | - | - | EVENTOUT |
| | PA4 | - | - | - | - | - | SPI1_NSS | SPI3_NSS I2S3_WS | USART2_CK | - | - | | - | OTG_HS_SOF | DCMI_HSYNC | - | EVENTOUT |
| | PA5 | - | TIM2_CH1_ETR | - | TIM8_CH1N | - | SPI1_SCK | - | - | - | - | OTG_HS_ULPI_C K | - | - | - | - | EVENTOUT |
| | PA6 | - | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | - | SPI1_MISO | - | - | - | TIM13_CH1 | - | - | - | DCMI_PIXCK | - | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI | - | - | - | TIM14_CH1 | - | ETH_MII _RX_DV ETH_RMII _CRS_DV | - | - | - | EVENTOUT |
| | PA8 | MCO1 | TIM1_CH1 | - | - | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | - | - | - | - | EVENTOUT |
| | PA9 | - | TIM1_CH2 | - | - | I2C3_SMBA | - | - | USART1_TX | - | - | | - | - | DCMI_D0 | - | EVENTOUT |
| | PA10 | - | TIM1_CH3 | - | - | - | - | - | USART1_RX | - | - | OTG_FS_ID | - | - | DCMI_D1 | - | EVENTOUT |
| | PA11 | - | TIM1_CH4 | - | - | - | - | - | USART1_CTS | - | CAN1_RX | OTG_FS_DM | - | - | - | - | EVENTOUT |
| | PA12 | - | TIM1_ETR | - | - | - | - | - | USART1_RTS | - | CAN1_TX | OTG_FS_DP | - | - | - | - | EVENTOUT |
| | PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA15 | JTDI | TIM 2_CH1 TIM 2_ETR | - | - | - | SPI1_NSS | SPI3_NSS I2S3_WS | - | - | - | - | - | - | - | - | EVENTOUT |

**Figure 16. Memory map**

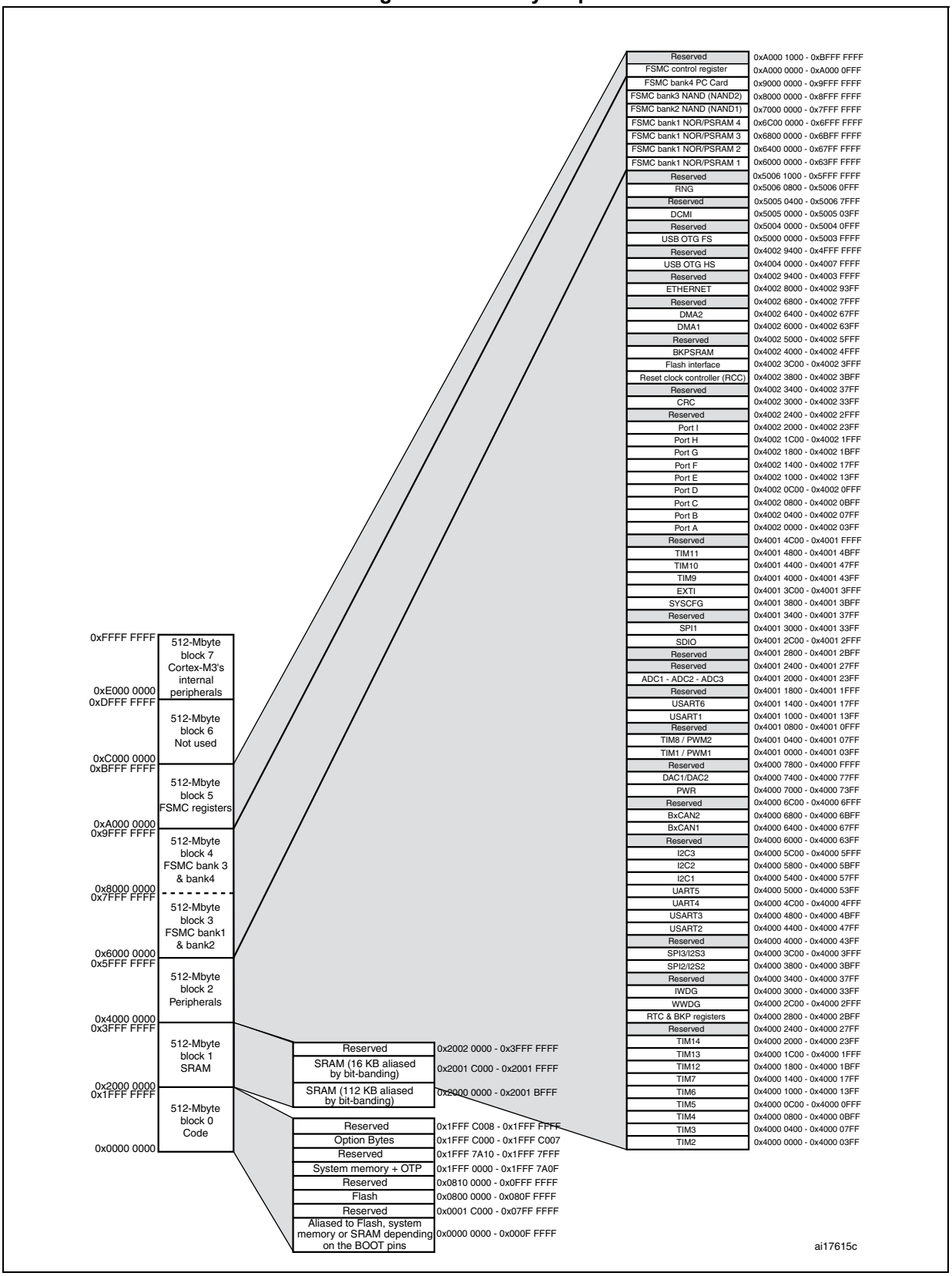


**Table 15. Limitations depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency ($f_{Flashmax}$) | Number of wait states at maximum CPU frequency ($f_{CPUmax}$= 120 MHz)(1) | I/O operation | FSMC_CLK frequency for synchronous accesses | Possible Flash memory operations |
|---|---|---|---|---|---|---|
| $V_{DD}$ =1.8 to 2.1 V(2) | Conversion time up to 1 Msps | 16 MHz with no Flash memory wait state | 7(3) | – Degraded speed performance<br>– No I/O compensation | Up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1 Msps | 18 MHz with no Flash memory wait state | 6(3) | – Degraded speed performance<br>– No I/O compensation | Up to 30 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2 Msps | 24 MHz with no Flash memory wait state | 4(3) | – Degraded speed performance<br>– I/O compensation works | Up to 48 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(4) | Conversion time up to 2 Msps | 30 MHz with no Flash memory wait state | 3(3) | – Full-speed operation<br>– I/O compensation works | – Up to 60 MHz when $V_{DD}$ = 3.0 to 3.6 V<br>– Up to 48 MHz when $V_{DD}$ = 2.7 to 3.0 V | 32-bit erase and program operations |

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to $V_{DD}$, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz and 3 wait states from 90 to 120 MHz).
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

**Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM (1)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | Max(2) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | External clock(3), all peripherals enabled(4) | 120 MHz | 49 | 63 | 72 | mA |
| | | | 90 MHz | 38 | 51 | 61 | |
| | | | 60 MHz | 26 | 39 | 49 | |
| | | | 30 MHz | 14 | 27 | 37 | |
| | | | 25 MHz | 11 | 24 | 34 | |
| | | | 16 MHz(5) | 8 | 21 | 30 | |
| | | | 8 MHz | 5 | 17 | 27 | |
| | | | 4 MHz | 3 | 16 | 26 | |
| | | | 2 MHz | 2 | 15 | 25 | |
| | | External clock(3), all peripherals disabled | 120 MHz | 21 | 34 | 44 | |
| | | | 90 MHz | 17 | 30 | 40 | |
| | | | 60 MHz | 12 | 25 | 35 | |
| | | | 30 MHz | 7 | 20 | 30 | |
| | | | 25 MHz | 5 | 18 | 28 | |
| | | | 16 MHz(5) | 4.0 | 17.0 | 27.0 | |
| | | | 8 MHz | 2.5 | 15.5 | 25.5 | |
| | | | 4 MHz | 2.0 | 14.7 | 24.8 | |
| | | | 2 MHz | 1.6 | 14.5 | 24.6 | |

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed by characterization, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
3. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
4. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. In this case HCLK = system clock/2.

Figure 30. High-speed external clock source AC timing diagram

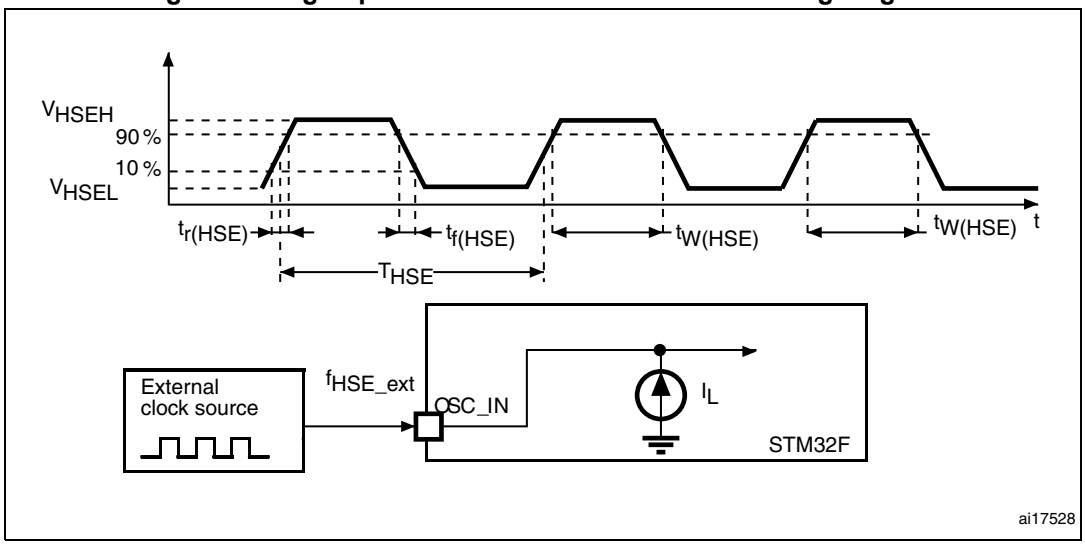
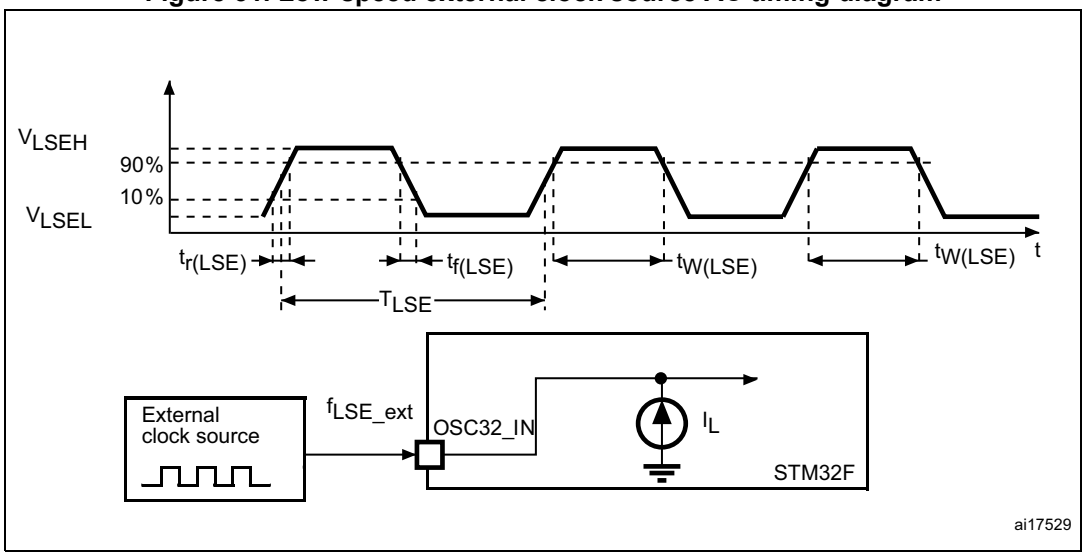



Figure 31. Low-speed external clock source AC timing diagram




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 30*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

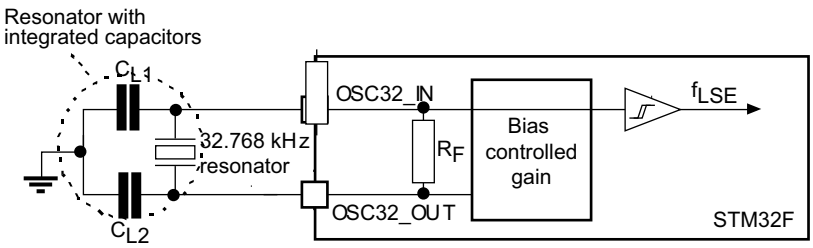
**Table 31. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 18.4 | - | MΩ |
| $I_{DD}$ | LSE current consumption | - | - | - | 1 | µA |
| $g_m$ | Oscillator Transconductance | - | 2.8 | - | - | µA/V |
| $t_{SU(LSE)}$ (2) | startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

*Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 33. Typical application with a 32.768 kHz crystal**




## 6.3.9 Internal clock source characteristics

The parameters given in *Table 32* and *Table 33* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 14*.

### High-speed internal (HSI) RC oscillator

**Table 32. HSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HSI}$ | HSI user-trimming step(2) | - | - | - | 1 | % |
| | Accuracy of the HSI oscillator | $T_A$ = –40 to 105 °C(3) | – 8 | - | 4.5 | % |
| | | $T_A$ = –10 to 85 °C(3) | – 4 | - | 4 | % |
| | | $T_A$ = 25 °C(4) | – 1 | - | 1 | % |
| $t_{su(HSI)}$ (2) | HSI oscillator startup time | - | - | 2.2 | 4.0 | µs |
| $I_{DD(HSI)}$ (2) | HSI oscillator power consumption | - | - | 60 | 80 | µA |

1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

## USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

**Table 56. USB OTG FS startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB OTG FS transceiver startup time | 1 | µs |

1. Guaranteed by design, not tested in production.

**Table 57. USB OTG FS DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min.(1) | Typ. | Max.(1) | Unit |
|---|---|---|---|---|---|---|---|
| Input levels | $V_{DD}$ | USB OTG FS operating voltage | | 3.0(2) | - | 3.6 | V |
| | $V_{DI}$(3) | Differential input sensitivity | I(USB_FS_DP/DM, USB_HS_DP/DM) | 0.2 | - | - | V |
| | $V_{CM}$(3) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{SE}$(3) | Single ended receiver threshold | | 1.3 | - | 2.0 | |
| Output levels | $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(4) | - | - | 0.3 | V |
| | $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(4) | 2.8 | - | 3.6 | |
| $R_{PD}$ | | PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM) | $V_{IN} = V_{DD}$ | 17 | 21 | 24 | kΩ |
| | | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | | 0.65 | 1.1 | 2.0 | |
| $R_{PU}$ | | PA12, PB15 (USB_FS_DP, USB_HS_DP) | $V_{IN} = V_{SS}$ | 1.5 | 1.8 | 2.1 | |
| | | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | $V_{IN} = V_{SS}$ | 0.25 | 0.37 | 0.55 | |

1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.
3. Guaranteed by design, not tested in production.
4. $R_L$ is the load connected on the USB OTG FS drivers

**Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | ns |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

**Figure 60. Asynchronous multiplexed PSRAM/NOR write waveforms**

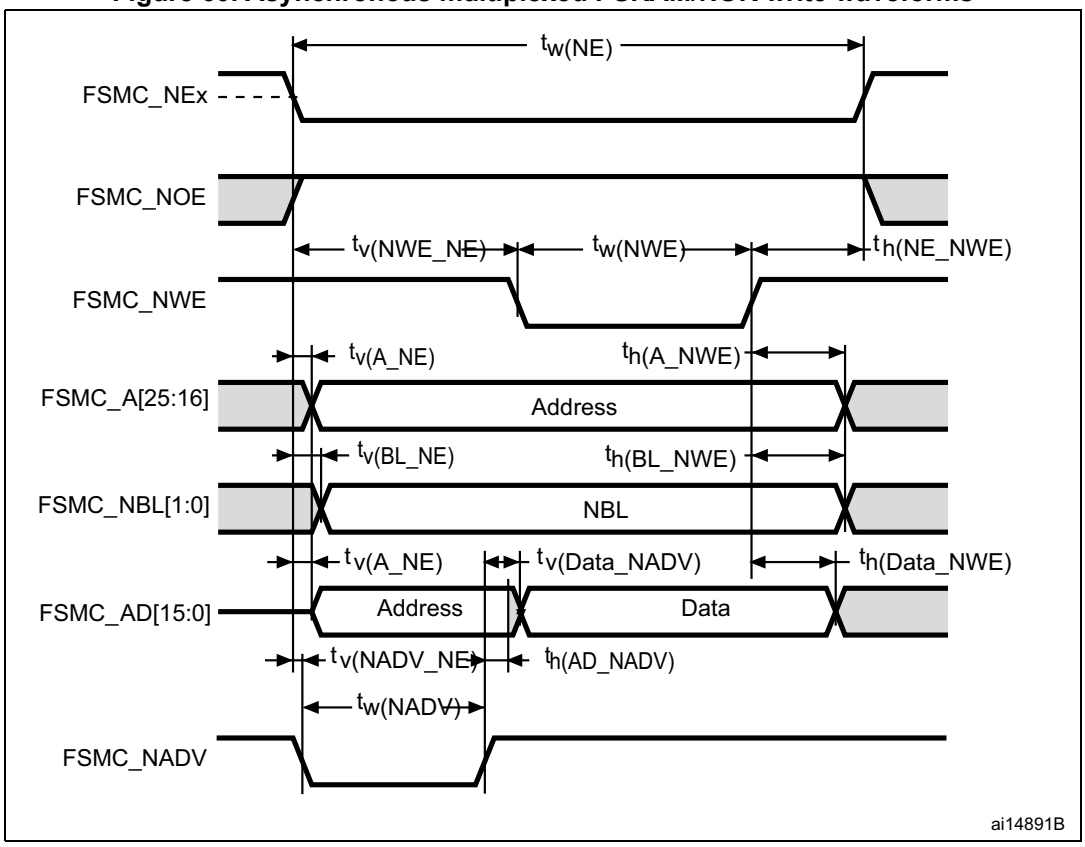



**Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $4T_{HCLK}$-1 | $4T_{HCLK}$+1 | ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK}$- 1 | $T_{HCLK}$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low tim e | $2T_{HCLK}$ | $2T_{HCLK}$+1 | ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK}$- 1 | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | 1 | 2 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK}$– 2 | $T_{HCLK}$+ 2 | ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD(adress) valid hold time after FSMC_NADV high) | $T_{HCLK}$ | - | ns |

**Table 76. Synchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{su(ADV-CLKH)}$ | FSMC_A/D[15:0] valid data before FSMC_CLK high | 5 | - | ns |
| $t_{h(CLKH-ADV)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | 0 | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

**Figure 62. Synchronous multiplexed PSRAM write timings**

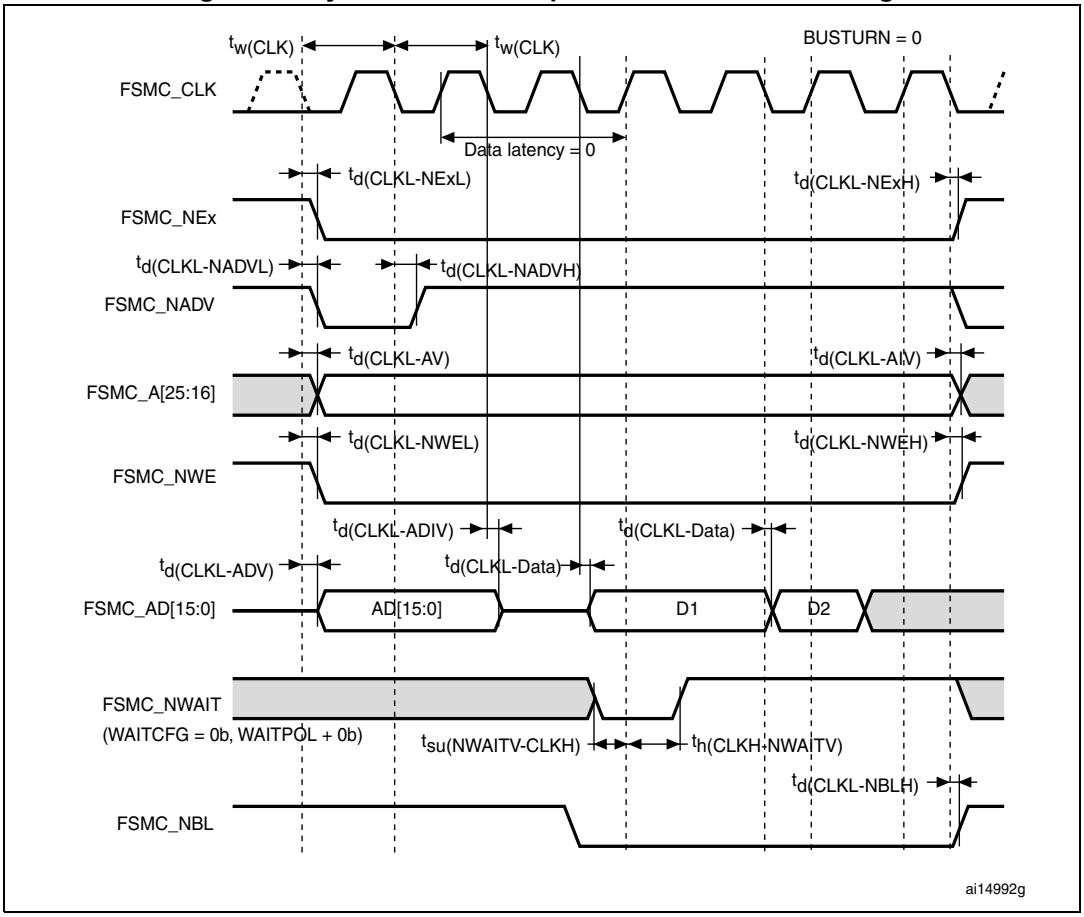



**Table 77. Synchronous multiplexed PSRAM write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | $2T_{HCLK}$- 1 | - | ns |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 0 | ns |
| $t_{d(CLKL-NExH)}$ | FSMC_CLK low to FSMC_NEx high (x= 0…2) | 2 | - | ns |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 2 | ns |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 3 | - | ns |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x=16…25) | - | 0 | ns |
| $t_{d(CLKL-AIV)}$ | FSMC_CLK low to FSMC_Ax invalid (x=16…25) | 7 | - | ns |

**Figure 70. PC Card/CompactFlash controller waveforms for I/O space write access**

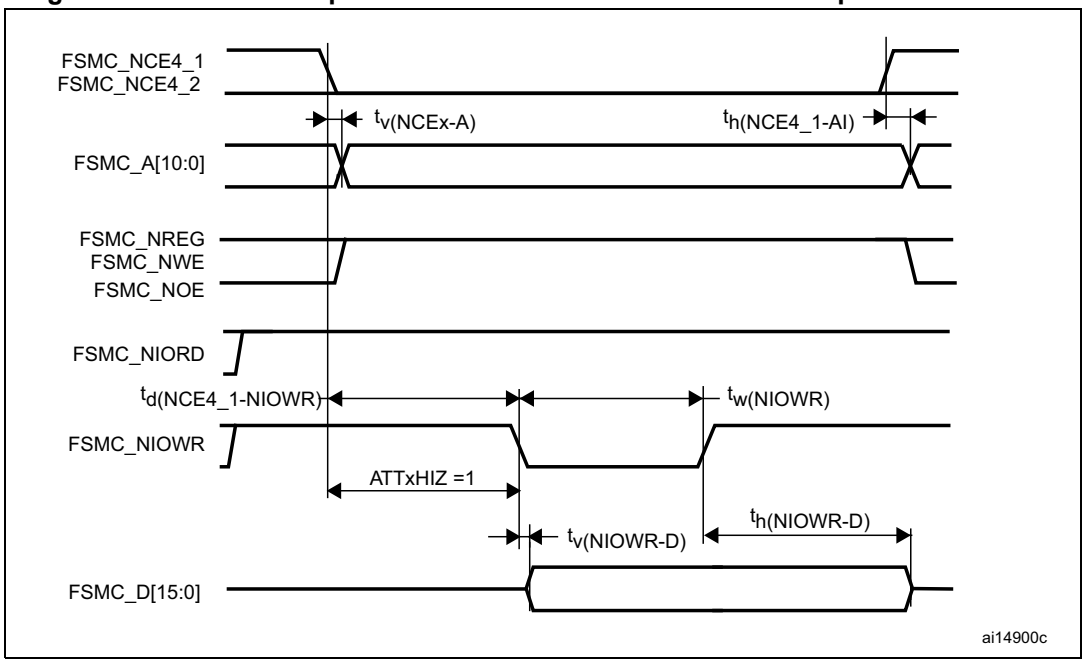



**Table 80. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{v(NCEx-A)}$ | FSMC_Ncex low to FSMC_Ay valid | - | 0 | ns |
| $t_{h(NCEx\_AI)}$ | FSMC_NCEx high to FSMC_Ax invalid | 4 | - | ns |
| $t_{d(NREG-NCEx)}$ | FSMC_NCEx low to FSMC_NREG valid | - | 3.5 | ns |
| $t_{h(NCEx-NREG)}$ | FSMC_NCEx high to FSMC_NREG invalid | $T_{HCLK}$+ 4 | - | ns |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | $5T_{HCLK}$+ 1 | ns |
| $t_{d(NCEx-NOE)}$ | FSMC_NCEx low to FSMC_NOE low | - | $5T_{HCLK}$ | ns |
| $t_{w(NOE)}$ | FSMC_NOE low width | $8T_{HCLK}$– 0.5 | $8T_{HCLK}$+ 1 | ns |
| $t_{d(NOE\_NCEx)}$ | FSMC_NOE high to FSMC_NCEx high | $5T_{HCLK}$+ 2.5 | - | ns |
| $t_{su\ (D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 4 | - | ns |
| $t_{h\ (N0E-D)}$ | FSMC_N0E high to FSMC_D[15:0] invalid | 2 | - | ns |
| $t_{w(NWE)}$ | FSMC_NWE low width | $8T_{HCLK}$- 1 | $8T_{HCLK}$+ 4 | ns |
| $t_{d(NWE\_NCEx)}$ | FSMC_NWE high to FSMC_NCEx high | $5T_{HCLK}$+ 1.5 | - | ns |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | 5HCLK+ 1 | ns |
| $t_{v\ (NWE-D)}$ | FSMC_NWE low to FSMC_D[15:0] valid | - | 0 | ns |
| $t_{h\ (NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | $8T_{HCLK}$ | - | ns |
| $t_{d\ (D-NWE)}$ | FSMC_D[15:0] valid before FSMC_NWE high | $13T_{HCLK}$ | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

**Table 81. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NIOWR)}$ | FSMC_NIOWR low width | $8T_{HCLK}$ - 0.5 | - | ns |
| $t_{v(NIOWR-D)}$ | FSMC_NIOWR low to FSMC_D[15:0] valid | - | $5T_{HCLK}$- 1 | ns |
| $t_{h(NIOWR-D)}$ | FSMC_NIOWR high to FSMC_D[15:0] invalid | $8T_{HCLK}$- 3 | - | ns |
| $t_{d(NCE4\_1-NIOWR)}$ | FSMC_NCE4_1 low to FSMC_NIOWR valid | - | $5T_{HCLK}$+ 1.5 | ns |
| $t_{h(NCEx-NIOWR)}$ | FSMC_NCEx high to FSMC_NIOWR invalid | $5T_{HCLK}$ | - | ns |
| $t_{d(NIORD-NCEx)}$ | FSMC_NCEx low to FSMC_NIORD valid | - | $5T_{HCLK}$+ 1 | ns |
| $t_{h(NCEx-NIORD)}$ | FSMC_NCEx high to FSMC_NIORD) valid | $5T_{HCLK}$– 0.5 | - | ns |
| $t_{w(NIORD)}$ | FSMC_NIORD low width | $8T_{HCLK}$+ 1 | - | ns |
| $t_{su(D-NIORD)}$ | FSMC_D[15:0] valid before FSMC_NIORD high | 9.5 | - | ns |
| $t_{d(NIORD-D)}$ | FSMC_D[15:0] valid after FSMC_NIORD high | 0 | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

### NAND controller waveforms and timings

*Figure 71* through *Figure 74* represent synchronous waveforms, together with *Table 82* and *Table 83* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

**Table 97. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 22-Apr-2011 | 6 | Changed datasheet status to “Full Datasheet”.<br>Introduced concept of SRAM1 and SRAM2.<br>LQFP176 package now in production and offered only for 256 Kbyte and 1 Mbyte devices. Availability of WLCSP64+2 package limited to 512 Kbyte and 1 Mbyte devices.<br>Updated *Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package* and *Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package*.<br>Added camera interface for STM32F207Vx devices in *Table 2: STM32F205xx features and peripheral counts*.<br>Removed 16 MHz internal RC oscillator accuracy in *Section 3.12: Clocks and startup*.<br>Updated *Section 3.16: Voltage regulator*.<br>Modified $I^2S$ sampling frequency range in *Section 3.12: Clocks and startup*, *Section 3.24: Inter-integrated sound (I2S)*, and *Section 3.30: Audio PLL (PLLI2S)*.<br>Updated *Section 3.17: Real-time clock (RTC), backup SRAM and backup registers* and description of TIM2 and TIM5 in *Section 3.20.2: General-purpose timers (TIMx)*.<br>Modified maximum baud rate (oversampling by 16) for USART1 in *Table 6: USART feature comparison*.<br>Updated note related to RFU pin below *Figure 12: STM32F20x LQFP100 pinout*, *Figure 13: STM32F20x LQFP144 pinout*, *Figure 14: STM32F20x LQFP176 pinout*, *Figure 15: STM32F20x UFBGA176 ballout*, and *Table 8: STM32F20x pin and ball definitions*.<br>In *Table 8: STM32F20x pin and ball definitions*,:changed I2S2_CK and I2S3_CK to I2S2_SCK and I2S3_SCK, respectively; added PA15 and TT (3.6 V tolerant I/O).<br>Added RTC_50Hz as PB15 alternate function in *Table 8: STM32F20x pin and ball definitions* and *Table 10: Alternate function mapping*.<br>Removed ETH _RMII_TX_CLK for PC3/AF11 in *Table 10: Alternate function mapping*.<br>Updated *Table 11: Voltage characteristics* and *Table 12: Current characteristics*.<br>$T_{STG}$ updated to –65 to +150 in *Table 13: Thermal characteristics*.<br>Added CEXT, ESL, and ESR in *Table 14: General operating conditions* as well as *Section 6.3.2: VCAP1/VCAP2 external capacitor*.<br>Modified *Note 4* in *Table 15: Limitations depending on the operating power supply range*.<br>Updated *Table 17: Operating conditions at power-up / power-down (regulator ON)*, and *Table 18: Operating conditions at power-up / power-down (regulator OFF)*.<br>Added OSC_OUT pin in *Figure 17: Pin loading conditions*. and *Figure 18: Pin input voltage*.<br>Updated *Figure 19: Power supply scheme* to add IRROFF and REGOFF pins and modified notes.<br>Updated $V_{PVD}$, $V_{BOR1}$, $V_{BOR2}$, $V_{BOR3}$, $T_{RSTTEMPO}$ typical value, and $I_{RUSH}$, added $E_{RUSH}$ and *Note 2* in *Table 19: Embedded reset and power control block characteristics*. |

**Table 97. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 14-Jun-2011 | 7 | Added SDIO in *Table 2: STM32F205xx features and peripheral counts*.<br>Updated $V_{IN}$ for 5V tolerant pins in *Table 11: Voltage characteristics*.<br>Updated jitter parameters description in *Table 34: Main PLL characteristics*.<br>Remove jitter values for system clock in *Table 35: PLLI2S (audio PLL) characteristics*.<br>Updated *Table 42: EMI characteristics*.<br>Update *Note 2* in *Table 52: I2C characteristics*.<br>Updated Avg_Slope typical value and $T_{S\_temp}$ minimum value in *Table 69: Temperature sensor characteristics*.<br>Updated $T_{S\_vbat}$ minimum value in *Table 70: VBAT monitoring characteristics*.<br>Updated $T_{S\_vrefint}$ minimum value in *Table 71: Embedded internal reference voltage*.<br>Added Software option in *Section 8: Part numbering*.<br>In *Table 101: Main applications versus package for STM32F2xxx microcontrollers*, renamed USB1 and USB2, USB OTG FS and USB OTG HS, respectively; and removed USB OTG FS and camera interface for 64-pin package; added USB OTG HS on 64-pin package; added *Note 1* and *Note 2*. |
| 20-Dec-2011 | 8 | Updated SDIO register addresses in *Figure 16: Memory map*.<br>Updated *Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package*, *Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package*, *Figure 1: Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package*, and added *Figure 4: Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package*.<br>Updated *Section 3.3: Memory protection unit*.<br>Updated *Section 3.6: Embedded SRAM*.<br>Updated *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)* to remove external FS OTG PHY support.<br>In *Table 8: STM32F20x pin and ball definitions*: changed SPI2_MCK and SPI3_MCK to I2S2_MCK and I2S3_MCK, respectively. Added ETH _RMII_TX_EN atlternate function to PG11. Added EVENTOUT in the list of alternate functions for I/O pin/balls. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions.<br>In *Table 10: Alternate function mapping*: changed I2S3_SCK to I2S3_MCK for PC7/AF6, added FSMC_NCE3 for PG9, FSMC_NE3 for PG10, and FSMC_NCE2 for PD7. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. Changed I2S3_SCK into I2S3_MCK for PC7/AF6. Updated peripherals corresponding to AF12.<br>Removed CEXT and ESR from *Table 14: General operating conditions*. |

**Table 97. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 29-Oct-2012 | 10 (continued) | Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in *Table 76: Synchronous multiplexed NOR/PSRAM read timings*, *Table 78: Synchronous non-multiplexed NOR/PSRAM read timings*, *Figure 61: Synchronous multiplexed NOR/PSRAM read timings* and *Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings*.<br>Added *Figure 87: LQFP176 recommended footprint*.<br>Added *Note 2* below *Figure 86: Regulator OFF/internal reset ON*.<br>Updated device subfamily in *Table 96: Ordering information scheme*.<br>Remove reference to note 2 for USB IOTG FS in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. |