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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

De	calls	5

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vgt6w

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in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to Figure 19: Power supply scheme for more details.

3.15 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry.

At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit. On devices in WLCSP64+2 package, the BOR, POR and PDR features can be disabled by setting IRROFF pin to V_{DD} . In this mode an external power supply supervisor is required (see Section 3.16).

The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.16 Voltage regulator

The regulator has five operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low-power regulator (LPR)
 - Power-down
- Regulator OFF
 - Regulator OFF/internal reset ON
 - Regulator OFF/internal reset OFF

3.16.1 Regulator ON

The regulator ON modes are activated by default on LQFP packages. On WLCSP64+2 package, they are activated by connecting both REGOFF and IRROFF pins to V_{SS}, while only REGOFF must be connected to V_{SS} on UFBGA176 package (IRROFF is not available).

 V_{DD} minimum value is 1.8 V.



If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see *Table 5* for differences).

TIM2, TIM3, TIM4, TIM5

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.



3.34 ADCs (analog-to-digital converters)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers TIM1, TIM2, TIM3, TIM4, TIM5 and TIM8 can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.35 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.



Table 8. STM32	F20>	c pin	and	ball definitions	

		Pi	ns								
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	1	1	1	A2	PE2	I/O	FT	-	TRACECLK, FSMC_A23, ETH_MII_TXD3, EVENTOUT	-
-	-	2	2	2	A1	PE3	I/O	FT	-	TRACED0,FSMC_A19, EVENTOUT	-
-	-	3	3	3	B1	PE4	I/O	FT	-	TRACED1,FSMC_A20, DCMI_D4, EVENTOUT	-
-	-	4	4	4	B2	PE5	I/O	FT	-	TRACED2, FSMC_A21, TIM9_CH1, DCMI_D6, EVENTOUT	-
-	-	5	5	5	В3	PE6	I/O	FT	-	TRACED3, FSMC_A22, TIM9_CH2, DCMI_D7, EVENTOUT	-
1	A9	6	6	6	C1	V _{BAT}	S		-	-	-
-	-	-	-	7	D2	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_AF2
2	B8	7	7	8	D1	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1
3	В9	8	8	9	E1	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN ⁽⁴⁾
4	C9	9	9	10	F1	PC15-OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT ⁽⁴⁾
-	-	-	-	11	D3	PI9	I/O	FT	-	CAN1_RX,EVENTOUT	-
-	-	-	-	12	E3	PI10	I/O	FT	-	ETH_MII_RX_ER, EVENTOUT	-
-	-	-	-	13	E4	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	-	-	14	F2	V _{SS}	S		-	-	-
-	-	-	-	15	F3	V _{DD}	S		-	-	-
-	-	-	10	16	E2	PF0	I/O	FT	-	FSMC_A0, I2C2_SDA, EVENTOUT	-
-	-	-	11	17	НЗ	PF1	I/O	FT	-	FSMC_A1, I2C2_SCL, EVENTOUT	
-	-	-	12	18	H2	PF2	I/O	FT	-	FSMC_A2, I2C2_SMBA, EVENTOUT	-
-	-	-	13	19	J2	PF3	I/O	FT	(4)	FSMC_A3, EVENTOUT	ADC3_IN9



		Pi	ins								
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-
-	-	-	-	85	M12	PH8	I/O	FT	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	86	M13	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	-
-	-	-	-	87	L13	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	88	L12	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	89	K12	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	90	H12	V _{SS}	S	-	-	-	-
-	-	-	-	91	J12	V _{DD}	S	-	-	-	-
33	J1	51	73	92	P12	PB12	I/O	FT	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-
34	H2	52	74	93	P13	PB13	I/O	FT	-	SPI2_SCK, I2S2_SCK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_ VBUS
35	H1	53	75	94	R14	PB14	I/O	FT	-	SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM USART3_RTS, TIM8_CH2N, EVENTOUT	-
36	G1	54	76	95	R15	PB15	I/O	FT	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, RTC_50Hz, EVENTOUT	-
-	-	55	77	96	P15	PD8	I/O	FT	-	FSMC_D13, USART3_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 26*. The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled unless otherwise mentioned
 - The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with one peripheral clocked on (with only the clock applied)
- The code is running from Flash memory and the Flash memory access time is equal to 3 wait states at 120 MHz
- Prefetch and Cache ON
- When the peripherals are enabled, HCLK = 120MHz, f_{PCLK1} = $f_{HCLK}/4,$ and f_{PCLK2} = $f_{HCLK}/2$
- The typical values are obtained for V_{DD} = 3.3 V and T_A= 25 °C, unless otherwise specified.

Per	ipheral ⁽¹⁾	Typical consumption at 25 °C	Unit
	GPIO A	0.45	
	GPIO B	0.43	
	GPIO C	0.46	
	GPIO D	0.44	
	GPIO E	0.44	
	GPIO F	0.42	
	GPIO G	0.44	
	GPIO H	0.42	
AHB1	GPIO I	0.43	
	OTG_HS + ULPI	3.64	
	CRC	1.17	mA
	BKPSRAM	0.21	
	DMA1	2.76	
	DMA2	2.85	
	ETH_MAC + ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	2.99	
AHB2	OTG_FS	3.16	
	DCMI	0.60	
AHB3	FSMC	1.74	

Table 26. Peripheral current consumption



6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 42: EMI characteristics*). It is available only on the main PLL.

Symbol	Parameter	Min	Тур	Max ⁽¹⁾	Unit
f _{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	2 ¹⁵ –1	-

Table 36	SSCG	naramotors	constraint
Table 30.	3366	parameters	constraint

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

```
MODEPER = round[f_{PLL \ IN}/ \ (4 \times f_{Mod})]
```

 $f_{\text{PLL}\ \text{IN}}$ and f_{Mod} must be expressed in Hz.

As an example:

If $f_{PLL_IN} = 1$ MHz and $f_{MOD} = 1$ kHz, the modulation depth (MODEPER) is given by equation 1:

MODEPER = round
$$[10^{6}/(4 \times 10^{3})] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

INCSTEP = round[
$$((2^{15} - 1) \times md \times PLLN)/(100 \times 5 \times MODEPER)$$
]

f_{VCO OUT} must be expressed in MHz.

With a modulation depth (md) = ± 2 % (4 % peak to peak), and PLLN = 240 (in MHz):

INCSTEP = round[$((2^{15}-1) \times 2 \times 240)/(100 \times 5 \times 250)$] = 126md(quantitazed)%

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}$$
% = (MODEPER × INCSTEP × 100 × 5)/ ((2¹⁵ - 1) × PLLN)

As a result:

$$md_{quantized} \% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%$$
(peak)



Symbol	Paran	neter	Conditions	Min	Тур	Мах	Unit
R _{PU}	Weak pull-up equivalent	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	
	resistor	PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	kO
R _{PD}	Weak pull-down equivalent resister ⁽⁷⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	K22
	TESISION	PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
C _{IO} ⁽⁸⁾	I/O pin capacitan	ice	-	-	5	-	pF

Table 46. I/O static characteristics (continued)

1. Guaranteed by design, not tested in production.

2. Guaranteed by tests in production.

3. With a minimum of 200 mV.

- 4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to Table 45: I/O current injection susceptibility
- To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to Table 45: I/O current injection susceptibility
- 6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
- 7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
- 8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.







6.3.17 **NRST** pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 49).

Unless otherwise specified, the parameters given in Table 49 are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 14.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	kΩ
V _{F(NRST)} ⁽²⁾	NRST Input filtered pulse	-	-	-	100	ns
V _{NF(NRST)} ⁽²⁾	NRST Input not filtered pulse	V _{DD} > 2.7 V	300	-	-	ns
T _{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	_	μs

Table 49. NRST pin characteristics

The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series 1. resistance must be minimum (~10% order).

2. Guaranteed by design, not tested in production.



Figure 40. Recommended NRST pin protection

- The reset network protects the device against parasitic resets. 1.
- The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in 2. Table 49. Otherwise the reset is not taken into account by the device.





Figure 48. ULPI timing diagram

Table 61. ULPI timing

Symbol	Parameter	Valu	Unit	
Symbol	Falanielei	Min.	Max.	onic
t _{sc}	Control in (ULPI_DIR) setup time	-	2.0	
	Control in (ULPI_NXT) setup time	-	1.5	
t _{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0	-	
t _{SD}	Data in setup time	-	2.0	ns
t _{HD}	Data in hold time	0	-	
t _{DC}	Control out (ULPI_STP) setup time and hold time	-	9.2	
t _{DD}	Data out available from clock rising edge	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = -40 to 85 °C.

Ethernet characteristics

Table 62 shows the Ethernet operating voltage.

Table 62. Ethernet DC electrical characteristics

Symbol		Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 63 gives the list of Ethernet MAC signals for the SMI (station management interface) and Figure 49 shows the corresponding timing diagram.



Table 65 gives the list of Ethernet MAC signals for MII and *Figure 50* shows the corresponding timing diagram.





Table 65.	Dvnamics	characteristics:	Ethernet	MAC s	ianals	for MI	
	Dynamics	onuluotonistios.		MAC 5	ignuis		

Symbol	Rating	Min	Тур	Мах	Unit
t _{su(RXD)}	Receive data setup time	7.5	-	-	ns
t _{ih(RXD)}	Receive data hold time	1	-	-	ns
t _{su(DV)}	Data valid setup time	4	-	-	ns
t _{ih(DV)}	Data valid hold time	0	-	-	ns
t _{su(ER)}	Error setup time	3.5	-	-	ns
t _{ih(ER)}	Error hold time	0	-	-	ns
t _{d(TXEN)}	Transmit enable valid delay time	-	11	14	ns
t _{d(TXD)}	Transmit data valid delay time	_	11	14	ns

CAN (controller area network) interface

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (CANTX and CANRX).



Symbol	Parameter	Min	Тур	Мах	Unit	Comments
Update rate ⁽²⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \le 50 \text{ pF},$ $R_{LOAD} \ge 5 \text{ k}\Omega$
t _{wakeup} (4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	$C_{LOAD} \le 50$ pF, $R_{LOAD} \ge 5$ k Ω input code between lowest and highest possible ones.
PSRR+ ⁽²⁾	Power supply rejection ratio (to V _{DDA}) (static DC measurement)	-	-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF

 Table 68. DAC characteristics (continued)

 On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see <u>Section 3.16</u>).

2. Guaranteed by design, not tested in production.

3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.

4. Guaranteed by characterization results, not tested in production.





1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly, without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.22 Temperature sensor characteristics

Symbol	Parameter	Min	Тур	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	±1	<u>+2</u>	°C
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/°C
V ₂₅ ⁽¹⁾	Voltage at 25 °C	-	0.76	-	V
t _{START} ⁽²⁾	Startup time	-	6	10	μs
T _{S_temp} ⁽²⁾	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	μs

1. Guaranteed by characterization results, not tested in production.

2. Guaranteed by design, not tested in production.



6.3.23 V_{BAT} monitoring characteristics

Table 70. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Тур	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V _{BAT} measurement	-	2	-	
Er ⁽¹⁾	Error on Q	–1	-	+1	%
T _{S_vbat} ⁽²⁾⁽²⁾	ADC sampling time when reading the V _{BAT} (1 mV accuracy)	5	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Embedded reference voltage

The parameters given in *Table 71* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{REFINT}	Internal reference voltage	–40 °C < T _A < +105 °C	1.18	1.21	1.24	V
T _{S_vrefint} ⁽¹⁾	ADC sampling time when reading the internal reference voltage	-	10	-	-	μs
V _{RERINT_s}	Internal reference voltage spread over the temperature range	V _{DD} = 3 V	-	3	5	mV
T _{Coeff} ⁽²⁾	Temperature coefficient	-	-	30	50	ppm/°C
t _{START} ⁽²⁾	Startup time	-	_	6	10	μs

Table 71. Embedded internal reference voltage

1. Shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design, not tested in production.

6.3.25 FSMC characteristics

Asynchronous waveforms and timings

Figure 57 through *Figure 60* represent asynchronous waveforms and *Table 72* through *Table 75* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 1
- DataSetupTime = 1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.



		(*******		
Symbol	Parameter	Min	Мах	Unit
t _{su(ADV-CLKH)}	FSMC_A/D[15:0] valid data before FSMC_CLK high	5	-	ns
t _{h(CLKH-ADV)}	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns

Table 76. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.



Figure 62. Synchronous multiplexed PSRAM write timings

Table 77. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Мах	Unit
t _{w(CLK)}	FSMC_CLK period	2T _{HCLK} - 1	-	ns
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x=02)	-	0	ns
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x= 02)	2	-	ns
t _{d(CLKL-NADVL)}	FSMC_CLK low to FSMC_NADV low	-	2	ns
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	3	-	ns
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x=1625)	-	0	ns
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x=1625)	7	-	ns





Figure 71. NAND controller waveforms for read access

Figure 72. NAND controller waveforms for write access







Symbol	Parameter	Conditions	Min	Max	Unit		
f _{PP}	Clock frequency in data transfer mode	$C_L \le 30 \text{ pF}$	0	48	MHz		
-	SDIO_CK/f _{PCLK2} frequency ratio	-	-	8/3	-		
t _{W(CKL)}	Clock low time, f _{PP} = 16 MHz	$C_L \le 30 \text{ pF}$	32	-			
t _{W(CKH)}	Clock high time, f _{PP} = 16 MHz	$C_L \le 30 \text{ pF}$	31	-			
t _r	Clock rise time	$C_L \le 30 \text{ pF}$	-	3.5	ns		
t _f	Clock fall time	$C_L \le 30 \text{ pF}$	-	5			
CMD, D inputs (referenced to CK)							
t _{ISU}	Input setup time	$C_L \le 30 \text{ pF}$	2	-	200		
t _{IH}	Input hold time	$C_L \le 30 \text{ pF}$	0	-	115		
CMD, D out	puts (referenced to CK) in MMC and	SD HS mode					
t _{OV}	Output valid time	$C_L \le 30 \text{ pF}$	-	6	20		
t _{OH}	Output hold time	$C_L \le 30 \text{ pF}$	0.3	-	115		
CMD, D outputs (referenced to CK) in SD default mode ⁽¹⁾							
t _{OVD}	Output valid default time	$C_L \le 30 \text{ pF}$	-	7	20		
t _{OHD}	Output hold default time	$C_L \le 30 \text{ pF}$	0.5	-	115		

Table 85. SD/MMC characteristics

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

6.3.28 RTC characteristics

Table 86. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f _{PCLK1} /RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-



Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
F	-	0.220	-	-	0.0087	-
G	-	0.386	-	-	0.0152	-
ааа	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ССС	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 80. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



Table 89. WLCSP64 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm



Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch,ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Тур.	Max.	Min.	Тур.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

Table 94. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm



Date	Revision	Changes		
Date 22-Apr-2011	Revision 6 (continued)	Changes Changed t _w (SCKH) to t _w (SCLL), t _w (SCKL) to t _w (SCL), tr(SCL), and t _f (SCK) to t _f (SCL) in Table 52: I2C characteristics and in Figure 41: I2C bus AC waveforms and measurement circuit. Added Table 57: USB OTG FS DC electrical characteristics and updated Table 58: USB OTG FS electrical characteristics. Updated V _{DD} minimum value in Table 62: Ethernet DC electrical characteristics. Updated Table 66: ADC characteristics and R _{AIN} equation. Updated Table 66: ADC characteristics and R _{AIN} equation. Updated Table 66: ADC characteristics and R _{AIN} equation. Updated Table 66: ADC characteristics and R _{AIN} equation. Updated Table 66: ADC characteristics and R _{AIN} equation. Updated Table 71: Embedded internal reference voltage. Modified FSMC_NOE waveform in Figure 57: Asynchronous non- multiplexed SRAM/PSRAM/NOR read waveforms. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLKL period, changed t _d (CLKH-NEXH) to t _d (CLKL-NEXH), t _d (CLKH-AIV) to t _d (CLKL-NWEH), and updated data latency from 1 to 0 in Figure 61: Synchronous non- multiplexed NOR/PSRAM read timings, Figure 62: Synchronous non- multiplexed NOR/PSRAM read timings, Figure 62: Synchronous non- multiplexed NOR/PSRAM read timings, and Figure 64: Synchronous non- multiplexed NOR/PSRAM read timings, Table 76, Table 77, Table 78, and Table 79. Updated not 2 in Table 72, Table 73, Table 74, Table 75, Table 76, Table 77, Table 78, and Table 79. Modified t _N (NOWR-D) in Figure 70: PC Card/CompactFlash controller waveforms for vrite access, Figure 73: NAND controller waveforms for common memory read access, Rigure 74: NAND controller waveforms for common memory vrite access Specified Full speed (FS) mode for Figure 89: USB OTG HS host-only		

Table 97. Document revision history (continued)

