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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205vgt7

2 Description

The STM32F20x family is based on the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of up to 120 MHz. The family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 128 Kbytes of system SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator™) which allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz. This performance has been validated using the CoreMark benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true number random generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), and a camera interface for CMOS sensors. The devices also feature standard peripherals.

- Up to three I^2Cs
- Three SPIs, two I^2Ss. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external PLL to allow synchronization.
- 4 USARTs and 2 UARTs
- A USB OTG high-speed with full-speed capability (with the ULPI)
- A second USB OTG (full-speed)
- Two CANs
- An SDIO interface
- Ethernet and camera interface available on STM32F207xx devices only.

Note: The STM32F205xx and STM32F207xx devices operate in the –40 to +105 °C temperature range from a 1.8 V to 3.6 V power supply. On devices in WLCSP64+2 package, if IRROFF is set to $V_{DD,}$ the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see Section 3.16).

A comprehensive set of power-saving modes allow the design of low-power applications.

STM32F205xx and STM32F207xx devices are offered in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.These features make the STM32F205xx and STM32F207xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS}. On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.26 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F207xx devices.

The STM32F207xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F207xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F207xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F207xx.

The STM32F207xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.27 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one

Table 8. STM32F20x pin and ball definitions

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	1	1	1	A2	PE2	I/O	FT	-	TRACECLK, FSMC_A23, ETH_MII_TXD3, EVENTOUT	-
-	-	2	2	2	A1	PE3	I/O	FT	-	TRACED0,FSMC_A19, EVENTOUT	-
-	-	3	3	3	B1	PE4	I/O	FT	-	TRACED1,FSMC_A20, DCMI_D4, EVENTOUT	-
-	-	4	4	4	B2	PE5	I/O	FT	-	TRACED2, FSMC_A21, TIM9_CH1, DCMI_D6, EVENTOUT	-
-	-	5	5	5	B3	PE6	I/O	FT	-	TRACED3, FSMC_A22, TIM9_CH2, DCMI_D7, EVENTOUT	-
1	A9	6	6	6	C1	V_{BAT}	S		-	-	-
-	-	-	-	7	D2	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_AF2
2	B8	7	7	8	D1	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1
3	B9	8	8	9	E1	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN[4]
4	C9	9	9	10	F1	PC15-OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT[4]
-	-	-	-	11	D3	PI9	I/O	FT	-	CAN1_RX,EVENTOUT	-
-	-	-	-	12	E3	PI10	I/O	FT	-	ETH_MII_RX_ER, EVENTOUT	-
-	-	-	-	13	E4	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	-	-	14	F2	V_{SS}	S		-	-	-
-	-	-	-	15	F3	V_{DD}	S		-	-	-
-	-	-	10	16	E2	PF0	I/O	FT	-	FSMC_A0, I2C2_SDA, EVENTOUT	-
-	-	-	11	17	H3	PF1	I/O	FT	-	FSMC_A1, I2C2_SCL, EVENTOUT	-
-	-	-	12	18	H2	PF2	I/O	FT	-	FSMC_A2, I2C2_SMBA, EVENTOUT	-
-	-	-	13	19	J2	PF3	I/O	FT	(4)	FSMC_A3, EVENTOUT	ADC3_IN9

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-
-	-	-	-	85	M12	PH8	I/O	FT	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	86	M13	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	-
-	-	-	-	87	L13	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	88	L12	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	89	K12	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	90	H12	V_{SS}	S	-	-	-	-
-	-	-	-	91	J12	V_{DD}	S	-	-	-	-
33	J1	51	73	92	P12	PB12	I/O	FT	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-
34	H2	52	74	93	P13	PB13	I/O	FT	-	SPI2_SCK, I2S2_SCK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_ VBUS
35	H1	53	75	94	R14	PB14	I/O	FT	-	SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM USART3_RTS, TIM8_CH2N, EVENTOUT	-
36	G1	54	76	95	R15	PB15	I/O	FT	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, RTC_50Hz, EVENTOUT	-
-	-	55	77	96	P15	PD8	I/O	FT	-	FSMC_D13, USART3_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	-	130	D13	PH15	I/O	FT	-	TIM8_CH3N, DCMI_D11, EVENTOUT	-
-	-	-	-	131	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS, I2S2_WS, DCMI_D13, EVENTOUT	-
-	-	-	-	132	D14	PI1	I/O	FT	-	SPI2_SCK, I2S2_SCK, DCMI_D8, EVENTOUT	-
-	-	-	-	133	C14	PI2	I/O	FT	-	TIM8_CH4 ,SPI2_MISO, DCMI_D9, EVENTOUT	-
-	-	-	-	134	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI, I2S2_SD, DCMI_D10, EVENTOUT	-
-	-	-	-	135	D9	V_{SS}	S	-	-	-	-
-	-	-	-	136	C9	V_{DD}	S	-	-	-	-
49	A1	76	109	137	A14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	A2	77	110	138	A13	PA15 (JTDI)	I/O	FT	-	JTDI, SPI3_NSS, I2S3_WS,TIM2_CH1_ETR, SPI1_NSS, EVENTOUT	-
51	B3	78	111	139	B14	PC10	I/O	FT	-	SPI3_SCK, I2S3_SCK, UART4_TX, SDIO_D2, DCMI_D8, USART3_TX, EVENTOUT	-
52	C3	79	112	140	B13	PC11	I/O	FT	-	UART4_RX, SPI3_MISO, SDIO_D3, DCMI_D4,USART3_RX, EVENTOUT	-
53	A3	80	113	141	A12	PC12	I/O	FT	-	UART5_TX, SDIO_CK, DCMI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT	-
-	-	81	114	142	B12	PD0	I/O	FT	-	FSMC_D2,CAN1_RX, EVENTOUT	-
-	-	82	115	143	C12	PD1	I/O	FT	-	FSMC_D3, CAN1_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	98	142	170	A3	PE1	I/O	FT	-	FSMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	D5	V_{SS}	S	-	-	-	-
63	D8	-	-	-	-	V_{SS}	S	-	-	-	-
-	-	99	143	171	C6	RFU	-	-	(7)	-	-
64	D9	100	144	172	C5	V_{DD}	S	-	-	-	-
-	-	-	-	173	D4	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5, EVENTOUT	-
-	-	-	-	174	C4	PI5	I/O	FT	-	TIM8_CH1, DCMI_VSYNC, EVENTOUT	-
-	-	-	-	175	C3	PI6	I/O	FT	-	TIM8_CH2, DCMI_D6, EVENTOUT	-
-	-	-	-	176	C2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	C8	-	-	-	-	IRROFF	I/O	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F20x and STM32F21x reference manual, available from the STMicroelectronics website: www.st.com.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA176 package and if the REGOFF pin is set to V_{DD} (Regulator OFF), then PA0 is used as an internal Reset (active low).
6. FSMC_NL pin is also named FSMC_NADV on memory devices.
7. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.

Table 9. FSMC pin definition

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	A23	A23	-	Yes
PE3	-	A19	A19	-	Yes
PE4	-	A20	A20	-	Yes

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled(3)	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz(4)	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock(2), all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz(4)	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

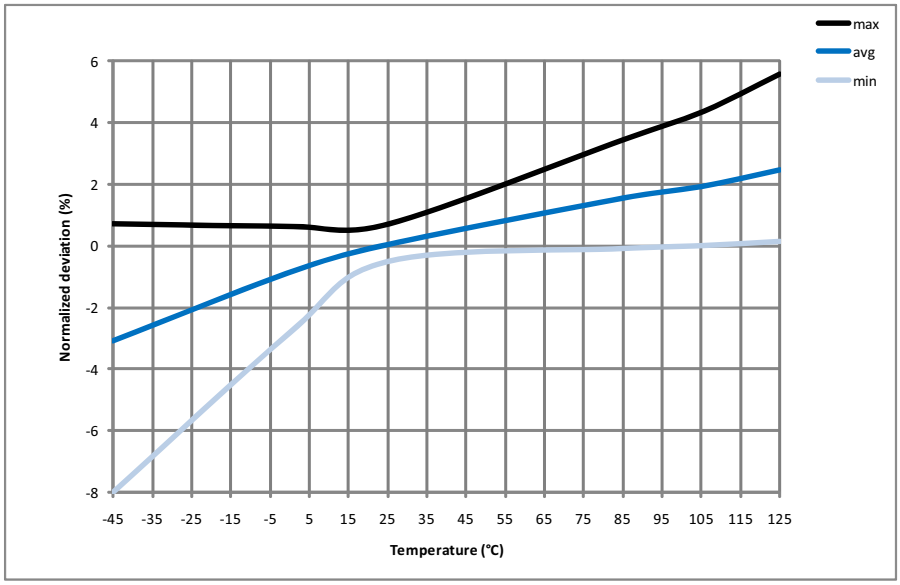
1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Table 22. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	120 MHz	38	51	61	mA
			90 MHz	30	43	53	
			60 MHz	20	33	43	
			30 MHz	11	25	35	
			25 MHz	8	21	31	
			16 MHz	6	19	29	
			8 MHz	3.6	17.0	27.0	
			4 MHz	2.4	15.4	25.3	
			2 MHz	1.9	14.9	24.7	
		External clock(2), all peripherals disabled	120 MHz	8	21	31	
			90 MHz	7	20	30	
			60 MHz	5	18	28	
			30 MHz	3.5	16.0	26.0	
			25 MHz	2.5	16.0	25.0	
			16 MHz	2.1	15.1	25.0	
			8 MHz	1.7	15.0	25.0	
			4 MHz	1.5	14.6	24.6	
			2 MHz	1.4	14.2	24.3	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Figure 34. ACC_{HSI} versus temperature



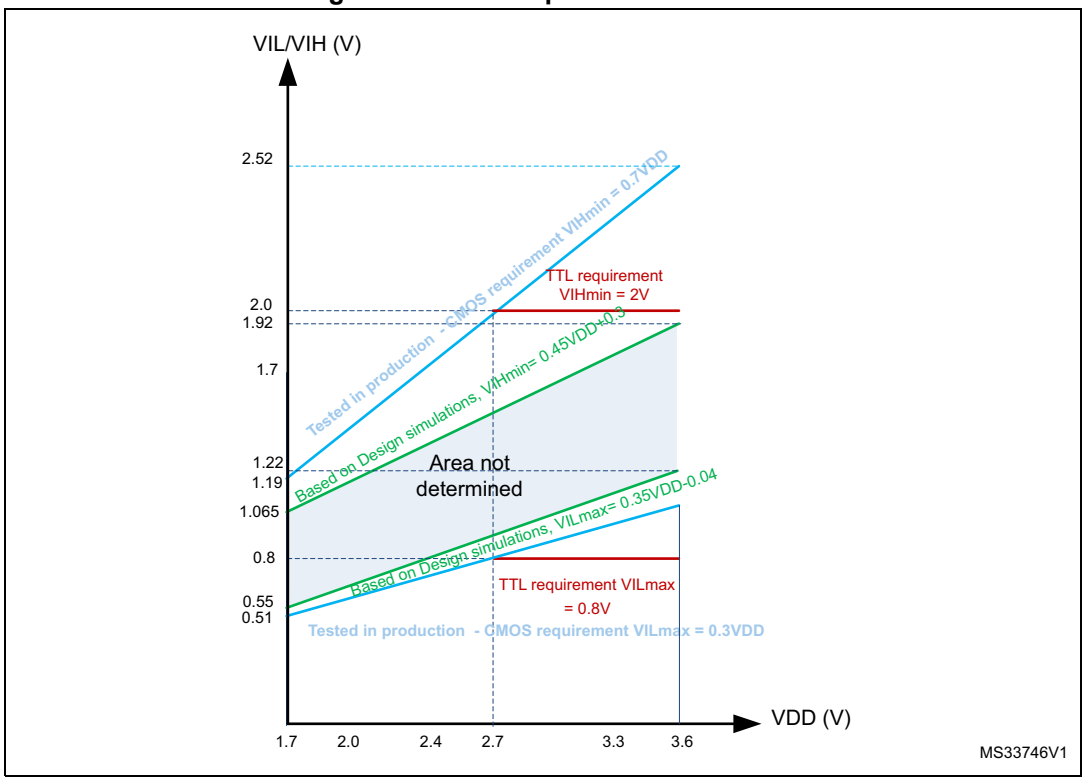
Low-speed internal (LSI) RC oscillator

Table 33. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

Figure 38. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 51. Characteristics of TIMx connected to the APB2 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB2 prescaler distinct from 1, $f_{TIMxCLK}$ = 120 MHz	1	-	$t_{TIMxCLK}$
			8.3	-	ns
		AHB/APB2 prescaler = 1, $f_{TIMxCLK}$ = 60 MHz	1	-	$t_{TIMxCLK}$
			16.7	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 120 MHz APB2 = 60 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	60	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0083	546	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	35.79	s

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.

6.3.19 Communications interfaces

I^2C interface characteristics

STM32F205xx and STM32F207xx I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 52*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 56. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 57. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

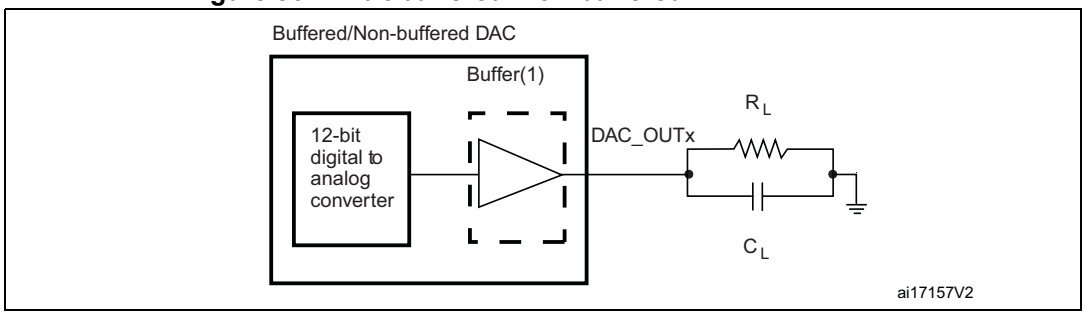
1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Table 68. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. Guaranteed by design, not tested in production.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results, not tested in production.

Figure 56. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly, without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.22 Temperature sensor characteristics

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.23 V_{BAT} monitoring characteristics

Table 70. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} (1 mV accuracy)	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Embedded reference voltage

The parameters given in *Table 71* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 71. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s} (2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

6.3.25 FSMC characteristics

Asynchronous waveforms and timings

Figure 57 through *Figure 60* represent asynchronous waveforms and *Table 72* through *Table 75* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 1
- DataSetupTime = 1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}– 0.5	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}- 1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK}+2	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}– 0.5	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 61 through *Figure 64* represent synchronous waveforms, and *Table 77* through *Table 79* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 73. NAND controller waveforms for common memory read access

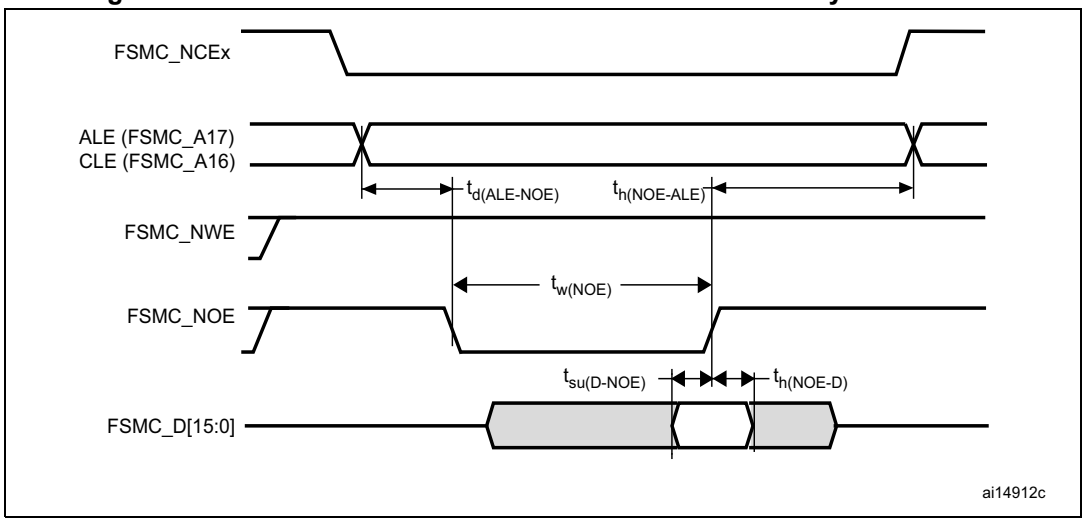


Figure 74. NAND controller waveforms for common memory write access

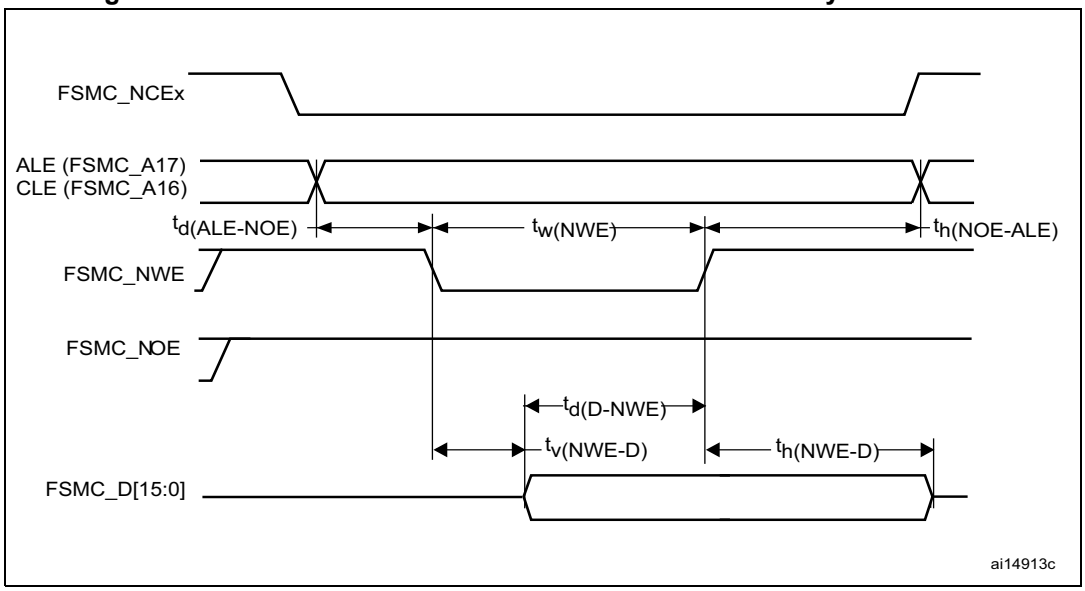


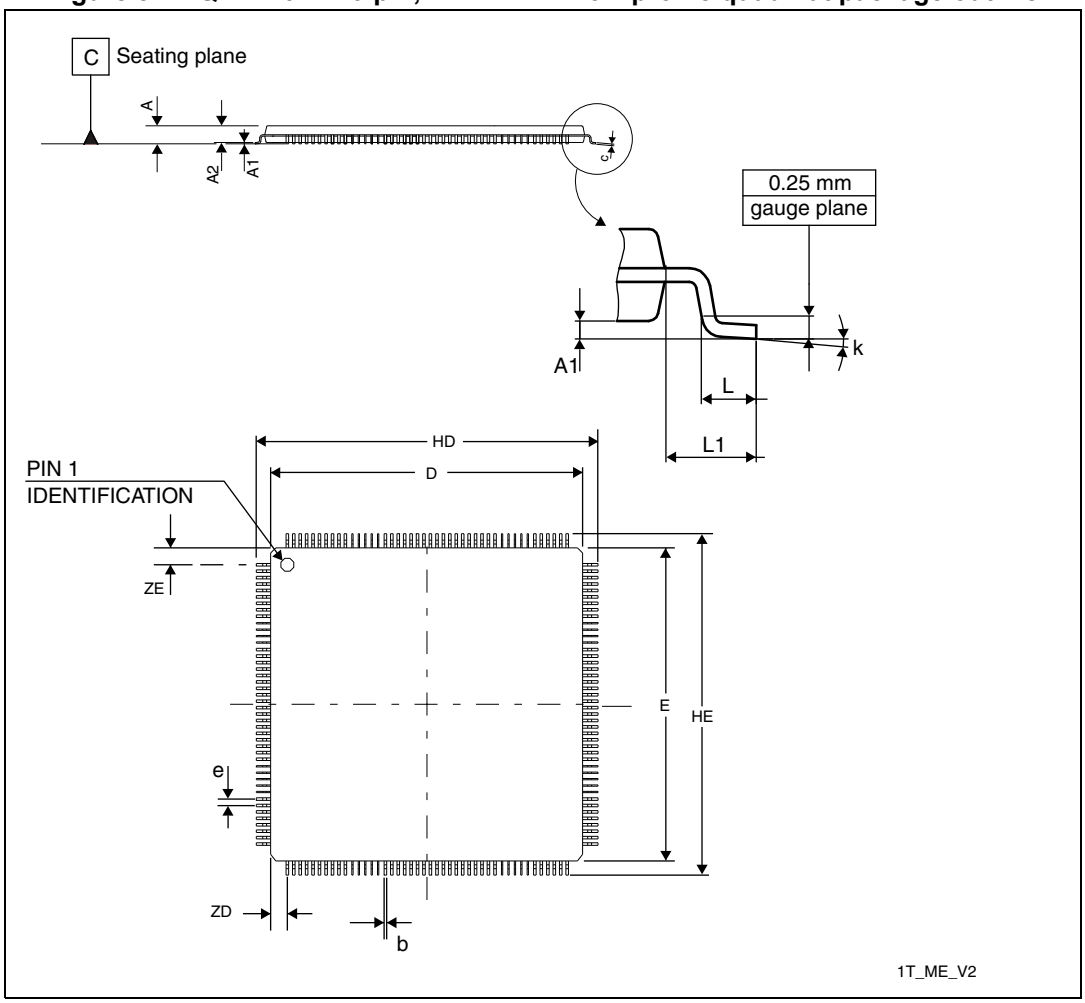
Table 82. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FSMC_NOE low width	$4T_{HCLK}$- 1	$4T_{HCLK}$+ 2	ns
$t_{su(D-NOE)}$	FSMC_D[15-0] valid data before FSMC_NOE high	9	-	ns
$t_{h(NOE-D)}$	FSMC_D[15-0] valid data after FSMC_NOE high	3	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$3T_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}$+ 2	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

7.5 LQFP176 package information

Figure 87. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 92. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

Symbol	Dimensions					
	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 97. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	10	Changed minimum supply voltage from 1.65 to 1.8 V. Updated number of AHB buses in *Section 2: Description* and *Section 3.12: Clocks and startup*. Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package. Updated *Note 2* below *Figure 4: STM32F20x block diagram*. Changed System memory to System memory + OTP in *Figure 16: Memory map*. Added *Note 1* below *Table 16: VCAP1/VCAP2 operating conditions*. Updated V_{DDA} and V_{REF+} decouping capacitor in *Figure 19: Power supply scheme* and updated *Note 3*. Changed simplex mode into half-duplex mode in *Section 3.24: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively.Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in *Table 10: Alternate function mapping*. Updated note applying to I_{DD} (external clock and all peripheral disabled) in *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*. Updated *Note 3* below *Table 22: Typical and maximum current consumption in Sleep mode*. Removed f_{HSE_ext} typical value in *Table 28: High-speed external user clock characteristics*. Updated master I2S clock jitter conditions and vlaues in *Table 35: PLLI2S (audio PLL) characteristics*. Updated equations in *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in *Table 47: Output voltage characteristics*. Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in *Table 49: NRST pin characteristics*. Updated *Table 54: SPI characteristics* and *Table 55: I2S characteristics*. Removed note 1 related to measurement points below *Figure 43: SPI timing diagram - slave mode and CPHA = 1*, *Figure 44: SPI timing diagram - master mode*, and *Figure 45: I2S slave timing diagram (Philips protocol)(1)*. Updated t_{HC} in *Table 61: ULPI timing*. Updated *Figure 49: Ethernet SMI timing diagram*, *Table 63: Dynamics characteristics: Ethernet MAC signals for SMI* and *Table 65: Dynamics characteristics: Ethernet MAC signals for MII*. Update f_{TRIG} in *Table 66: ADC characteristics*. Updated I_{DDA} description in *Table 68: DAC characteristics*. Updated note below *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*.

Table 97. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	11 (continued)	Removed Appendix A Application block diagrams. Updated *Figure 77: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 87: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 80: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 83: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*.
27-Oct-2014	12	Updated V_{BAT} voltage range in *Figure 19: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 14: General operating conditions*. Removed note 1 in *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Table 45: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 69: Temperature sensor characteristics*. Updated *Figure 79: WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline* and *Table 88: WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data*. Added *Figure 83: LQFP100 marking (package top view)* and *Figure 86: LQFP144 marking (package top view)*.
2-Feb-2016	13	Updated *Section 1: Introduction*. Updated *Table 32: HSI oscillator characteristics* and its footnotes. Updated *Figure 36: PLL output clock waveforms in center spread mode*, *Figure 37: PLL output clock waveforms in down spread mode*, *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.