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Applications of "Embedded - Microcontrollers"

| Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	100K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205zct7tr

Figure 5. Multi-AHB matrix
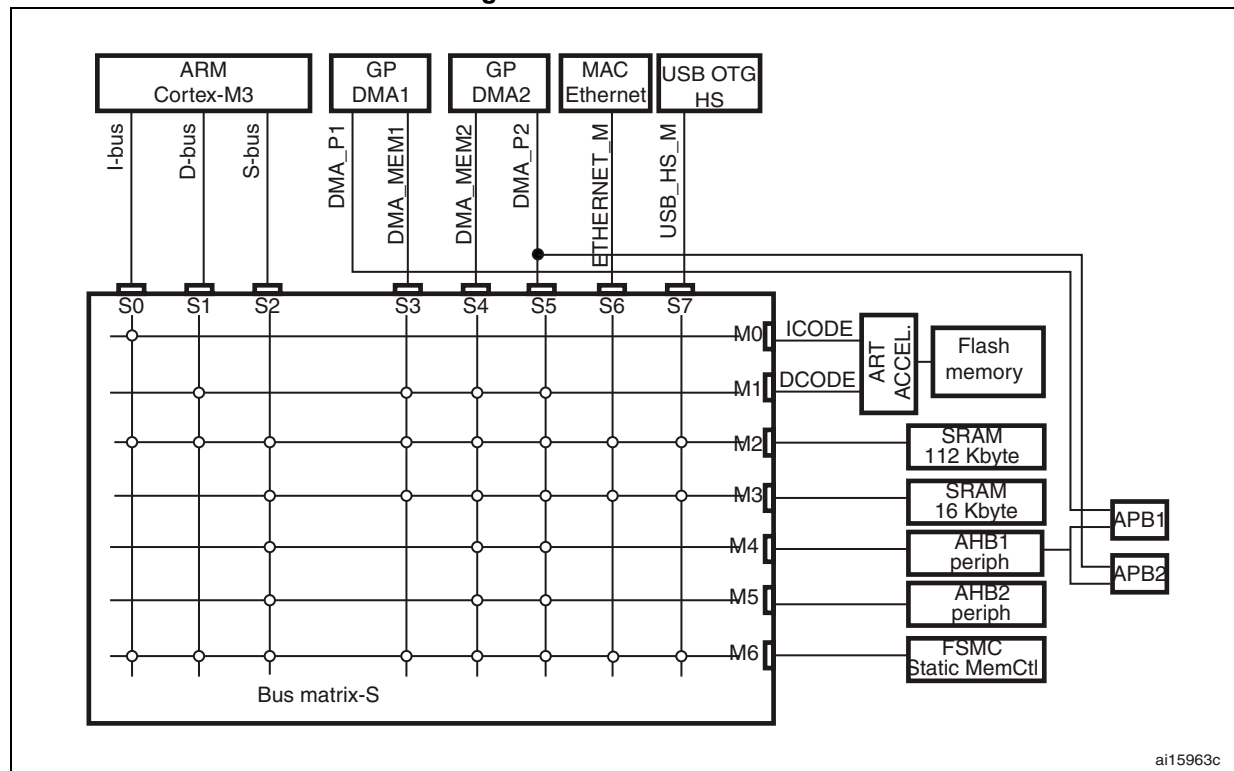
3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

Figure 6. Regulator OFF/internal reset ON
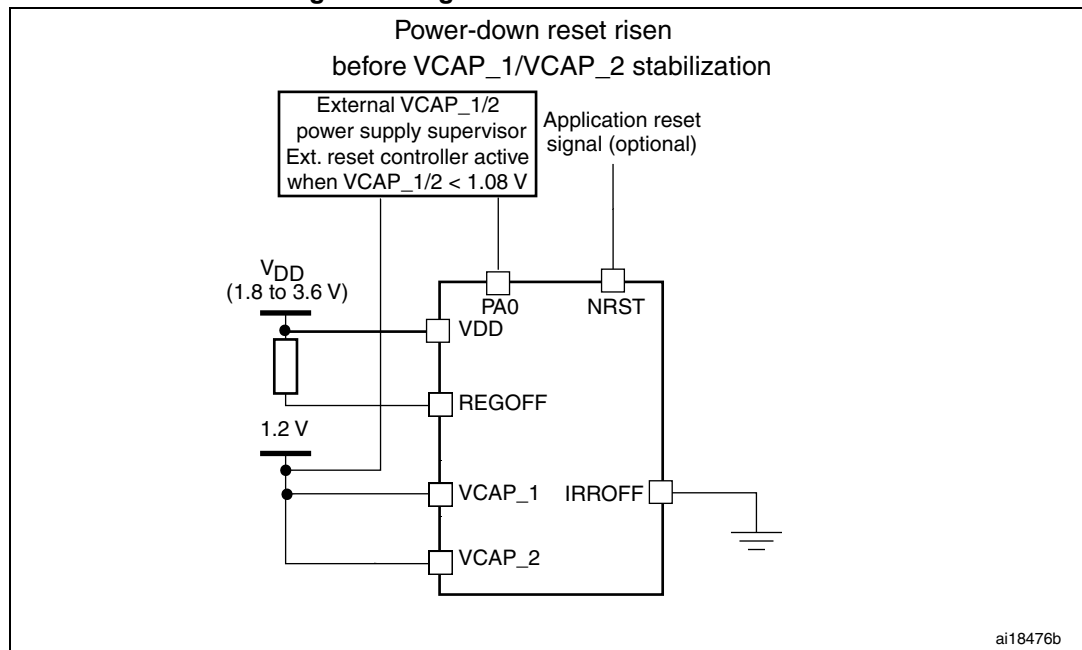
The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.

- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 8*).

- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).

- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD}. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON/internal reset ON	Regulator OFF/internal reset ON	Regulator OFF/internal reset OFF
LQFP64 LQFP100 LQFP144 LQFP176	Yes	No	No
WLCSP 64+2	Yes REGOFF and IRROFF set to V_{SS}	Yes REGOFF set to V_{DD} and IRROFF set to V_{SS}	Yes REGOFF set to V_{SS} and IRROFF set to V_{DD}
UFBGA176	Yes REGOFF set to V_{SS}	Yes REGOFF set to V_{DD}	No

3.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F20x devices includes:
- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Its main features are the following:
- Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.
- It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.
- Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.
- A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The 4-Kbyte backup SRAM is an EEPROM-like area.It can be used to store data which need to be retained in VBAT and standby mode.This memory area is disabled to minimize power consumption (see *Section 3.18: Low-power modes*). It can be enabled by software.

3.20 Timers and watchdogs

The STM32F20x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	30 MHz	60 MHz
General purpose	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	60 MHz	120 MHz
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	60 MHz	120 MHz
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	30 MHz	60 MHz
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	30 MHz	60 MHz

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see *Table 5* for differences).

TIM2, TIM3, TIM4, TIM5

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

Table 8. STM32F20x pin and ball definitions

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	1	1	1	A2	PE2	I/O	FT	-	TRACECLK, FSMC_A23, ETH_MII_TXD3, EVENTOUT	-
-	-	2	2	2	A1	PE3	I/O	FT	-	TRACED0,FSMC_A19, EVENTOUT	-
-	-	3	3	3	B1	PE4	I/O	FT	-	TRACED1,FSMC_A20, DCMI_D4, EVENTOUT	-
-	-	4	4	4	B2	PE5	I/O	FT	-	TRACED2, FSMC_A21, TIM9_CH1, DCMI_D6, EVENTOUT	-
-	-	5	5	5	B3	PE6	I/O	FT	-	TRACED3, FSMC_A22, TIM9_CH2, DCMI_D7, EVENTOUT	-
1	A9	6	6	6	C1	V_{BAT}	S		-	-	-
-	-	-	-	7	D2	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_AF2
2	B8	7	7	8	D1	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1
3	B9	8	8	9	E1	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN[4]
4	C9	9	9	10	F1	PC15-OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT[4]
-	-	-	-	11	D3	PI9	I/O	FT	-	CAN1_RX,EVENTOUT	-
-	-	-	-	12	E3	PI10	I/O	FT	-	ETH_MII_RX_ER, EVENTOUT	-
-	-	-	-	13	E4	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	-	-	14	F2	V_{SS}	S		-	-	-
-	-	-	-	15	F3	V_{DD}	S		-	-	-
-	-	-	10	16	E2	PF0	I/O	FT	-	FSMC_A0, I2C2_SDA, EVENTOUT	-
-	-	-	11	17	H3	PF1	I/O	FT	-	FSMC_A1, I2C2_SCL, EVENTOUT	-
-	-	-	12	18	H2	PF2	I/O	FT	-	FSMC_A2, I2C2_SMBA, EVENTOUT	-
-	-	-	13	19	J2	PF3	I/O	FT	(4)	FSMC_A3, EVENTOUT	ADC3_IN9

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
38	F2	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	-
39	F3	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	D1	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	E2	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	E3	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	D3	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	D2	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4,OTG_FS_DM, EVENTOUT	-
45	C1	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	B2	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	C2	73	106	125	F13	V_{CAP_2}	S	-	-	-	-
-	B1	74	107	126	F12	V_{SS}	S	-	-	-	-
48	A8	75	108	127	G13	V_{DD}	S	-	-	-	-
-	-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

Table 9. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	**NOR/PSRAM/SRAM**	**NOR/PSRAM Mux**	**NAND 16 bit**	
PE5	-	A21	A21	-	Yes
PE6	-	A22	A22	-	Yes
PF0	A0	A0	-	-	-
PF1	A1	A1	-	-	-
PF2	A2	A2	-	-	-
PF3	A3	A3	-	-	-
PF4	A4	A4	-	-	-
PF5	A5	A5	-	-	-
PF6	NIORD	-	-	-	-
PF7	NREG	-	-	-	-
PF8	NIOWR	-	-	-	-
PF9	CD	-	-	-	-
PF10	INTR	-	-	-	-
PF12	A6	A6	-	-	-
PF13	A7	A7	-	-	-
PF14	A8	A8	-	-	-
PF15	A9	A9	-	-	-
PG0	A10	A10	-	-	-
PG1	-	A11	-	-	-
PE7	D4	D4	DA4	D4	Yes
PE8	D5	D5	DA5	D5	Yes
PE9	D6	D6	DA6	D6	Yes
PE10	D7	D7	DA7	D7	Yes
PE11	D8	D8	DA8	D8	Yes
PE12	D9	D9	DA9	D9	Yes
PE13	D10	D10	DA10	D10	Yes
PE14	D11	D11	DA11	D11	Yes
PE15	D12	D12	DA12	D12	Yes
PD8	D13	D13	DA13	D13	Yes
PD9	D14	D14	DA14	D14	Yes
PD10	D15	D15	DA15	D15	Yes
PD11	-	A16	A16	CLE	Yes
PD12	-	A17	A17	ALE	Yes

Table 10. Alternate function mapping (continued)

Port		AF0 SYS	AF1 TIM1/2	AF2 TIM3/4/5	AF3 TIM8/9/10/11	AF4 I2C1/I2C2/I2C3	AF5 SPI1/SPI2/I2S2	AF6 SPI3/I2S3	AF7 USART1/2/3	AF8 UART4/5/ USART6	AF9 CAN1/CAN2/ TIM12/13/14	AF10 OTG_FS/ OTG_HS	AF11 ETH	AF12 FSMC/SDIO/ OTG_HS	AF13 DCMI	AF014	AF15
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH _MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	-	OTG_HS_ULPI_D2	ETH _MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_SCK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	-	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT	-	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH _MII_TXD3	SDIO_D4	DCMI_D6	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_SCK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH _MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_SCK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	-	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_50Hz	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Table 22. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max[1]		Unit
				$T_A = 25\ °C$	$T_A = 85\ °C$	$T_A = 105\ °C$	
I_{DD}	Supply current in Sleep mode	External clock[2], all peripherals enabled[3]	120 MHz	38	51	61	mA
			90 MHz	30	43	53	
			60 MHz	20	33	43	
			30 MHz	11	25	35	
			25 MHz	8	21	31	
			16 MHz	6	19	29	
			8 MHz	3.6	17.0	27.0	
			4 MHz	2.4	15.4	25.3	
			2 MHz	1.9	14.9	24.7	
		External clock[2], all peripherals disabled	120 MHz	8	21	31	
			90 MHz	7	20	30	
			60 MHz	5	18	28	
			30 MHz	3.5	16.0	26.0	
			25 MHz	2.5	16.0	25.0	
			16 MHz	2.1	15.1	25.0	
			8 MHz	1.7	15.0	25.0	
			4 MHz	1.5	14.6	24.6	
			2 MHz	1.4	14.2	24.3	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.

2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.

3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 31. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	-	-	-	1	µA
g_m	Oscillator Transconductance	-	2.8	-	-	µA/V
$t_{SU(LSE)}$[2]	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.

2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: *For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

Figure 33. Typical application with a 32.768 kHz crystal
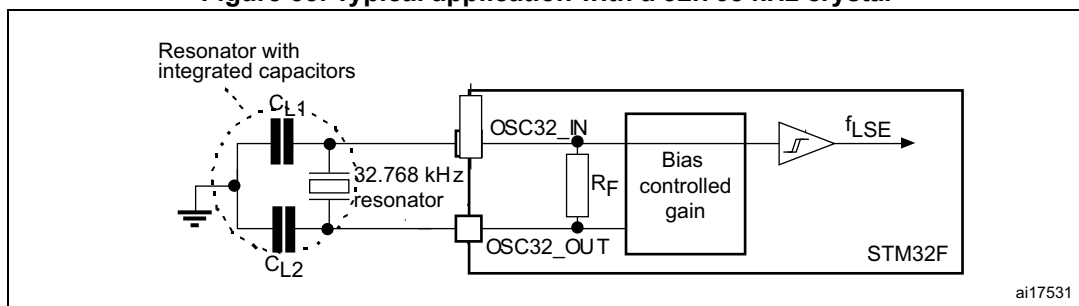
6.3.9 Internal clock source characteristics

The parameters given in *Table 32* and *Table 33* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 32. HSI oscillator characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user-trimming step[2]	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C[3]	– 8	-	4.5	%
		T_A = –10 to 85 °C[3]	– 4	-	4	%
		T_A = 25 °C[4]	– 1	-	1	%
$t_{su(HSI)}$[2]	HSI oscillator startup time	-	-	2.2	4.0	µs
$I_{DD(HSI)}$[2]	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Guaranteed by characterization results.

4. Factory calibrated, parts not soldered.

Table 34. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter[3]	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$[4]	PLL power consumption on VDD	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$[4]	PLL power consumption on VDDA	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.

2. Guaranteed by design, not tested in production.

3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.

4. Guaranteed by characterization results, not tested in production.

Table 35. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock[1]	-	0.95[2]	1	2.10[2]	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-	-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output	-	192	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 47. Output voltage characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}[2]	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS ports I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}[3]	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL}[2]	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL ports I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}[3]	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}[2][4]	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}[3][4]	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}[2][4]	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}[3][4]	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).

2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

4. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 48. I/O AC characteristics[1]

OSPEEDRy [1:0] bit value[1]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns

Figure 39. I/O AC characteristics definition
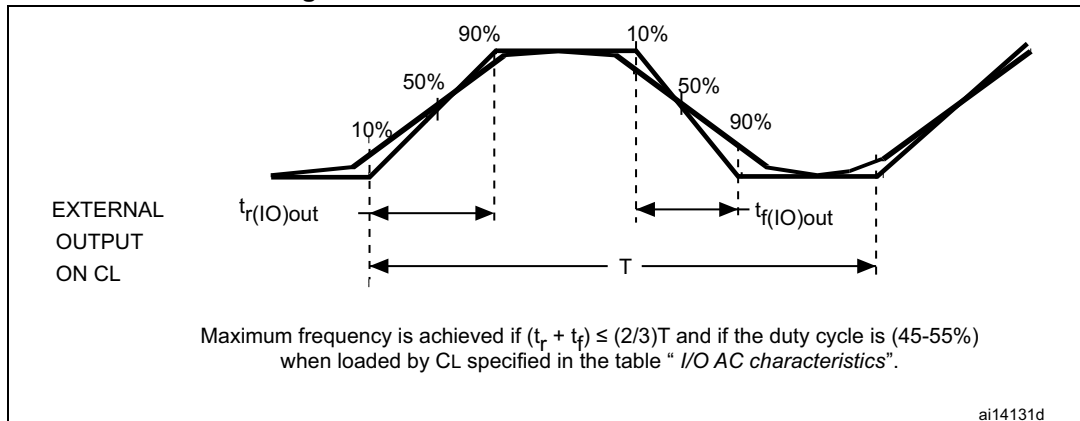
6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 49*).

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor[1]	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$[2]	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$[2]	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2. Guaranteed by design, not tested in production.

Figure 40. Recommended NRST pin protection
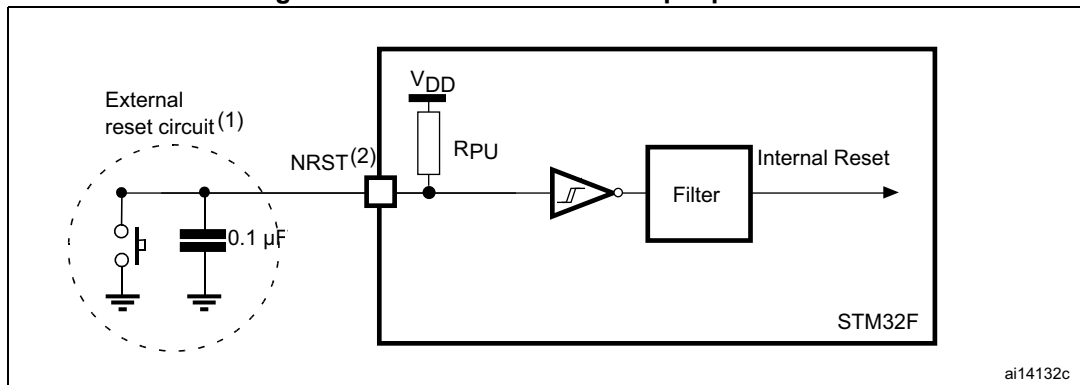
1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 49*. Otherwise the reset is not taken into account by the device.

Table 76. Synchronous multiplexed NOR/PSRAM read timings[1][2] (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	5	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.

Figure 62. Synchronous multiplexed PSRAM write timings
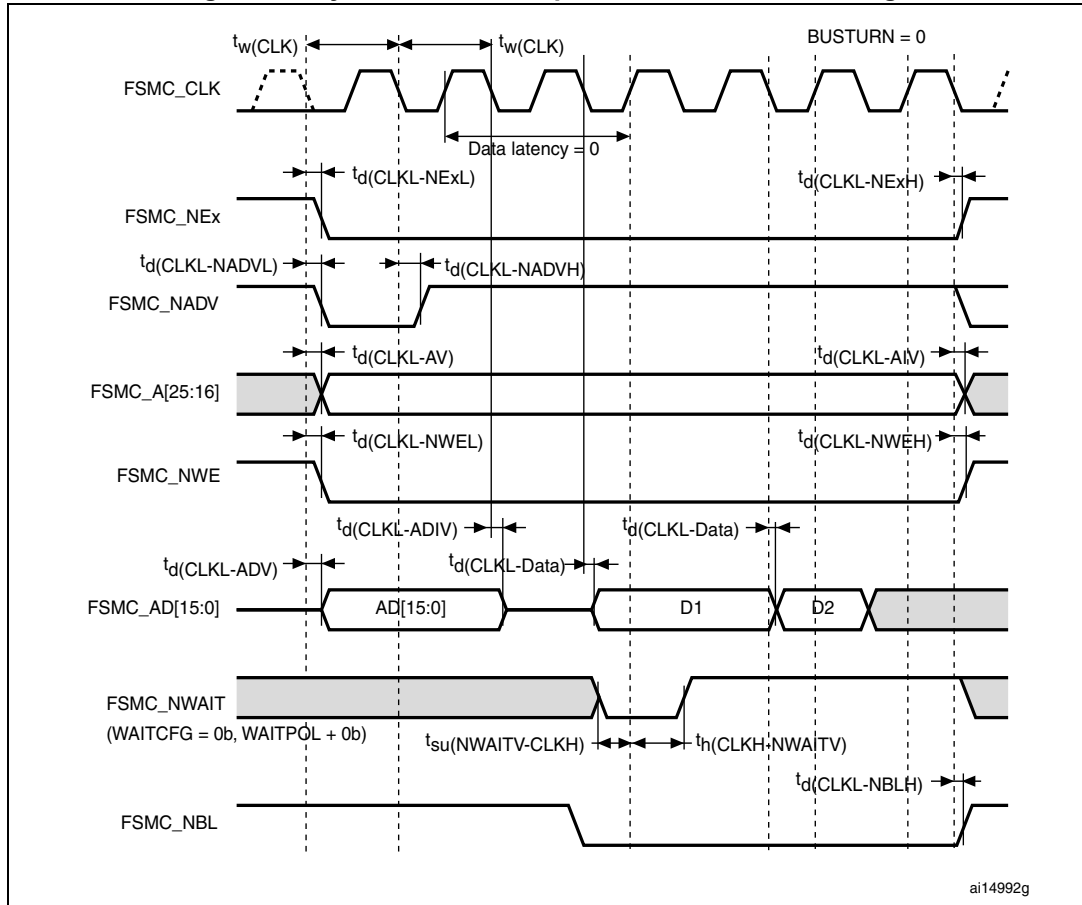
Table 77. Synchronous multiplexed PSRAM write timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}- 1$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16...25)	7	-	ns

Table 81. Switching characteristics for PC Card/CF read and write cycles in I/O space[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK} - 0.5$	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK} - 1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK} - 3$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK} + 1.5$	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK} + 1$	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK} - 0.5$	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK} + 1$	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 71 through *Figure 74* represent synchronous waveforms, together with *Table 82* and *Table 83* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

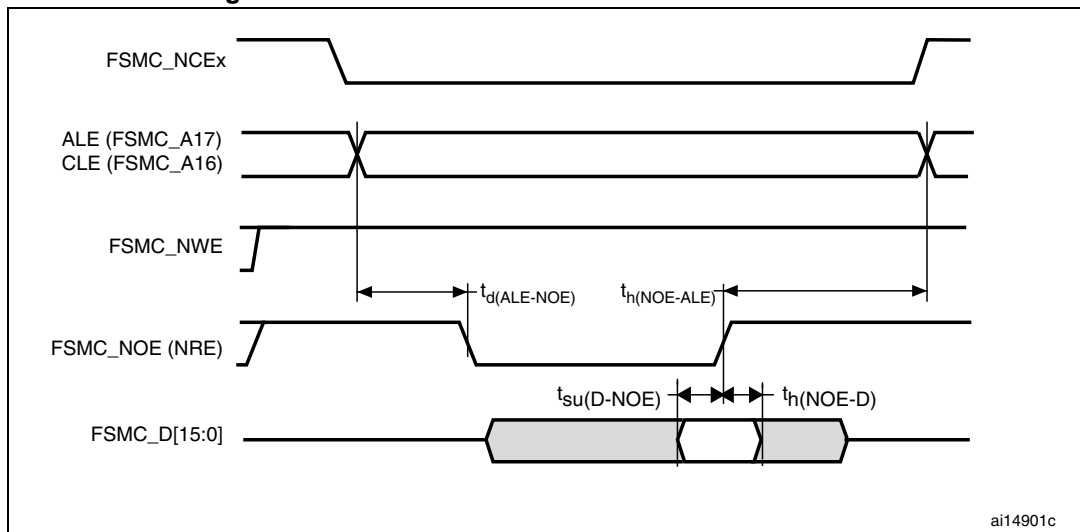### Figure 71. NAND controller waveforms for read access

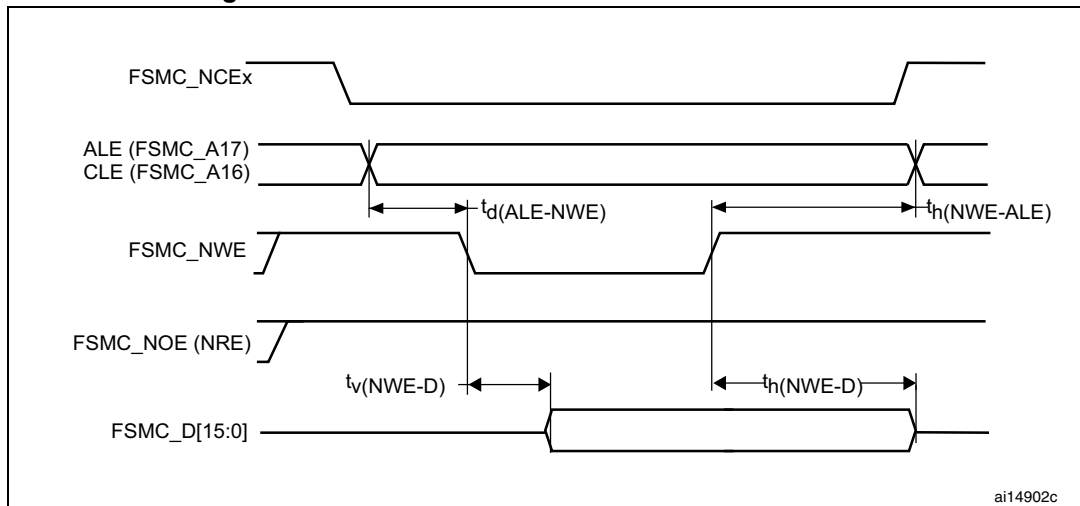### Figure 72. NAND controller waveforms for write access

Table 83. Switching characteristics for NAND Flash write cycles[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}- 1$	$4T_{HCLK}+ 3$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}+ 2$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}- 2$	-	ns

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.

6.3.26 Camera interface (DCMI) timing specifications

Table 84. DCMI characteristics

Symbol	Parameter	Conditions	Min	Max
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	DCMI_PIXCLK= 48 MHz	-	0.4

6.3.27 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 85* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).
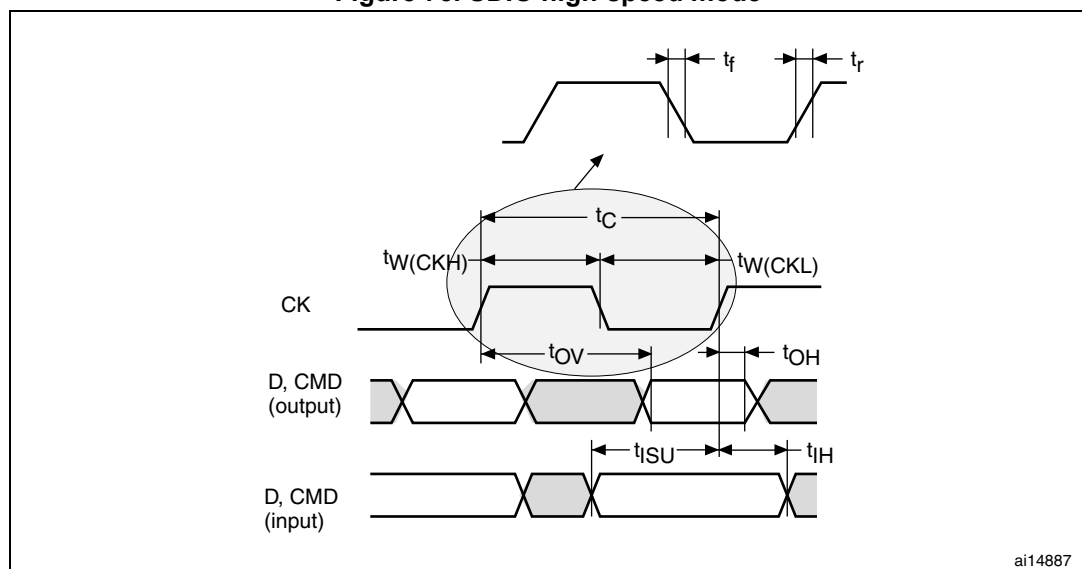
Figure 75. SDIO high-speed mode

7.6 UFBGA176+25 package information

**Figure 89. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch,
ultra fine pitch ball grid array package outline**

1. Drawing is not to scale.

**Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch,
ultra fine pitch ball grid array package mechanical data**

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 97. Document revision history (continued)

Date	Revision	Changes
13-Jul-2010	4 (continued)	Added USB OTG_FS features in *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)*. Updated V_{CAP_1} and V_{CAP_2} capacitor value to 2.2 µF in *Figure 19: Power supply scheme*. Removed DAC, modified ADC limitations, and updated I/O compensation for 1.8 to 2.1 V range in *Table 15: Limitations depending on the operating power supply range*. Added V_{BORL}, V_{BORM}, V_{BORH} and I_{RUSH} in *Table 19: Embedded reset and power control block characteristics*. Removed table Typical current consumption in Sleep mode with Flash memory in Deep power down mode. Merged typical and maximum current consumption sections and added *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*, *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM, Table 22: Typical and maximum current consumption in Sleep mode, Table 23: Typical and maximum current consumptions in Stop mode, Table 24: Typical and maximum current consumptions in Standby mode*, and *Table 25: Typical and maximum current consumptions in VBAT mode*. Update *Table 34: Main PLL characteristics* and added *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Added *Note 8* for CIO in *Table 48: I/O AC characteristics*. Updated *Section 6.3.18: TIM timer characteristics*. Added T_{NRST_OUT} in *Table 49: NRST pin characteristics*. Updated *Table 52: I2C characteristics*. Removed 8-bit data in and data out waveforms from *Figure 48: ULPI timing diagram*. Removed note related to ADC calibration in *Table 67*. *Section 6.3.20: 12-bit ADC characteristics*: ADC characteristics tables merged into one single table; tables ADC conversion time and ADC accuracy removed. Updated *Table 68: DAC characteristics*. Updated *Section 6.3.22: Temperature sensor characteristics* and *Section 6.3.23: VBAT monitoring characteristics*. Update *Section 6.3.26: Camera interface (DCMI) timing specifications*. Added *Section 6.3.27: SD/SDIO MMC card host interface (SDIO) characteristics*, and *Section 6.3.28: RTC characteristics*. Added *Section 7.7: Thermal characteristics*. Updated *Table 91: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data* and *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Changed tape and reel code to TX in *Table 96: Ordering information scheme*. Added *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Updated figures in Appendix *A.2: USB OTG full speed (FS) interface solutions* and *A.3: USB OTG high speed (HS) interface solutions*. Updated *Figure 94: Audio player solution using PLL, PLLI2S, USB and 1 crystal* and *Figure 95: Audio PLL (PLLI2S) providing accurate I2S clock*.