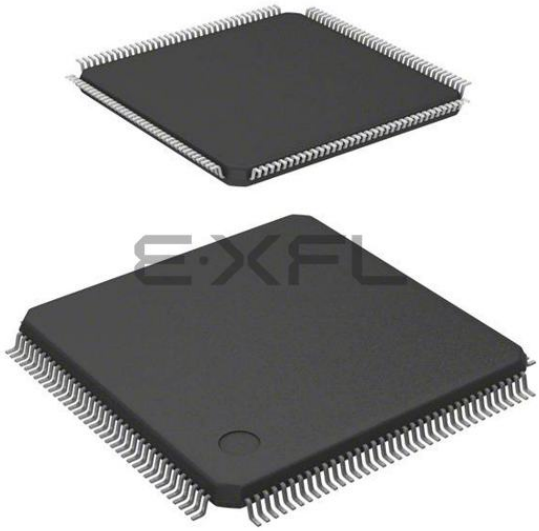


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205zft6

Figure 2. Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package

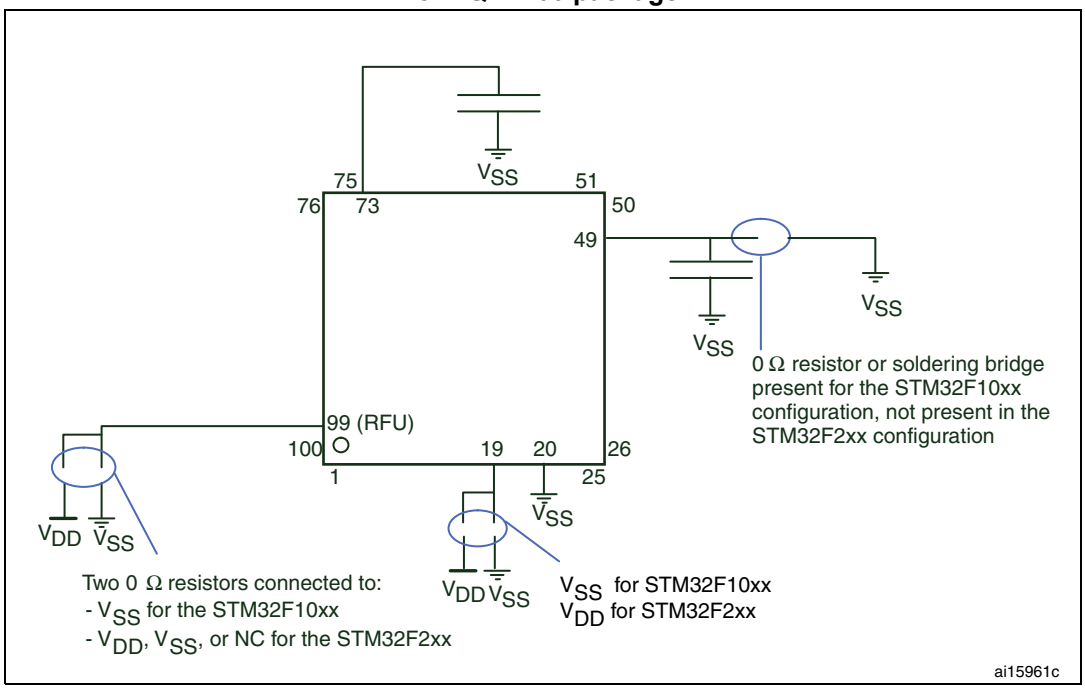
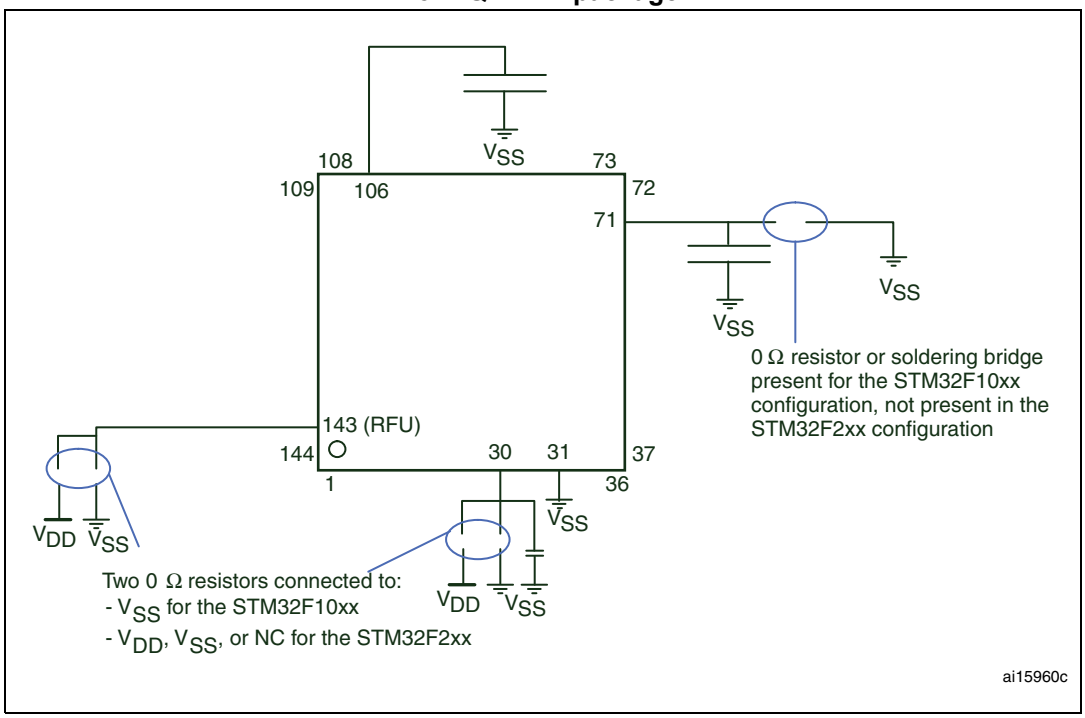
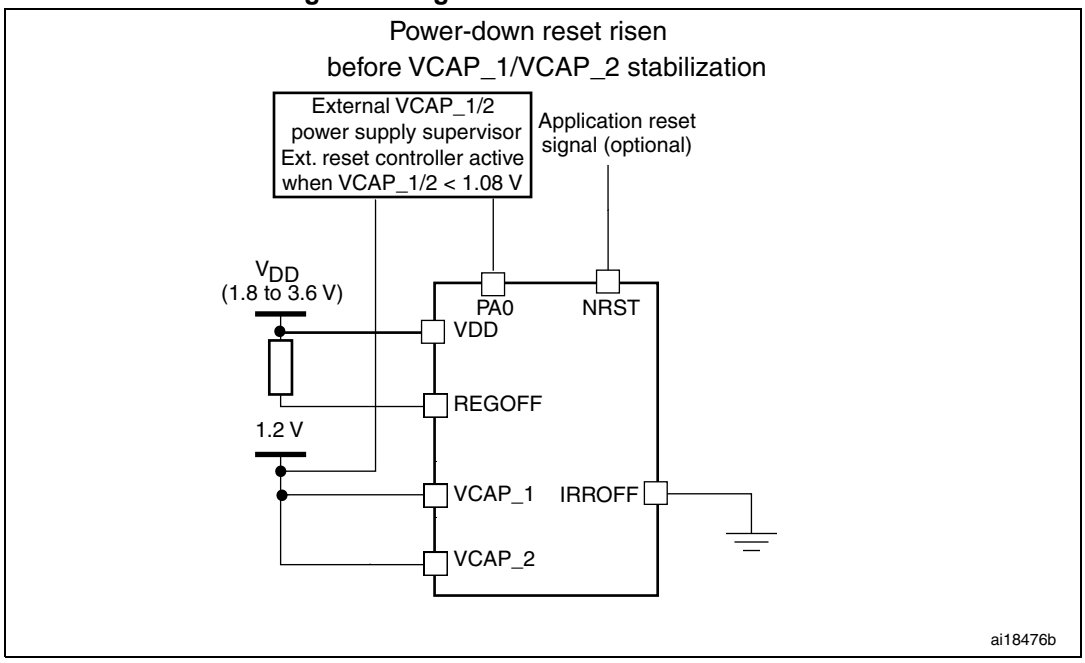


Figure 3. Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package



1. RFU = reserved for future use.

Figure 6. Regulator OFF/internal reset ON



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 8*).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD}. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.
The counter can be frozen in debug mode.

3.20.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.21 Inter-integrated circuit interface (I²C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

3.22 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F20x devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-
-	-	-	-	85	M12	PH8	I/O	FT	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	86	M13	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	-
-	-	-	-	87	L13	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	88	L12	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	89	K12	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	90	H12	V_{SS}	S	-	-	-	-
-	-	-	-	91	J12	V_{DD}	S	-	-	-	-
33	J1	51	73	92	P12	PB12	I/O	FT	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-
34	H2	52	74	93	P13	PB13	I/O	FT	-	SPI2_SCK, I2S2_SCK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_ VBUS
35	H1	53	75	94	R14	PB14	I/O	FT	-	SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM USART3_RTS, TIM8_CH2N, EVENTOUT	-
36	G1	54	76	95	R15	PB15	I/O	FT	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, RTC_50Hz, EVENTOUT	-
-	-	55	77	96	P15	PD8	I/O	FT	-	FSMC_D13, USART3_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
54	C7	83	116	144	D12	PD2	I/O	FT	-	TIM3_ETR,UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	-	84	117	145	D11	PD3	I/O	FT	-	FSMC_CLK,USART2_CTS, EVENTOUT	-
-	-	85	118	146	D10	PD4	I/O	FT	-	FSMC_NOE, USART2_RTS, EVENTOUT	-
-	-	86	119	147	C11	PD5	I/O	FT	-	FSMC_NWE,USART2_TX, EVENTOUT	-
-	-	-	120	148	D8	V_{SS}	S	-	-	-	-
-	-	-	121	149	C8	V_{DD}	S	-	-	-	-
-	-	87	122	150	B11	PD6	I/O	FT	-	FSMC_NWAIT, USART2_RX, EVENTOUT	-
-	-	88	123	151	A11	PD7	I/O	FT	-	USART2_CK,FSMC_NE1, FSMC_NCE2, EVENTOUT	-
-	-	-	124	152	C10	PG9	I/O	FT	-	USART6_RX, FSMC_NE2,FSMC_NCE3, EVENTOUT	-
-	-	-	125	153	B10	PG10	I/O	FT	-	FSMC_NCE4_1, FSMC_NE3, EVENTOUT	-
-	-	-	126	154	B9	PG11	I/O	FT	-	FSMC_NCE4_2, ETH_MII_TX_EN , ETH _RMII_TX_EN, EVENTOUT	-
-	-	-	127	155	B8	PG12	I/O	FT	-	FSMC_NE4, USART6_RTS, EVENTOUT	-
-	-	-	128	156	A8	PG13	I/O	FT	-	FSMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-
-	-	-	129	157	A7	PG14	I/O	FT	-	FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT	-
-	-	-	130	158	D7	V_{SS}	S	-	-	-	-

Table 10. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port A	PA0-WKUP	-	TIM2_CH1_ETR	TIM 5_CH1	TIM8_ETR	-	-		USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-		USART2_RTS	UART4_RX	-	-	ETH_MII _RX_CLK ETH_RMII _REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-		USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-		USART2_RX	-	-	OTG_HS_ULPI_D0	ETH _MII_COL	-	-	-	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-		-	OTG_HS_SOF	DCMI_HSYNC	-	EVENTOUT
	PA5	-	TIM2_CH1_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_C K	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII _RX_DV ETH_RMII _CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-		-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-	-	-	-	-	-	-	-	EVENTOUT

6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 17. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator OFF)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz and 3 wait states from 90 to 120 MHz).
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM (1)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(2)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(3), all peripherals enabled(4)	120 MHz	49	63	72	mA
			90 MHz	38	51	61	
			60 MHz	26	39	49	
			30 MHz	14	27	37	
			25 MHz	11	24	34	
			16 MHz(5)	8	21	30	
			8 MHz	5	17	27	
			4 MHz	3	16	26	
			2 MHz	2	15	25	
		External clock(3), all peripherals disabled	120 MHz	21	34	44	
			90 MHz	17	30	40	
			60 MHz	12	25	35	
			30 MHz	7	20	30	
			25 MHz	5	18	28	
			16 MHz(5)	4.0	17.0	27.0	
			8 MHz	2.5	15.5	25.5	
			4 MHz	2.0	14.7	24.8	
			2 MHz	1.6	14.5	24.6	

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
3. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
4. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. In this case HCLK = system clock/2.

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator and RTC ON	3.0	3.4	4.0	15.1	25.8	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	2.4	2.7	3.3	12.4	20.5	
		Backup SRAM ON, RTC OFF	2.4	2.6	3.0	12.5	24.8	
		Backup SRAM OFF, RTC OFF	1.7	1.9	2.2	9.8	19.2	

1. Guaranteed by characterization results, not tested in production.

Table 25. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	12	19	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	8	10	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	9	16	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	5	7	

1. Guaranteed by characterization results, not tested in production.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 28* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 28. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	26	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 29* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 29. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Table 37. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V_{DD} = 3.3 V	-	12	-	

Table 38. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 56. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

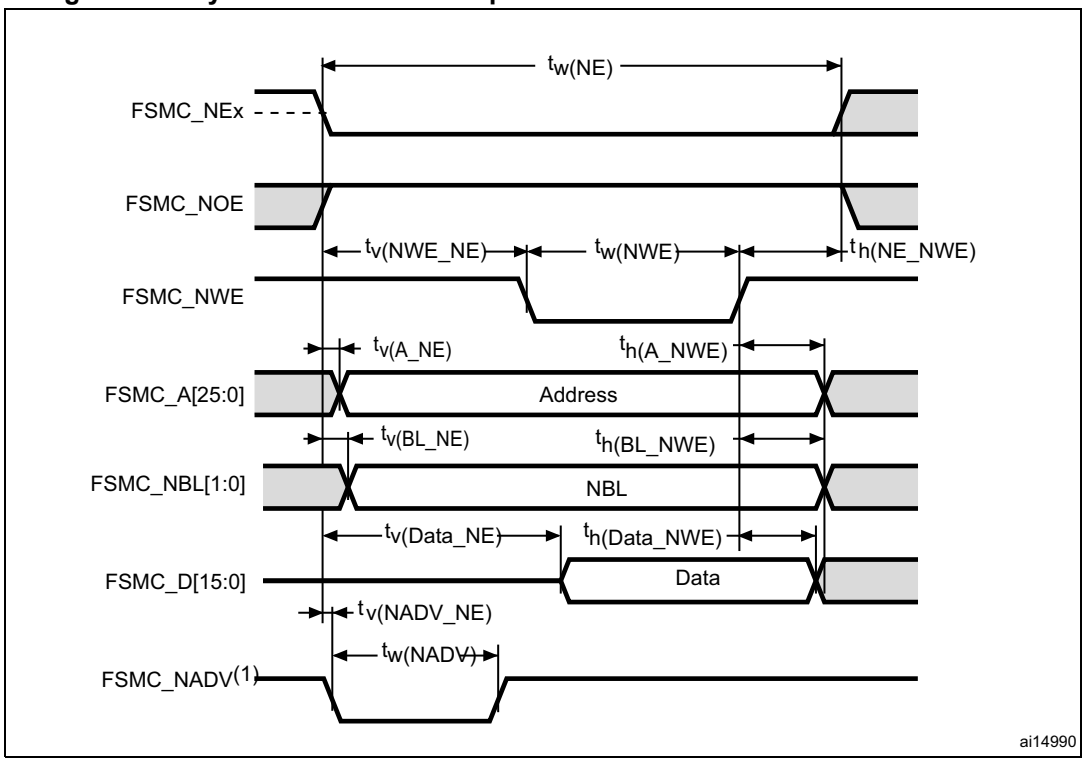
1. Guaranteed by design, not tested in production.

Table 57. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Figure 58. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 73. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+4$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK}-0.5$	$T_{HCLK}+3$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK}-3$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK}-1$	-	ns
$t_{v(Data\_NE)}$	Data to FSMC_NEx low to Data valid	-	$T_{HCLK}+5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK}+1.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Table 79. Synchronous non-multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	6	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	8	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	2	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	2	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

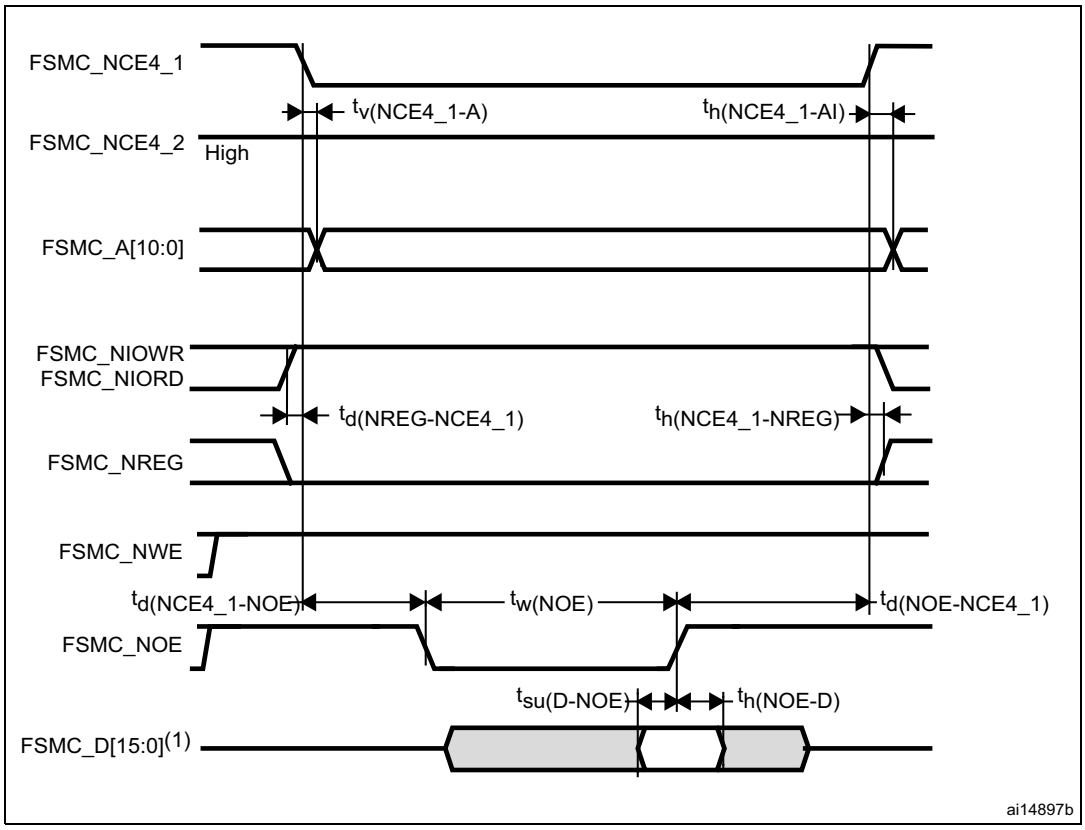
PC Card/CompactFlash controller waveforms and timings

Figure 65 through *Figure 70* represent synchronous waveforms, with *Table 80* and *Table 81* providing the corresponding timings. The results shown in these table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 67. PC Card/CompactFlash controller waveforms for attribute memory read access



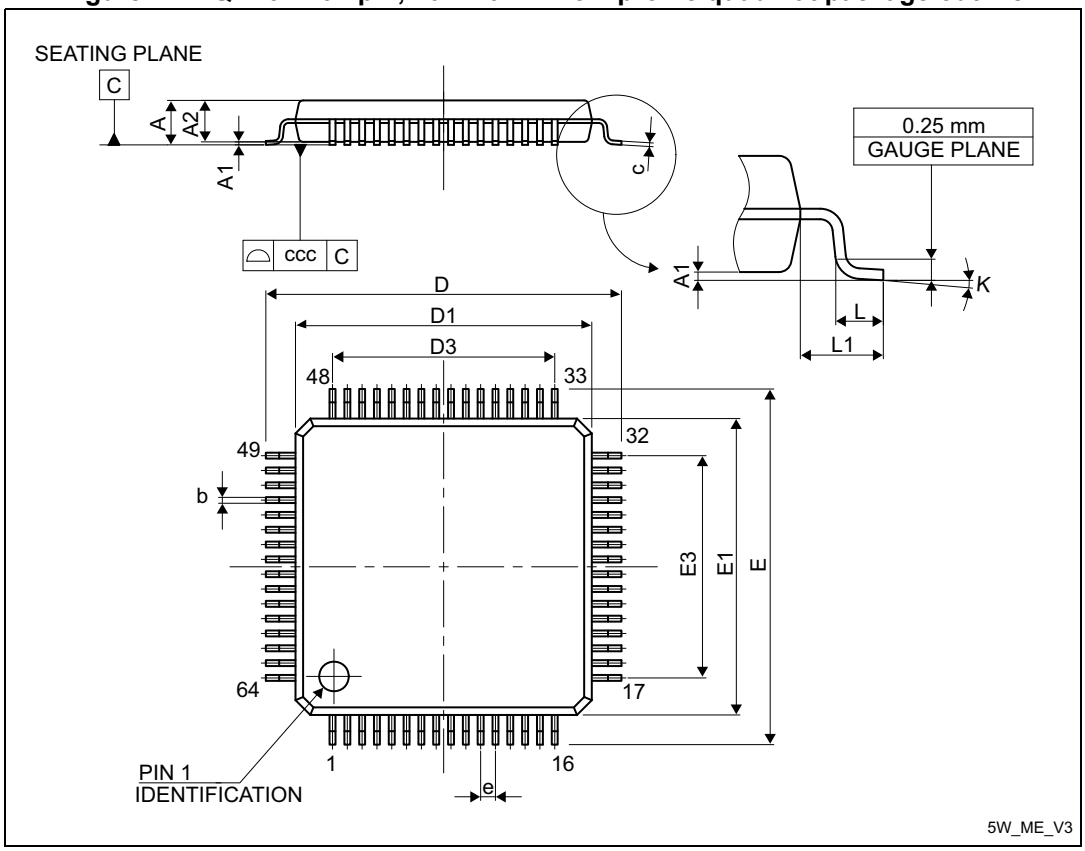
1. Only data bits 0...7 are read (bits 8...15 are disregarded).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

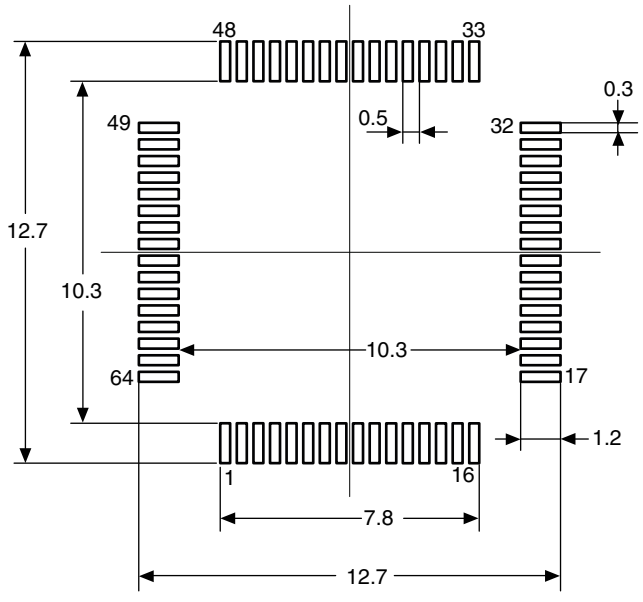
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

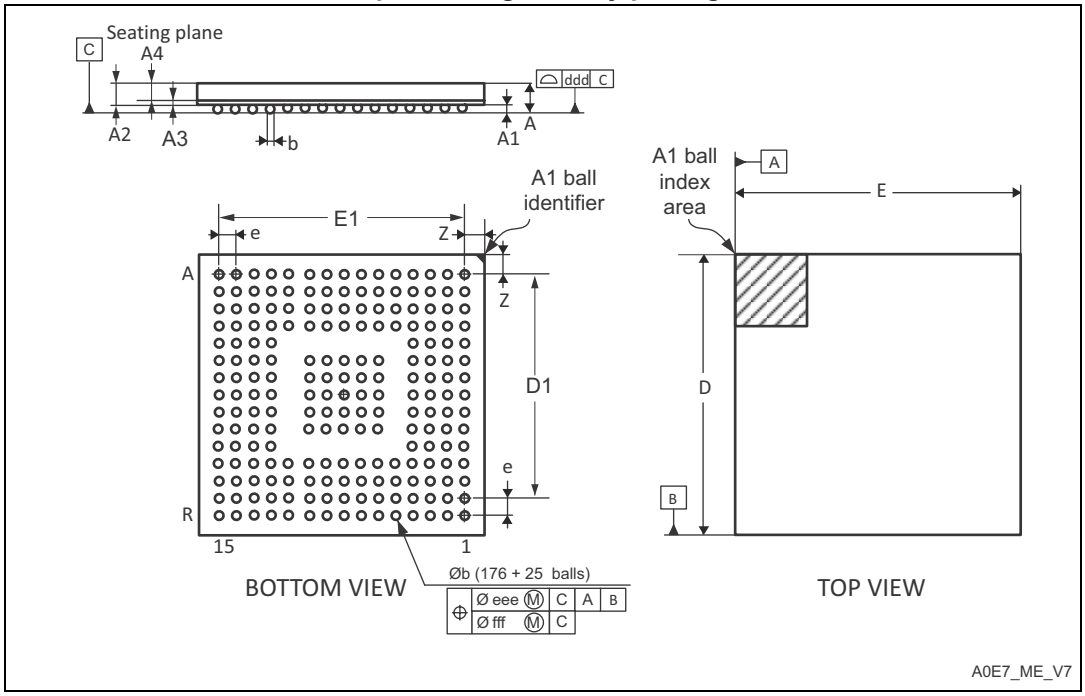
Figure 78. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.6 UFBGA176+25 package information

Figure 89. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 97. Document revision history (continued)

Date	Revision	Changes
13-Jul-2010	4 (continued)	Added USB OTG_FS features in *Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS)*. Updated V_{CAP_1} and V_{CAP_2} capacitor value to 2.2 µF in *Figure 19: Power supply scheme*. Removed DAC, modified ADC limitations, and updated I/O compensation for 1.8 to 2.1 V range in *Table 15: Limitations depending on the operating power supply range*. Added V_{BORL}, V_{BORM}, V_{BORH} and I_{RUSH} in *Table 19: Embedded reset and power control block characteristics*. Removed table Typical current consumption in Sleep mode with Flash memory in Deep power down mode. Merged typical and maximum current consumption sections and added *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*, *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM, Table 22: Typical and maximum current consumption in Sleep mode, Table 23: Typical and maximum current consumptions in Stop mode, Table 24: Typical and maximum current consumptions in Standby mode*, and *Table 25: Typical and maximum current consumptions in VBAT mode*. Update *Table 34: Main PLL characteristics* and added *Section 6.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Added *Note 8* for CIO in *Table 48: I/O AC characteristics*. Updated *Section 6.3.18: TIM timer characteristics*. Added T_{NRST_OUT} in *Table 49: NRST pin characteristics*. Updated *Table 52: I2C characteristics*. Removed 8-bit data in and data out waveforms from *Figure 48: ULPI timing diagram*. Removed note related to ADC calibration in *Table 67*. *Section 6.3.20: 12-bit ADC characteristics*: ADC characteristics tables merged into one single table; tables ADC conversion time and ADC accuracy removed. Updated *Table 68: DAC characteristics*. Updated *Section 6.3.22: Temperature sensor characteristics* and *Section 6.3.23: VBAT monitoring characteristics*. Update *Section 6.3.26: Camera interface (DCMI) timing specifications*. Added *Section 6.3.27: SD/SDIO MMC card host interface (SDIO) characteristics*, and *Section 6.3.28: RTC characteristics*. Added *Section 7.7: Thermal characteristics*. Updated *Table 91: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data* and *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Changed tape and reel code to TX in *Table 96: Ordering information scheme*. Added *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Updated figures in Appendix *A.2: USB OTG full speed (FS) interface solutions* and *A.3: USB OTG high speed (HS) interface solutions*. Updated *Figure 94: Audio player solution using PLL, PLLI2S, USB and 1 crystal* and *Figure 95: Audio PLL (PLLI2S) providing accurate I2S clock*.