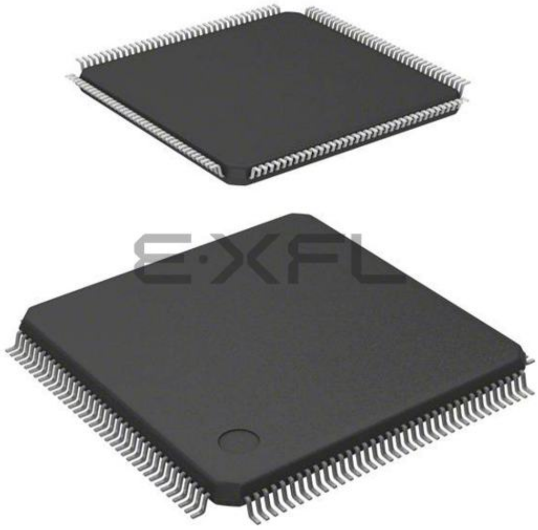


Welcome to E-XFL.COM

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 132K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205zgt6 |

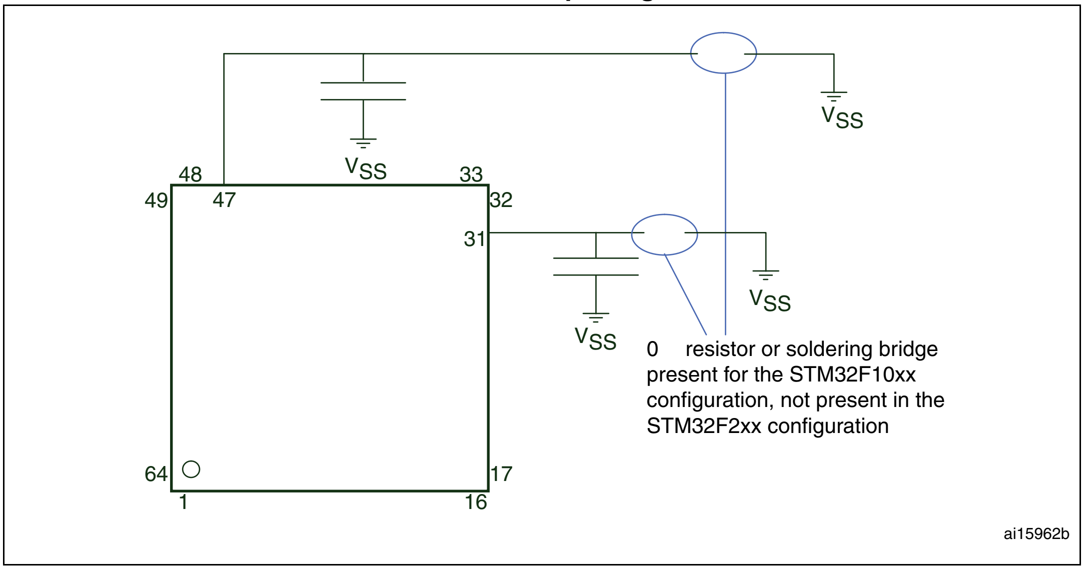
## 2.1 Full compatibility throughout the family

The STM32F205xx and STM32F207xx constitute the STM32F20x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F205xx and STM32F207xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F205xx and STM32F207xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F20x family remains simple as only a few pins are impacted.

*Figure 1*, *Figure 2* and *Figure 3* provide compatible board designs between the STM32F20x and the STM32F10xxx family.

**Figure 1. Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package**



## 3.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

## 3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.6 Embedded SRAM

All STM32F20x products embed:

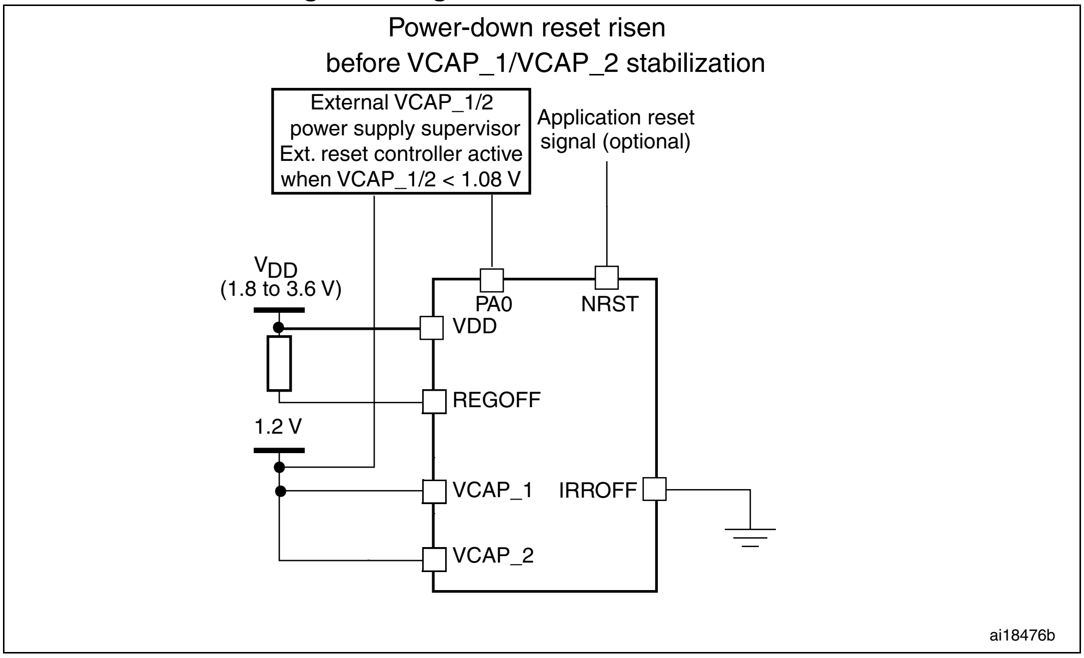
- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.

## 3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 6. Regulator OFF/internal reset ON**




The following conditions must be respected:

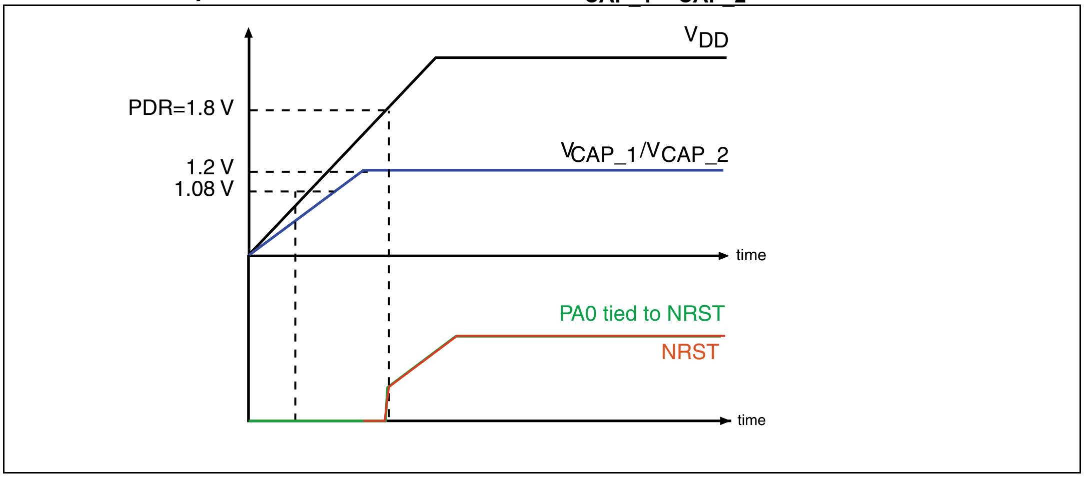
- $V_{DD}$ should always be higher than $V_{CAP\_1}$ and $V_{CAP\_2}$ to avoid current injection between power domains.
- If the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach 1.08 V is faster than the time for $V_{DD}$ to reach 1.8 V, then PA0 should be kept low to cover both conditions: until $V_{CAP\_1}$ and $V_{CAP\_2}$ reach 1.08 V and until $V_{DD}$ reaches 1.8 V (see *Figure 8*).
- Otherwise, If the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach 1.08 V is slower than the time for $V_{DD}$ to reach 1.8 V, then PA0 should be asserted low externally (see *Figure 9*).
- If $V_{CAP\_1}$ and $V_{CAP\_2}$ go below 1.08 V and $V_{DD}$ is higher than 1.8 V, then a reset must be asserted on PA0 pin.

### Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to $V_{SS}$ and IRROFF to $V_{DD}$. IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through $V_{CAP\_1}$ and $V_{CAP\_2}$ pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external $V_{DD}$ supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The $V_{DD}$ specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

**Figure 8. Startup in regulator OFF: slow $V_{DD}$ slope - power-down reset risen after $V_{CAP\_1}/V_{CAP\_2}$ stabilization**




1. This figure is valid both whatever the internal reset mode (ON or OFF).

**Figure 9. Startup in regulator OFF: fast $V_{DD}$ slope - power-down reset risen before $V_{CAP\_1}/V_{CAP\_2}$ stabilization**

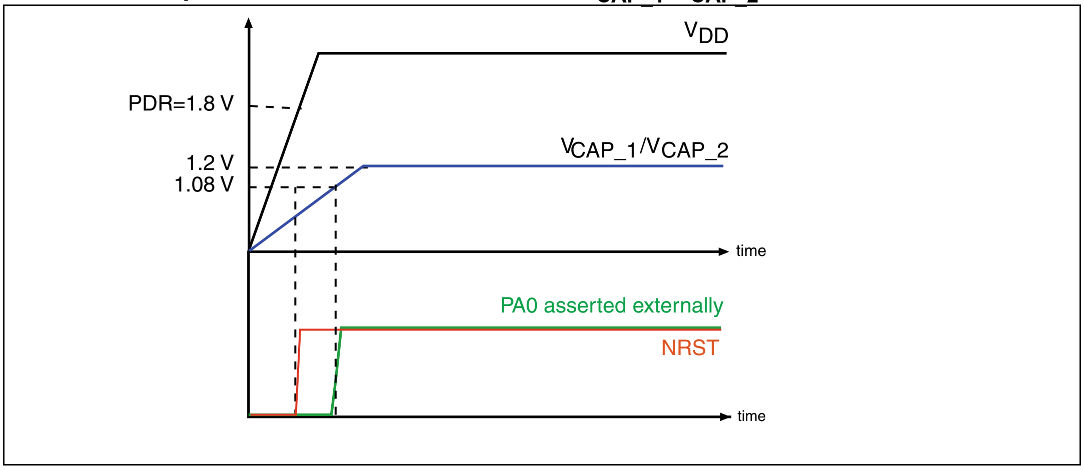
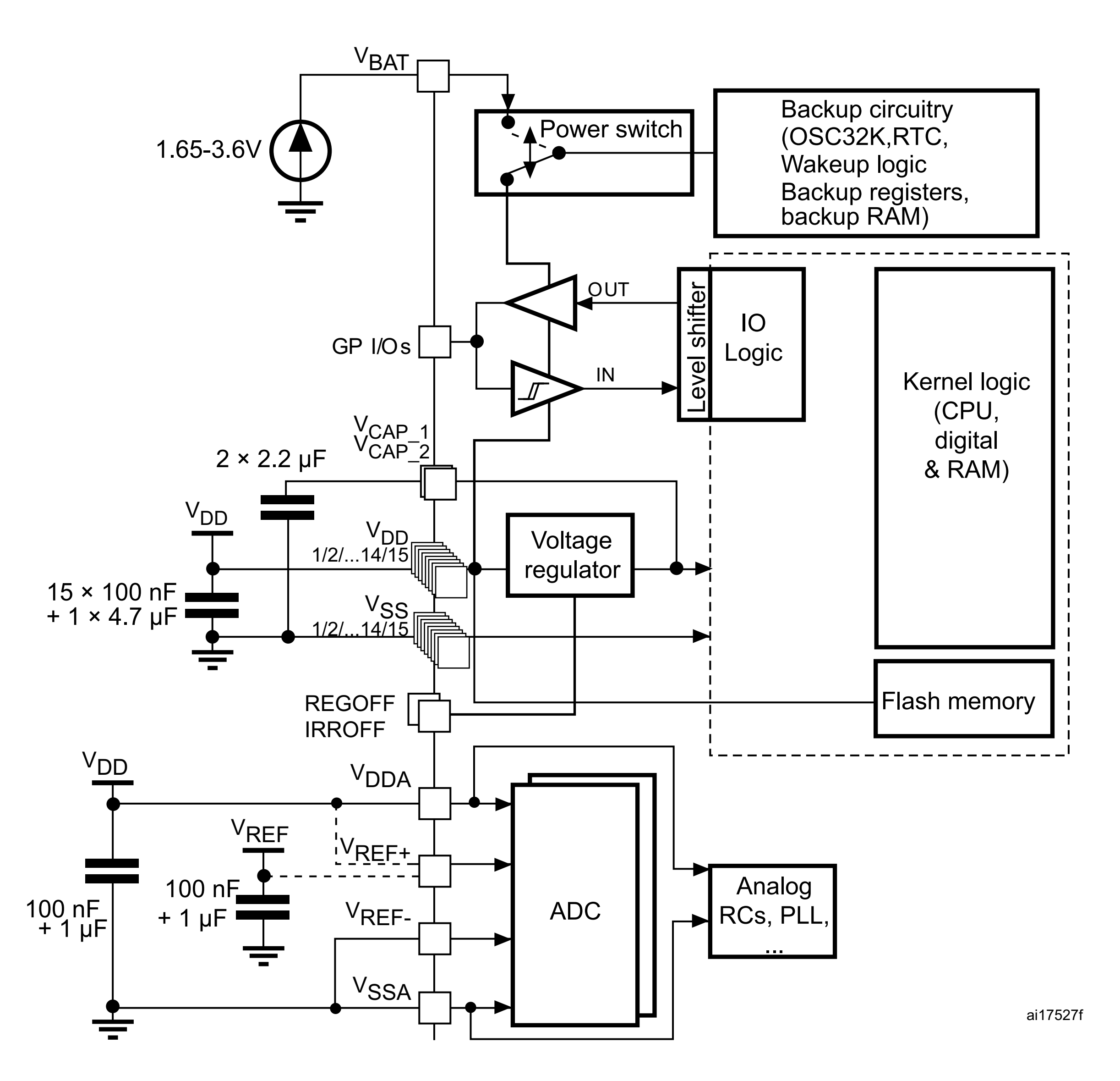


**Table 8. STM32F20x pin and ball definitions (continued)**

| Pins | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | - | 130 | D13 | PH15 | I/O | FT | - | TIM8_CH3N, DCMI_D11, EVENTOUT | - |
| - | - | - | - | 131 | E14 | PI0 | I/O | FT | - | TIM5_CH4, SPI2_NSS, I2S2_WS, DCMI_D13, EVENTOUT | - |
| - | - | - | - | 132 | D14 | PI1 | I/O | FT | - | SPI2_SCK, I2S2_SCK, DCMI_D8, EVENTOUT | - |
| - | - | - | - | 133 | C14 | PI2 | I/O | FT | - | TIM8_CH4 ,SPI2_MISO, DCMI_D9, EVENTOUT | - |
| - | - | - | - | 134 | C13 | PI3 | I/O | FT | - | TIM8_ETR, SPI2_MOSI, I2S2_SD, DCMI_D10, EVENTOUT | - |
| - | - | - | - | 135 | D9 | $V_{SS}$ | S | - | - | - | - |
| - | - | - | - | 136 | C9 | $V_{DD}$ | S | - | - | - | - |
| 49 | A1 | 76 | 109 | 137 | A14 | PA14 (JTCK-SWCLK) | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |
| 50 | A2 | 77 | 110 | 138 | A13 | PA15 (JTDI) | I/O | FT | - | JTDI, SPI3_NSS, I2S3_WS,TIM2_CH1_ETR, SPI1_NSS, EVENTOUT | - |
| 51 | B3 | 78 | 111 | 139 | B14 | PC10 | I/O | FT | - | SPI3_SCK, I2S3_SCK, UART4_TX, SDIO_D2, DCMI_D8, USART3_TX, EVENTOUT | - |
| 52 | C3 | 79 | 112 | 140 | B13 | PC11 | I/O | FT | - | UART4_RX, SPI3_MISO, SDIO_D3, DCMI_D4,USART3_RX, EVENTOUT | - |
| 53 | A3 | 80 | 113 | 141 | A12 | PC12 | I/O | FT | - | UART5_TX, SDIO_CK, DCMI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT | - |
| - | - | 81 | 114 | 142 | B12 | PD0 | I/O | FT | - | FSMC_D2,CAN1_RX, EVENTOUT | - |
| - | - | 82 | 115 | 143 | C12 | PD1 | I/O | FT | - | FSMC_D3, CAN1_TX, EVENTOUT | - |

### 6.1.6 Power supply scheme

**Figure 19. Power supply scheme**




1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect REGOFF and IRROFF pins, refer to *Section 3.16: Voltage regulator*.
3. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
4. The 4.7 µF ceramic capacitor must be connected to one of the $V_{DD}$ pin.

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB, to ensure good device operation. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect device operation.

**Table 15. Limitations depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency ($f_{Flashmax}$) | Number of wait states at maximum CPU frequency ($f_{CPUmax}$= 120 MHz)(1) | I/O operation | FSMC_CLK frequency for synchronous accesses | Possible Flash memory operations |
|---|---|---|---|---|---|---|
| $V_{DD}$ =1.8 to 2.1 V(2) | Conversion time up to 1 Msps | 16 MHz with no Flash memory wait state | 7(3) | – Degraded speed performance<br>– No I/O compensation | Up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1 Msps | 18 MHz with no Flash memory wait state | 6(3) | – Degraded speed performance<br>– No I/O compensation | Up to 30 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2 Msps | 24 MHz with no Flash memory wait state | 4(3) | – Degraded speed performance<br>– I/O compensation works | Up to 48 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(4) | Conversion time up to 2 Msps | 30 MHz with no Flash memory wait state | 3(3) | – Full-speed operation<br>– I/O compensation works | – Up to 60 MHz when $V_{DD}$ = 3.0 to 3.6 V<br>– Up to 48 MHz when $V_{DD}$ = 2.7 to 3.0 V | 32-bit erase and program operations |

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to $V_{DD}$, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

### 6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 14*.

**Table 19. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | V |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | V |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | V |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | V |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | V |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | V |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | V |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | V |
| | | PLS[2:0]=101 (falling edge) | 2.65 | 2.84 | 3.02 | V |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | V |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | V |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | V |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | V |
| $V_{PVDhyst}$(1) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60 | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | V |
| $V_{PDRhyst}$(1) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR1}$ | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | V |

**Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | Max[1] | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | External clock[2], all peripherals enabled[3] | 120 MHz | 61 | 81 | 93 | mA |
| | | | 90 MHz | 48 | 68 | 80 | |
| | | | 60 MHz | 33 | 53 | 65 | |
| | | | 30 MHz | 18 | 38 | 50 | |
| | | | 25 MHz | 14 | 34 | 46 | |
| | | | 16 MHz[4] | 10 | 30 | 42 | |
| | | | 8 MHz | 6 | 26 | 38 | |
| | | | 4 MHz | 4 | 24 | 36 | |
| | | | 2 MHz | 3 | 23 | 35 | |
| | | External clock[2], all peripherals disabled | 120 MHz | 33 | 54 | 66 | |
| | | | 90 MHz | 27 | 47 | 59 | |
| | | | 60 MHz | 19 | 39 | 51 | |
| | | | 30 MHz | 11 | 31 | 43 | |
| | | | 25 MHz | 8 | 28 | 41 | |
| | | | 16 MHz[4] | 6 | 26 | 38 | |
| | | | 8 MHz | 4 | 24 | 36 | |
| | | | 4 MHz | 3 | 23 | 35 | |
| | | | 2 MHz | 2 | 23 | 34 | |

1. Guaranteed by characterization results, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

### On-chip peripheral current consumption

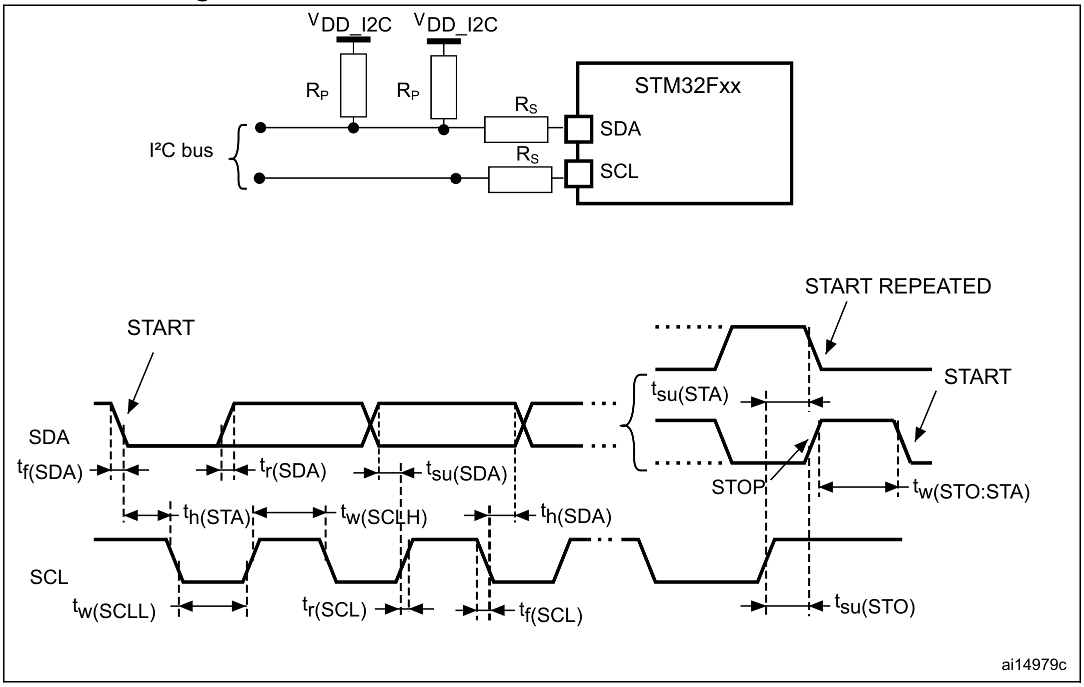
The current consumption of the on-chip peripherals is given in *Table 26*. The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- The code is running from Flash memory and the Flash memory access time is equal to 3 wait states at 120 MHz
- Prefetch and Cache ON
- When the peripherals are enabled, HCLK = 120MHz, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$
- The typical values are obtained for $V_{DD}$ = 3.3 V and $T_A$= 25 °C, unless otherwise specified.

**Table 26. Peripheral current consumption**

| Peripheral[(1)] | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| AHB1 | GPIO A | 0.45 | mA |
| | GPIO B | 0.43 | |
| | GPIO C | 0.46 | |
| | GPIO D | 0.44 | |
| | GPIO E | 0.44 | |
| | GPIO F | 0.42 | |
| | GPIO G | 0.44 | |
| | GPIO H | 0.42 | |
| | GPIO I | 0.43 | |
| | OTG_HS + ULPI | 3.64 | |
| | CRC | 1.17 | |
| | BKPSRAM | 0.21 | |
| | DMA1 | 2.76 | |
| | DMA2 | 2.85 | |
| | ETH_MAC +<br>ETH_MAC_TX<br>ETH_MAC_RX<br>ETH_MAC_PTP | 2.99 | |
| AHB2 | OTG_FS | 3.16 | |
| | DCMI | 0.60 | |
| AHB3 | FSMC | 1.74 | |

**Figure 41. $I^2C$ bus AC waveforms and measurement circuit**




1. $R_S$= series protection resistor.
2. $R_P$ = external pull-up resistor.
3. $V_{DD\_I2C}$ is the $I^2C$ bus power supply.

**Table 53. SCL frequency ($f_{PCLK1}$= 30 MHz.,$V_{DD}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = $I^2C$ speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

**Figure 49. Ethernet SMI timing diagram**

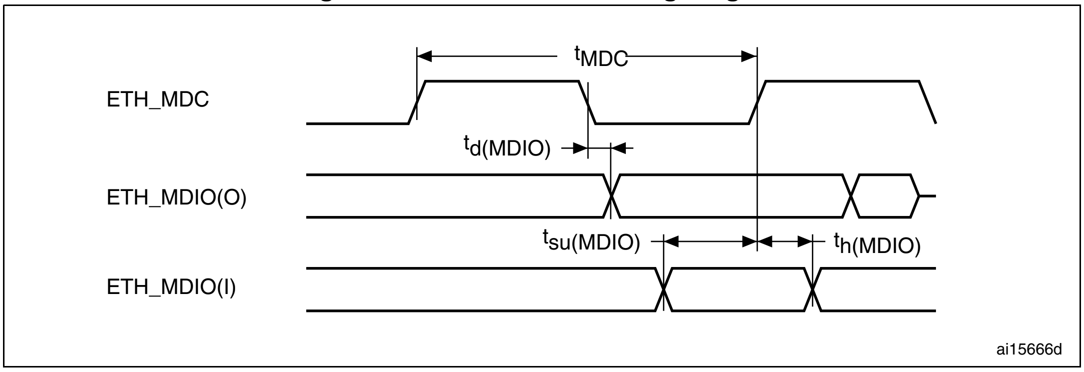



**Table 63. Dynamics characteristics: Ethernet MAC signals for SMI**

| Symbol | Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{MDC}$ | MDC cycle time (2.38 MHz) | 411 | 420 | 425 | ns |
| $t_{d(MDIO)}$ | MDIO write data valid time | 6 | 10 | 13 | ns |
| $t_{su(MDIO)}$ | Read data setup time | 12 | - | - | ns |
| $t_{h(MDIO)}$ | Read data hold time | 0 | - | - | ns |

*Table 64* gives the list of Ethernet MAC signals for the RMII and *Figure 50* shows the corresponding timing diagram.

**Figure 50. Ethernet RMII timing diagram**

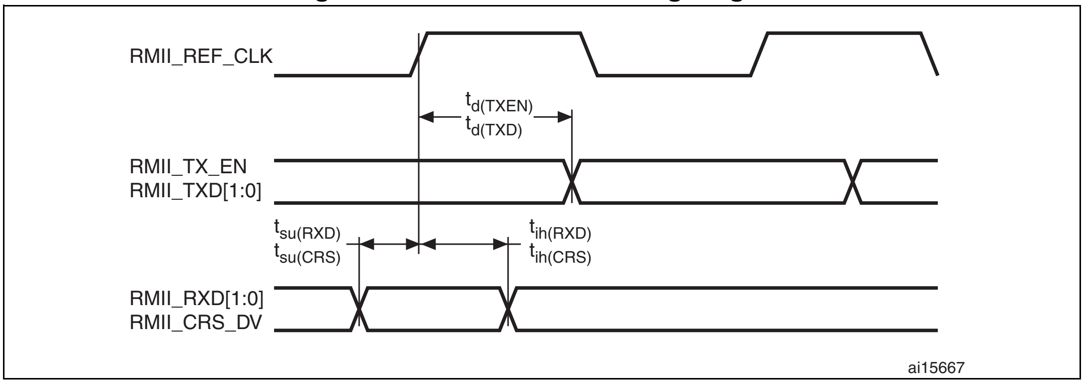


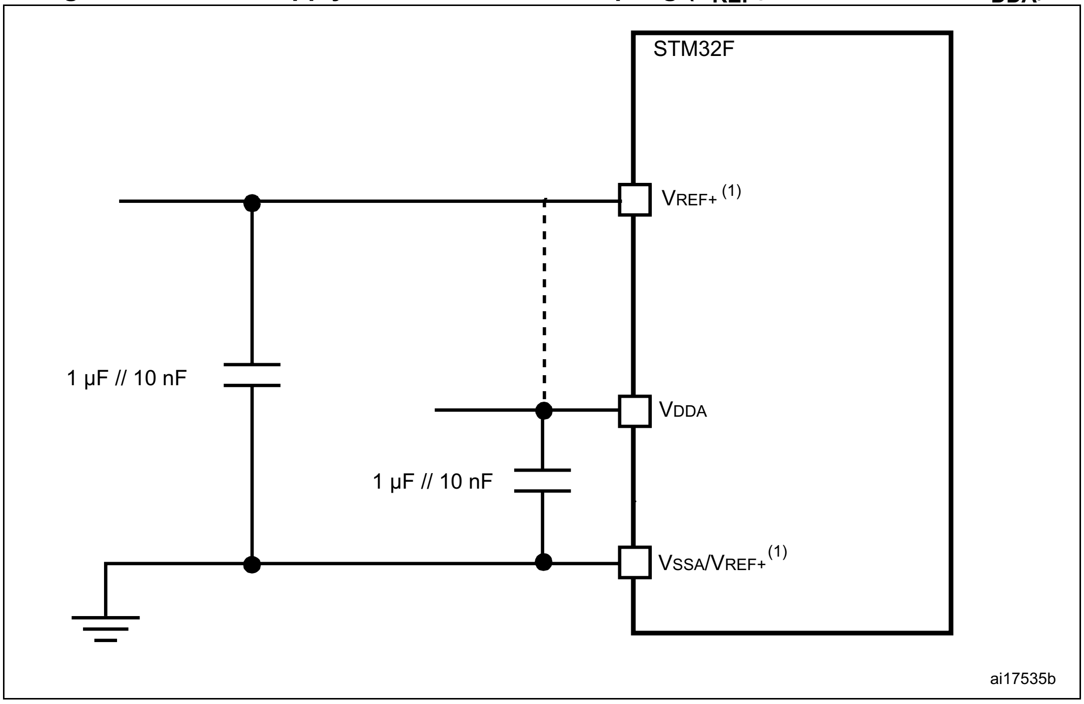

**Table 64. Dynamics characteristics: Ethernet MAC signals for RMII**

| Symbol | Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Receive data setup time | 1 | - | - | ns |
| $t_{ih(RXD)}$ | Receive data hold time | 1.5 | - | - | |
| $t_{su(CRS)}$ | Carrier sense set-up time | 0 | - | - | |
| $t_{ih(CRS)}$ | Carrier sense hold time | 2 | - | - | |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 9 | 11 | 13 | |
| $t_{d(TXD)}$ | Transmit data valid delay time | 9 | 11.5 | 14 | |

### General PCB design guidelines

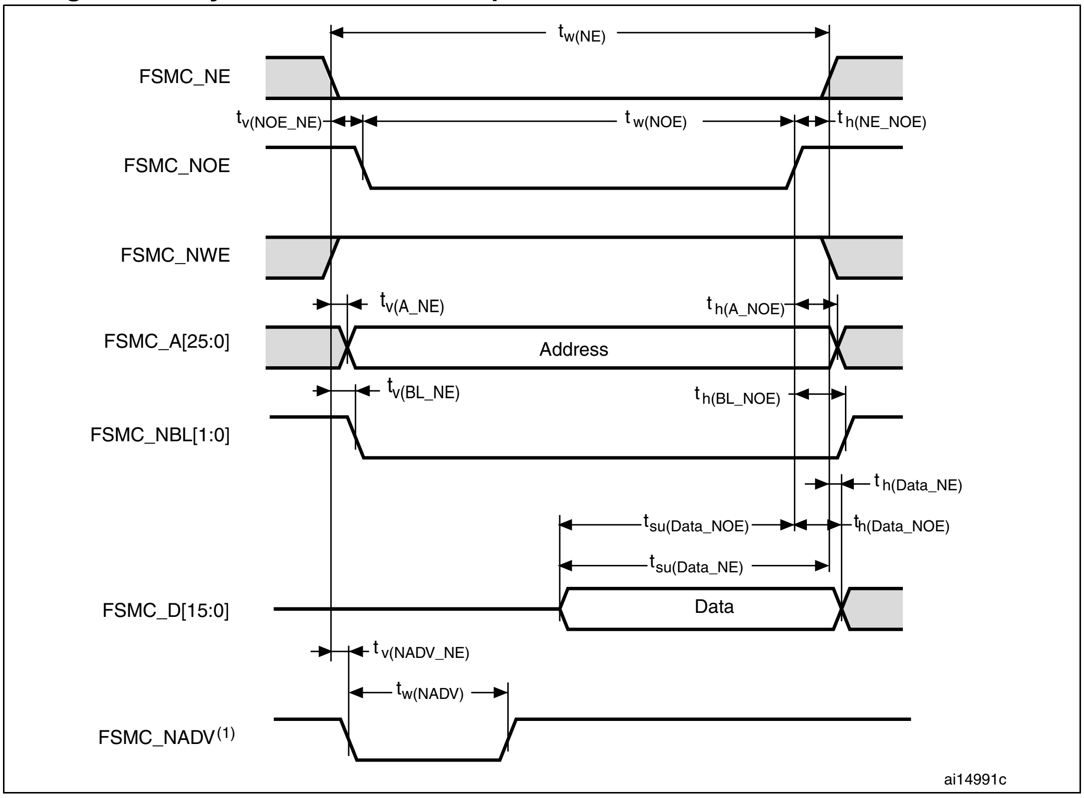
Power supply decoupling should be performed as shown in *Figure 54* or *Figure 55*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 54. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. $V_{REF+}$ and $V_{REF-}$ inputs are both available on UFBGA176 package. $V_{REF+}$ is also available on all packages except for LQFP64. When $V_{REF+}$ and $V_{REF-}$ are not available, they are internally connected to $V_{DDA}$ and $V_{SSA}$.

**Figure 57. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $2T_{HCLK} - 0.5$ | $2T_{HCLK} + 0.5$ | ns |
| $t_{v(NOE\_NE)}$ | FSMC_NEx low to FSMC_NOE low | 0.5 | 2.5 | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $2T_{HCLK} - 1$ | $2T_{HCLK} + 0.5$ | ns |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 4 | ns |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | 0 | - | ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | ns |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | - | ns |
| $t_{su(Data\_NE)}$ | Data to FSMC_NEx high setup time | $T_{HCLK} + 0.5$ | - | ns |
| $t_{su(Data\_NOE)}$ | Data to FSMC_NOEx high setup time | $T_{HCLK} + 2.5$ | - | ns |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | ns |
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 2.5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $T_{HCLK} - 0.5$ | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 73. NAND controller waveforms for common memory read access

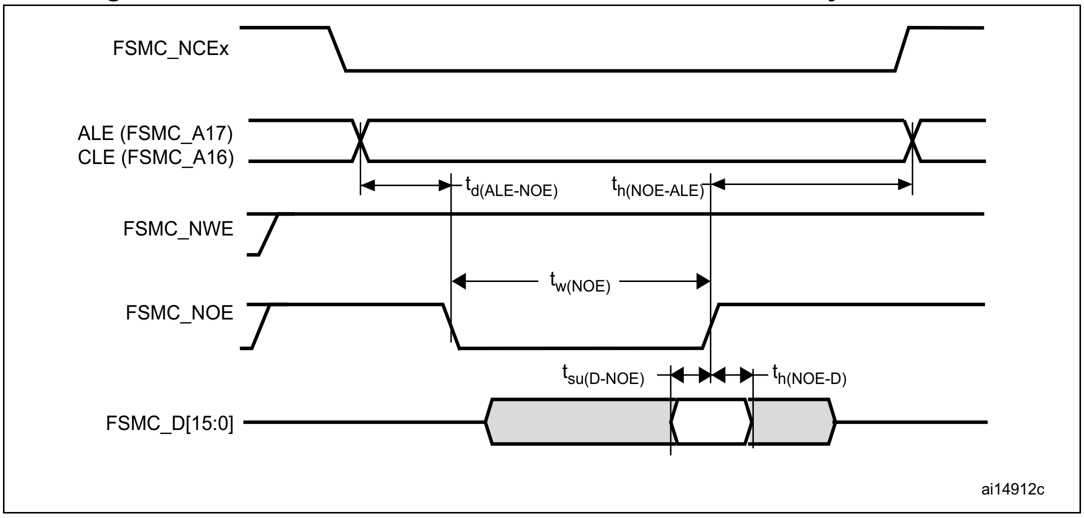



Figure 74. NAND controller waveforms for common memory write access

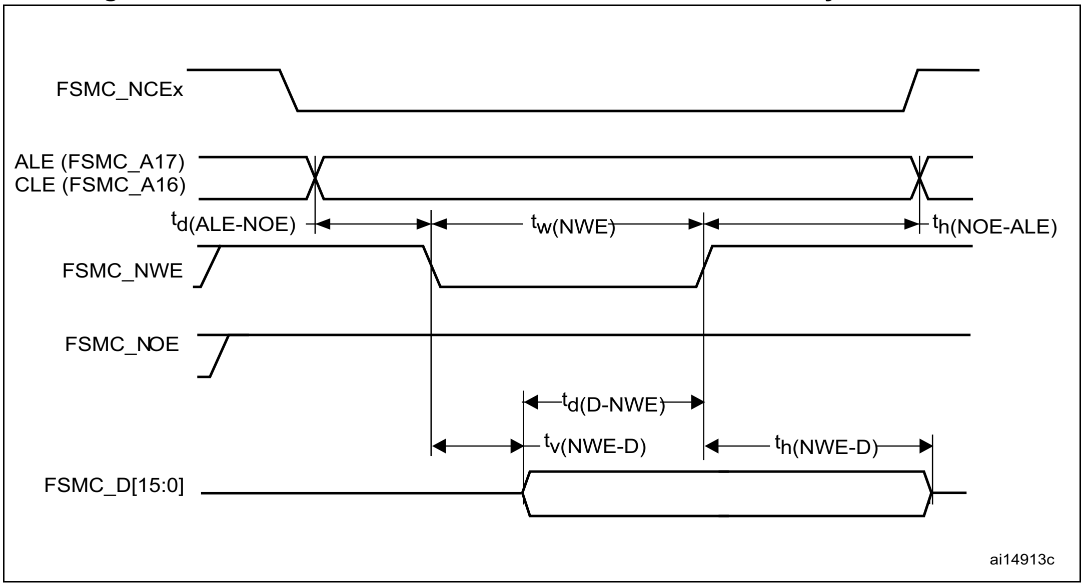


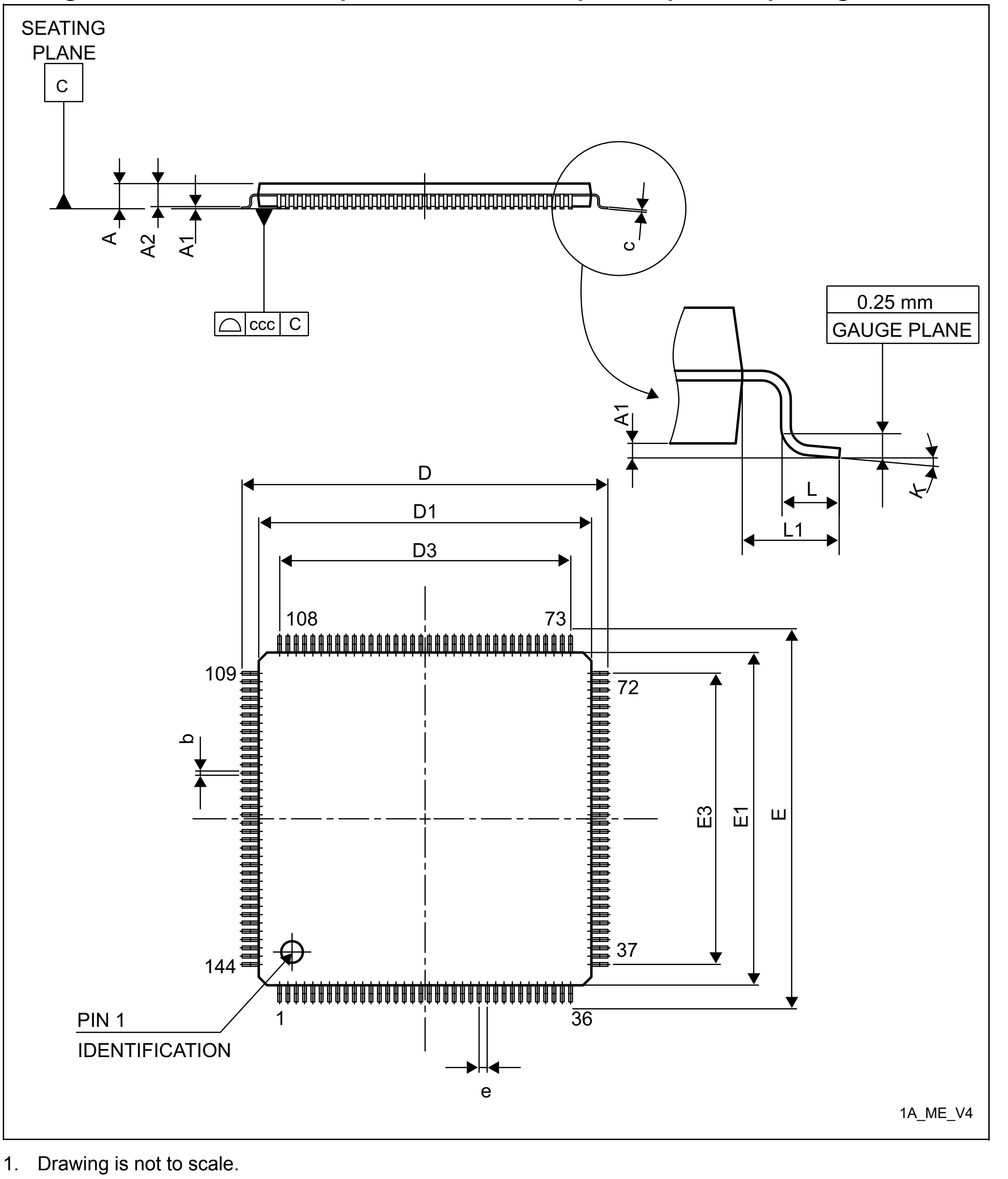

Table 82. Switching characteristics for NAND Flash read cycles(1)(2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(N0E)}$ | FSMC_NOE low width | $4T_{HCLK} - 1$ | $4T_{HCLK} + 2$ | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15-0] valid data before FSMC_NOE high | 9 | - | ns |
| $t_{h(NOE-D)}$ | FSMC_D[15-0] valid data after FSMC_NOE high | 3 | - | ns |
| $t_{d(ALE-NOE)}$ | FSMC_ALE valid before FSMC_NOE low | - | $3T_{HCLK}$ | ns |
| $t_{h(NOE-ALE)}$ | FSMC_NWE high to FSMC_ALE invalid | $3T_{HCLK} + 2$ | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

## 7.4 LQFP144 package information

**Figure 84. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline**




1. Drawing is not to scale.

Table 91. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.6890 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

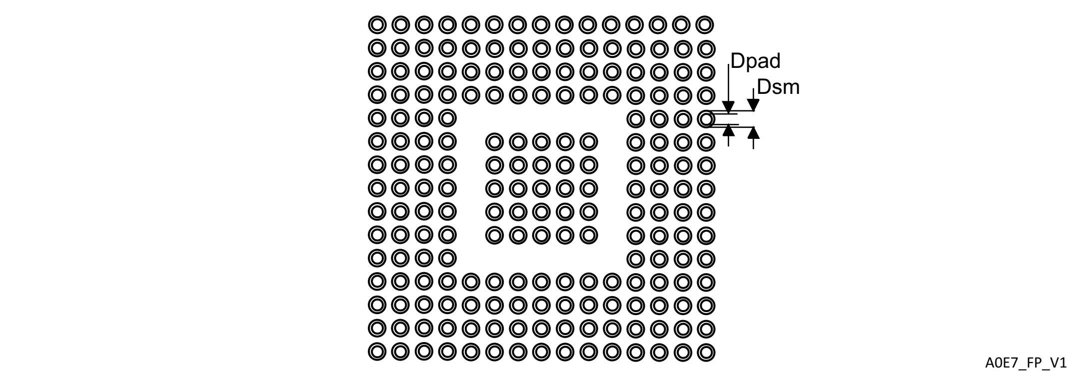



Table 94. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

| Dimension | Recommended values |
|---|---|
| Pitch | 0.65 mm |
| Dpad | 0.300 mm |
| Dsm | 0.400 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.300 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |

Table 97. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 24-Apr-2012 | 9 (continued) | Removed support of I2C for OTG PHY in *Section 3.29: Universal serial bus on-the-go high-speed (OTG_HS)*.<br>Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in *Table 8: STM32F20x pin and ball definitions* and *Table 10: Alternate function mapping*.<br>Renamed PH10 alternate function into TIM5_CH1 in *Table 10: Alternate function mapping*.<br>Added *Table 9: FSMC pin definition*.<br>Updated *Note 1* in *Table 14: General operating conditions*, *Note 2* in *Table 15: Limitations depending on the operating power supply range*, and *Note 1* below *Figure 21: Number of wait states versus fCPU and VDD range*.<br>Updated $V_{POR/PDR}$ in *Table 19: Embedded reset and power control block characteristics*.<br>Updated typical values in *Table 24: Typical and maximum current consumptions in Standby mode* and *Table 25: Typical and maximum current consumptions in VBAT mode*.<br>Updated *Table 30: HSE 4-26 MHz oscillator characteristics* and *Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)*.<br>Updated *Table 37: Flash memory characteristics*, *Table 38: Flash memory programming*, and *Table 39: Flash memory programming with VPP*.<br>Updated *Section : Output driving current*.<br>Updated *Note 3* and removed note related to minimum hold time value in *Table 52: I2C characteristics*.<br>Updated *Table 64: Dynamics characteristics: Ethernet MAC signals for RMII*.<br>Updated *Note 1*, $C_{ADC}$, $I_{VREF+}$, and $I_{VDDA}$ in *Table 66: ADC characteristics*.<br>Updated *Note 3* and note concerning ADC accuracy vs. negative injection current in *Table 67: ADC accuracy*.<br>Updated *Note 1* in *Table 68: DAC characteristics*.<br>Updated *Section Figure 88.: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*.<br>Appendix *A.1: Main applications versus package*: removed number of address lines for FSMC/NAND in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*.<br>Appendix *A.4: Ethernet interface solutions*: updated *Figure 92: Complete audio player solution 1* and *Figure 93: Complete audio player solution 2*. |