



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f205zgt6j

6.1.7	Current consumption measurement	70
6.2	Absolute maximum ratings	70
6.3	Operating conditions	71
6.3.1	General operating conditions	71
6.3.2	VCAP1/VCAP2 external capacitor	74
6.3.3	Operating conditions at power-up / power-down (regulator ON)	75
6.3.4	Operating conditions at power-up / power-down (regulator OFF)	75
6.3.5	Embedded reset and power control block characteristics	76
6.3.6	Supply current characteristics	77
6.3.7	Wakeup time from low-power mode	88
6.3.8	External clock source characteristics	89
6.3.9	Internal clock source characteristics	92
6.3.10	PLL characteristics	94
6.3.11	PLL spread spectrum clock generation (SSCG) characteristics	97
6.3.12	Memory characteristics	98
6.3.13	EMC characteristics	100
6.3.14	Absolute maximum ratings (electrical sensitivity)	102
6.3.15	I/O current injection characteristics	103
6.3.16	I/O port characteristics	104
6.3.17	NRST pin characteristics	109
6.3.18	TIM timer characteristics	110
6.3.19	Communications interfaces	111
6.3.20	12-bit ADC characteristics	124
6.3.21	DAC electrical characteristics	128
6.3.22	Temperature sensor characteristics	130
6.3.23	V _{BAT} monitoring characteristics	131
6.3.24	Embedded reference voltage	131
6.3.25	FSMC characteristics	131
6.3.26	Camera interface (DCMI) timing specifications	149
6.3.27	SD/SDIO MMC card host interface (SDIO) characteristics	149
6.3.28	RTC characteristics	150
7	Package information	151
7.1	LQFP64 package information	151
7.2	WLCSP64+2 package information	153
7.3	LQFP100 package information	155

	7.4	LQFP144 package information	158
	7.5	LQFP176 package information	162
	7.6	UFBGA176+25 package information	165
	7.7	Thermal characteristics	167
8		Part numbering	168
9		Revision history	169

Table 93.	UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data	165
Table 94.	UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)	166
Table 95.	Package thermal characteristics	167
Table 96.	Ordering information scheme	168
Table 97.	Document revision history	169

List of figures

Figure 1.	Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package.	17
Figure 2.	Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package.	18
Figure 3.	Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package.	18
Figure 4.	STM32F20x block diagram.	19
Figure 5.	Multi-AHB matrix.	22
Figure 6.	Regulator OFF/internal reset ON.	27
Figure 7.	Regulator OFF/internal reset OFF.	28
Figure 8.	Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization.	29
Figure 9.	Startup in regulator OFF: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization.	29
Figure 10.	STM32F20x LQFP64 pinout.	41
Figure 11.	STM32F20x WLCSP64+2 ballout.	41
Figure 12.	STM32F20x LQFP100 pinout.	42
Figure 13.	STM32F20x LQFP144 pinout.	43
Figure 14.	STM32F20x LQFP176 pinout.	44
Figure 15.	STM32F20x UFBGA176 ballout.	45
Figure 16.	Memory map.	67
Figure 17.	Pin loading conditions.	68
Figure 18.	Pin input voltage.	68
Figure 19.	Power supply scheme.	69
Figure 20.	Current consumption measurement scheme.	70
Figure 21.	Number of wait states versus f_{CPU} and V_{DD} range.	74
Figure 22.	External capacitor C_{EXT}	74
Figure 23.	Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals ON.	80
Figure 24.	Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals OFF.	80
Figure 25.	Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON.	81
Figure 26.	Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals OFF.	81
Figure 27.	Typical current consumption vs. temperature in Sleep mode, peripherals ON.	83
Figure 28.	Typical current consumption vs. temperature in Sleep mode, peripherals OFF.	83
Figure 29.	Typical current consumption vs. temperature in Stop mode.	84
Figure 30.	High-speed external clock source AC timing diagram.	90
Figure 31.	Low-speed external clock source AC timing diagram.	90
Figure 32.	Typical application with an 8 MHz crystal.	91
Figure 33.	Typical application with a 32.768 kHz crystal.	92
Figure 34.	ACC_{HSI} versus temperature.	93
Figure 35.	ACC_{LSI} versus temperature.	94
Figure 36.	PLL output clock waveforms in center spread mode.	98
Figure 37.	PLL output clock waveforms in down spread mode.	98

**Table 3. STM32F207xx features and peripheral counts (continued)**

Peripherals		STM32F207Vx	STM32F207Zx	STM32F207Ix
Comm. interfaces	SPI/(I ² S)	3/(2) ⁽²⁾		
	I ² C	3		
	USART UART	4 2		
	USB OTG FS	Yes		
	USB OTG HS	Yes		
	CAN	2		
Camera interface		Yes		
GPIOs		82	114	140
SDIO		Yes		
12-bit ADC Number of channels		3		
		16	24	24
12-bit DAC Number of channels		Yes		
		2		
Maximum CPU frequency		120 MHz		
Operating voltage		1.8 V to 3.6 V ⁽³⁾		
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C		
		Junction temperature: –40 to + 125 °C		
Package		LQFP100	LQFP144	LQFP176/ UFBGA176

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	56	78	97	P14	PD9	I/O	FT	-	FSMC_D14, USART3_RX, EVENTOUT	-
-	-	57	79	98	N15	PD10	I/O	FT	-	FSMC_D15, USART3_CK, EVENTOUT	-
-	-	58	80	99	N14	PD11	I/O	FT	-	FSMC_A16, USART3_CTS, EVENTOUT	-
-	-	59	81	100	N13	PD12	I/O	FT	-	FSMC_A17, TIM4_CH1, USART3_RTS, EVENTOUT	-
-	-	60	82	101	M15	PD13	I/O	FT	-	FSMC_A18, TIM4_CH2, EVENTOUT	-
-	-	-	83	102	-	V _{SS}	S	-	-	-	-
-	-	-	84	103	J13	V _{DD}	S	-	-	-	-
-	-	61	85	104	M14	PD14	I/O	FT	-	FSMC_D0, TIM4_CH3, EVENTOUT	-
-	-	62	86	105	L14	PD15	I/O	FT	-	FSMC_D1, TIM4_CH4, EVENTOUT	-
-	-	-	87	106	L15	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	88	107	K15	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	89	108	K14	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	90	109	K13	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	91	110	J15	PG6	I/O	FT	-	FSMC_INT2, EVENTOUT	-
-	-	-	92	111	J14	PG7	I/O	FT	-	FSMC_INT3, USART6_CK, EVENTOUT	-
-	-	-	93	112	H14	PG8	I/O	FT	-	USART6_RTS, ETH_PPS_OUT, EVENTOUT	-
-	-	-	94	113	G12	V _{SS}	S	-	-	-	-
-	-	-	95	114	H13	V _{DD}	S	-	-	-	-
37	G2	63	96	115	H15	PC6	I/O	FT	-	I2S2_MCK, TIM8_CH1, SDIO_D6, USART6_TX, DCMI_D0, TIM3_CH1, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	-	130	D13	PH15	I/O	FT	-	TIM8_CH3N, DCMI_D11, EVENTOUT	-
-	-	-	-	131	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS, I2S2_WS, DCMI_D13, EVENTOUT	-
-	-	-	-	132	D14	PI1	I/O	FT	-	SPI2_SCK, I2S2_SCK, DCMI_D8, EVENTOUT	-
-	-	-	-	133	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, DCMI_D9, EVENTOUT	-
-	-	-	-	134	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI, I2S2_SD, DCMI_D10, EVENTOUT	-
-	-	-	-	135	D9	V _{SS}	S	-	-	-	-
-	-	-	-	136	C9	V _{DD}	S	-	-	-	-
49	A1	76	109	137	A14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	A2	77	110	138	A13	PA15 (JTDI)	I/O	FT	-	JTDI, SPI3_NSS, I2S3_WS, TIM2_CH1_ETR, SPI1_NSS, EVENTOUT	-
51	B3	78	111	139	B14	PC10	I/O	FT	-	SPI3_SCK, I2S3_SCK, UART4_TX, SDIO_D2, DCMI_D8, USART3_TX, EVENTOUT	-
52	C3	79	112	140	B13	PC11	I/O	FT	-	UART4_RX, SPI3_MISO, SDIO_D3, DCMI_D4, USART3_RX, EVENTOUT	-
53	A3	80	113	141	A12	PC12	I/O	FT	-	UART5_TX, SDIO_CK, DCMI_D9, SPI3_MOSI, I2S3_SD, USART3_CK, EVENTOUT	-
-	-	81	114	142	B12	PD0	I/O	FT	-	FSMC_D2, CAN1_RX, EVENTOUT	-
-	-	82	115	143	C12	PD1	I/O	FT	-	FSMC_D3, CAN1_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
54	C7	83	116	144	D12	PD2	I/O	FT	-	TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	-	84	117	145	D11	PD3	I/O	FT	-	FSMC_CLK, USART2_CTS, EVENTOUT	-
-	-	85	118	146	D10	PD4	I/O	FT	-	FSMC_NOE, USART2_RTS, EVENTOUT	-
-	-	86	119	147	C11	PD5	I/O	FT	-	FSMC_NWE, USART2_TX, EVENTOUT	-
-	-	-	120	148	D8	V _{SS}	S	-	-	-	-
-	-	-	121	149	C8	V _{DD}	S	-	-	-	-
-	-	87	122	150	B11	PD6	I/O	FT	-	FSMC_NWAIT, USART2_RX, EVENTOUT	-
-	-	88	123	151	A11	PD7	I/O	FT	-	USART2_CK, FSMC_NE1, FSMC_NCE2, EVENTOUT	-
-	-	-	124	152	C10	PG9	I/O	FT	-	USART6_RX, FSMC_NE2, FSMC_NCE3, EVENTOUT	-
-	-	-	125	153	B10	PG10	I/O	FT	-	FSMC_NCE4_1, FSMC_NE3, EVENTOUT	-
-	-	-	126	154	B9	PG11	I/O	FT	-	FSMC_NCE4_2, ETH_MII_TX_EN, ETH_RMII_TX_EN, EVENTOUT	-
-	-	-	127	155	B8	PG12	I/O	FT	-	FSMC_NE4, USART6_RTS, EVENTOUT	-
-	-	-	128	156	A8	PG13	I/O	FT	-	FSMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-
-	-	-	129	157	A7	PG14	I/O	FT	-	FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT	-
-	-	-	130	158	D7	V _{SS}	S	-	-	-	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	98	142	170	A3	PE1	I/O	FT	-	FSMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	D5	V _{SS}	S	-	-	-	-
63	D8	-	-	-	-	V _{SS}	S	-	-	-	-
-	-	99	143	171	C6	RFU	-	-	(7)	-	-
64	D9	100	144	172	C5	V _{DD}	S	-	-	-	-
-	-	-	-	173	D4	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5, EVENTOUT	-
-	-	-	-	174	C4	PI5	I/O	FT	-	TIM8_CH1, DCMI_VSYNC, EVENTOUT	-
-	-	-	-	175	C3	PI6	I/O	FT	-	TIM8_CH2, DCMI_D6, EVENTOUT	-
-	-	-	-	176	C2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	C8	-	-	-	-	IRROFF	I/O	-	-	-	-

1. Function availability depends on the chosen device.

2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).

3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F20x and STM32F21x reference manual, available from the STMicroelectronics website: www.st.com.

4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

5. If the device is delivered in an UFBGA176 package and if the REGOFF pin is set to V_{DD} (Regulator OFF), then PA0 is used as an internal Reset (active low).

6. FSMC_NL pin is also named FSMC_NADV on memory devices.

7. RFU means "reserved for future use". This pin can be tied to V_{DD}, V_{SS} or left unconnected.

Table 9. FSMC pin definition

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	A23	A23	-	Yes
PE3	-	A19	A19	-	Yes
PE4	-	A20	A20	-	Yes



Table 10. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port A	PA0-WKUP	-	TIM2_CH1_ETR	TIM5_CH1	TIM8_ETR	-	-		USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-		USART2_RTS	UART4_RX	-	-	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-		USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-		USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	-	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-		-	OTG_HS_SOF	DCMI_HSYNC	-	EVENTOUT
	PA5	-	TIM2_CH1_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-		-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1 TIM2_ETR	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-	-	-	-	-	-	-	-

Table 22. Typical and maximum current consumption in Sleep mode

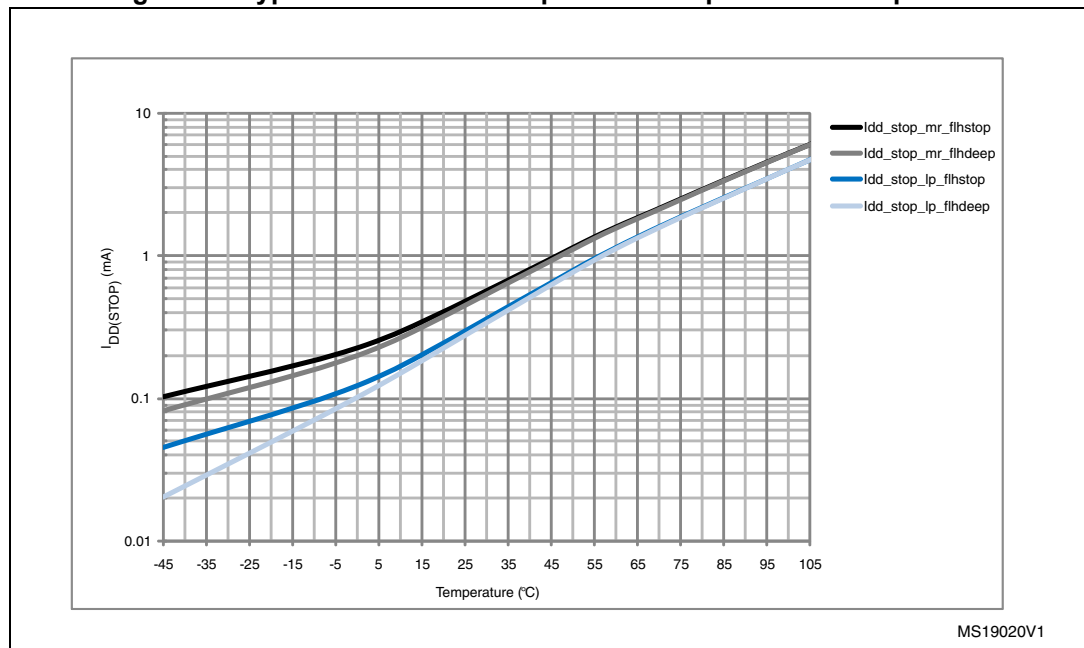
Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max ⁽¹⁾		Unit
				$T_A = 25\text{ °C}$	$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
I_{DD}	Supply current in Sleep mode	External clock ⁽²⁾ , all peripherals enabled ⁽³⁾	120 MHz	38	51	61	mA
			90 MHz	30	43	53	
			60 MHz	20	33	43	
			30 MHz	11	25	35	
			25 MHz	8	21	31	
			16 MHz	6	19	29	
			8 MHz	3.6	17.0	27.0	
			4 MHz	2.4	15.4	25.3	
			2 MHz	1.9	14.9	24.7	
		External clock ⁽²⁾ , all peripherals disabled	120 MHz	8	21	31	
			90 MHz	7	20	30	
			60 MHz	5	18	28	
			30 MHz	3.5	16.0	26.0	
			25 MHz	2.5	16.0	25.0	
			16 MHz	2.1	15.1	25.0	
			8 MHz	1.7	15.0	25.0	
			4 MHz	1.5	14.6	24.6	
			2 MHz	1.4	14.2	24.3	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK} > 25$ MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max				Unit
			T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C		
I _{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	mA	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00		
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00		
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00		

Figure 29. Typical current consumption vs. temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Table 37. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD}	Supply current	Write / Erase 8-bit mode V _{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode V _{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode V _{DD} = 3.3 V	-	12	-	

Table 38. Flash memory programming

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100 ⁽²⁾	μs
t _{ERASE16KB}	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
t _{ERASE64KB}	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
t _{ERASE128KB}	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t _{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V _{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.

2. The maximum programming time is measured after 100K erase operations.

Table 47. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS ports $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL ports $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
$V_{OL}^{(2)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-1.3$	-	
$V_{OL}^{(2)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	

- PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
- The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
- The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
- Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

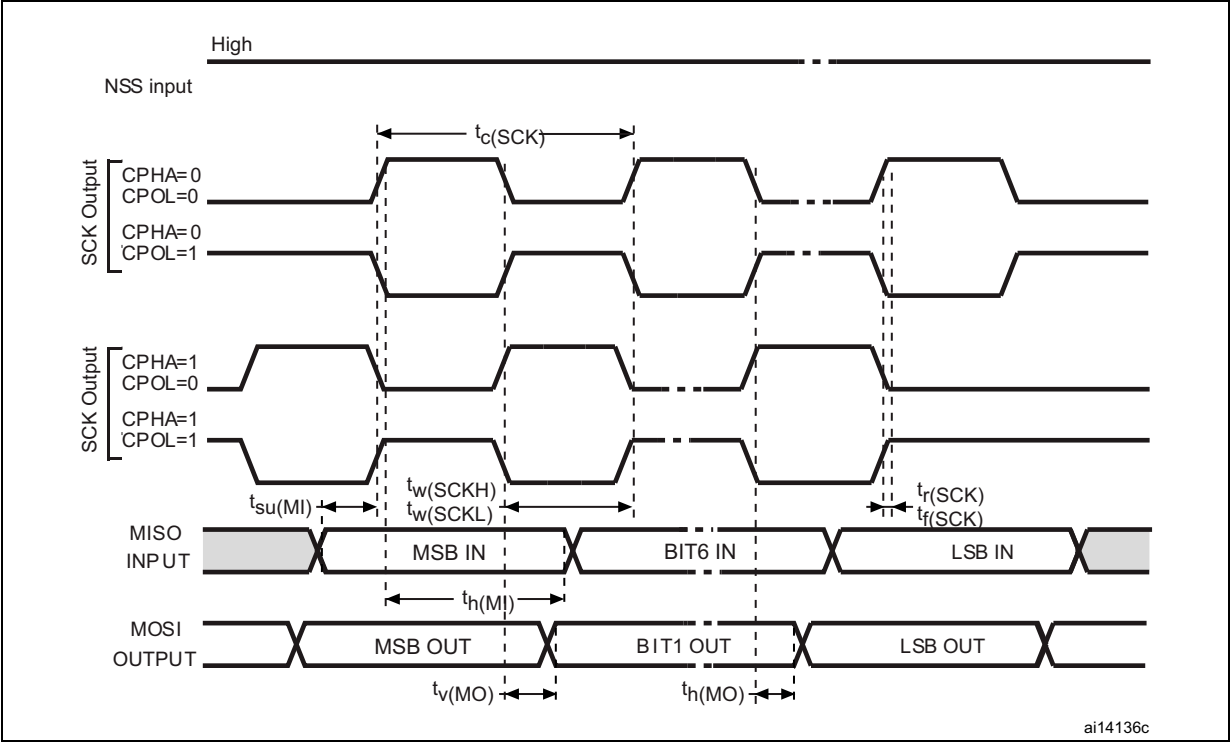
The definition and values of input/output AC characteristics are given in [Figure 39](#) and [Table 48](#), respectively.

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 48. I/O AC characteristics⁽¹⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(I/O)out}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	4	
	$t_{f(I/O)out}/$ $t_{r(I/O)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.8 \text{ V to}$ 3.6 V	-	-	100	ns

Figure 44. SPI timing diagram - master mode



6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 66](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 14](#).

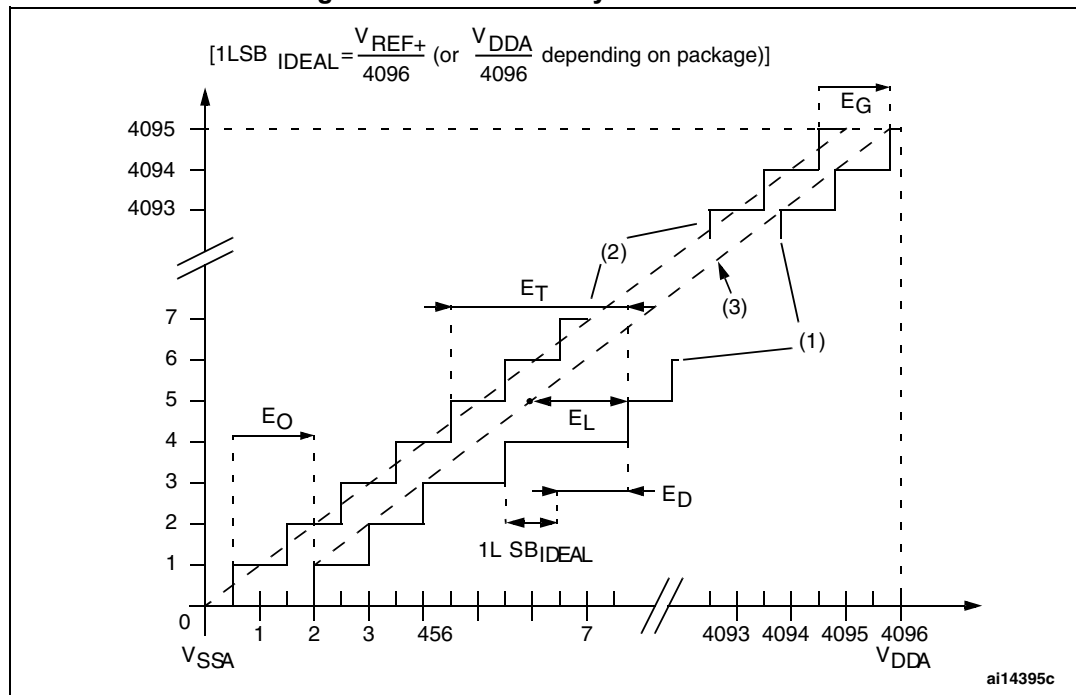
Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8 ⁽¹⁾	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8 ⁽¹⁾⁽²⁾	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	$V_{DDA} = 1.8^{(1)}$ to 2.4 V	0.6	-	15	MHz
		$V_{DDA} = 2.4$ to 3.6 V	0.6	-	30	MHz
$f_{TRIG}^{(3)}$	External trigger frequency	$f_{ADC} = 30$ MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	1/ f_{ADC}
V_{AIN}	Conversion voltage range ⁽⁴⁾	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(3)}$	External input impedance	See Equation 1 for details	-	-	50	k Ω
$R_{ADC}^{(3)(5)}$	Sampling switch resistance	-	1.5	-	6	k Ω
$C_{ADC}^{(3)}$	Internal sample and hold capacitor	-	-	4	-	pF
$t_{lat}^{(3)}$	Injection trigger conversion latency	$f_{ADC} = 30$ MHz	-	-	0.100	μ s
		-	-	-	3 ⁽⁶⁾	1/ f_{ADC}
$t_{latr}^{(3)}$	Regular trigger conversion latency	$f_{ADC} = 30$ MHz	-	-	0.067	μ s
		-	-	-	2 ⁽⁶⁾	1/ f_{ADC}
$t_S^{(3)}$	Sampling time	$f_{ADC} = 30$ MHz	0.100	-	16	μ s
		-	3	-	480	1/ f_{ADC}
$t_{STAB}^{(3)}$	Power-up time	-	-	2	3	μ s
$t_{CONV}^{(3)}$	Total conversion time (including sampling time)	$f_{ADC} = 30$ MHz 12-bit resolution	0.5	-	16.40	μ s
		$f_{ADC} = 30$ MHz 10-bit resolution	0.43	-	16.34	μ s
		$f_{ADC} = 30$ MHz 8-bit resolution	0.37	-	16.27	μ s
		$f_{ADC} = 30$ MHz 6-bit resolution	0.3	-	16.20	μ s
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				1/ f_{ADC}

being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

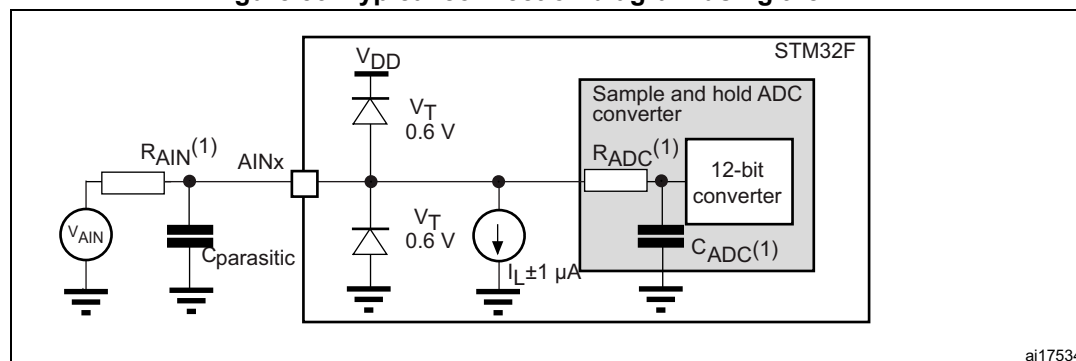
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.16](#) does not affect the ADC accuracy.

Figure 52. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset Error: deviation between the first actual transition and the first ideal one.
 E_G = Gain Error: deviation between the last ideal transition and the last actual one.
 E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
 E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 53. Typical connection diagram using the ADC



1. Refer to [Table 66](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

**Table 91. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 97. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	10 (continued)	Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in Table 76: Synchronous multiplexed NOR/PSRAM read timings, Table 78: Synchronous non-multiplexed NOR/PSRAM read timings, Figure 61: Synchronous multiplexed NOR/PSRAM read timings and Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings. Added Figure 87: LQFP176 recommended footprint. Added Note 2 below Figure 86: Regulator OFF/internal reset ON. Updated device subfamily in Table 96: Ordering information scheme. Remove reference to note 2 for USB IOTG FS in Table 101: Main applications versus package for STM32F2xxx microcontrollers.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved