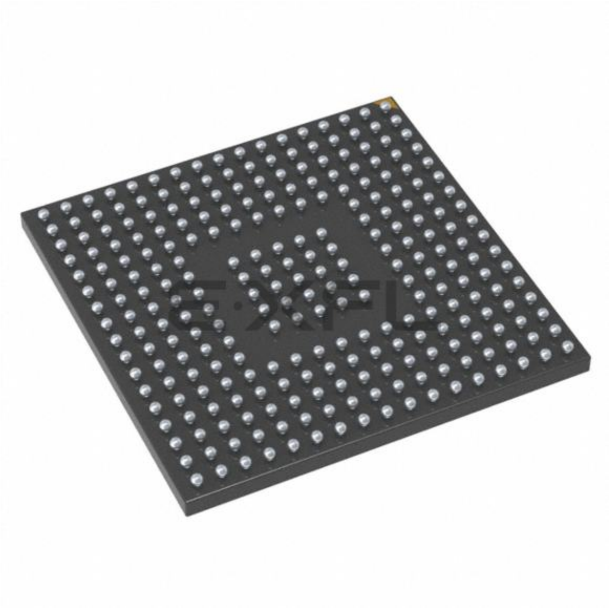


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207ich6

List of tables

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes
  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
  The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS}. On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

Table 8. STM32F20x pin and ball definitions

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	1	1	1	A2	PE2	I/O	FT	-	TRACECLK, FSMC_A23, ETH_MII_TXD3, EVENTOUT	-
-	-	2	2	2	A1	PE3	I/O	FT	-	TRACED0,FSMC_A19, EVENTOUT	-
-	-	3	3	3	B1	PE4	I/O	FT	-	TRACED1,FSMC_A20, DCMI_D4, EVENTOUT	-
-	-	4	4	4	B2	PE5	I/O	FT	-	TRACED2, FSMC_A21, TIM9_CH1, DCMI_D6, EVENTOUT	-
-	-	5	5	5	B3	PE6	I/O	FT	-	TRACED3, FSMC_A22, TIM9_CH2, DCMI_D7, EVENTOUT	-
1	A9	6	6	6	C1	V_{BAT}	S		-	-	-
-	-	-	-	7	D2	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_AF2
2	B8	7	7	8	D1	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1
3	B9	8	8	9	E1	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN(4)
4	C9	9	9	10	F1	PC15-OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT(4)
-	-	-	-	11	D3	PI9	I/O	FT	-	CAN1_RX,EVENTOUT	-
-	-	-	-	12	E3	PI10	I/O	FT	-	ETH_MII_RX_ER, EVENTOUT	-
-	-	-	-	13	E4	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	-	-	14	F2	V_{SS}	S		-	-	-
-	-	-	-	15	F3	V_{DD}	S		-	-	-
-	-	-	10	16	E2	PF0	I/O	FT	-	FSMC_A0, I2C2_SDA, EVENTOUT	-
-	-	-	11	17	H3	PF1	I/O	FT	-	FSMC_A1, I2C2_SCL, EVENTOUT	-
-	-	-	12	18	H2	PF2	I/O	FT	-	FSMC_A2, I2C2_SMBA, EVENTOUT	-
-	-	-	13	19	J2	PF3	I/O	FT	(4)	FSMC_A3, EVENTOUT	ADC3_IN9

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
38	F2	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	-
39	F3	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3,SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	D1	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	E2	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	E3	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	D3	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID,DCMI_D1, EVENTOUT	-
44	D2	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4,OTG_FS_DM, EVENTOUT	-
45	C1	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	B2	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	C2	73	106	125	F13	V_{CAP_2}	S	-	-	-	-
-	B1	74	107	126	F12	V_{SS}	S	-	-	-	-
48	A8	75	108	127	G13	V_{DD}	S	-	-	-	-
-	-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176	Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	98	142	170	A3	PE1	I/O	FT	-	FSMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	D5	V_{SS}	S	-	-	-	-
63	D8	-	-	-	-	V_{SS}	S	-	-	-	-
-	-	99	143	171	C6	RFU	-	-	(7)	-	-
64	D9	100	144	172	C5	V_{DD}	S	-	-	-	-
-	-	-	-	173	D4	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5, EVENTOUT	-
-	-	-	-	174	C4	PI5	I/O	FT	-	TIM8_CH1, DCMI_VSYNC, EVENTOUT	-
-	-	-	-	175	C3	PI6	I/O	FT	-	TIM8_CH2, DCMI_D6, EVENTOUT	-
-	-	-	-	176	C2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	C8	-	-	-	-	IRROFF	I/O	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F20x and STM32F21x reference manual, available from the STMicroelectronics website: www.st.com.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA176 package and if the REGOFF pin is set to V_{DD} (Regulator OFF), then PA0 is used as an internal Reset (active low).
6. FSMC_NL pin is also named FSMC_NADV on memory devices.
7. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.

Table 9. FSMC pin definition

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	A23	A23	-	Yes
PE3	-	A19	A19	-	Yes
PE4	-	A20	A20	-	Yes

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator and RTC ON	3.0	3.4	4.0	15.1	25.8	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	2.4	2.7	3.3	12.4	20.5	
		Backup SRAM ON, RTC OFF	2.4	2.6	3.0	12.5	24.8	
		Backup SRAM OFF, RTC OFF	1.7	1.9	2.2	9.8	19.2	

1. Guaranteed by characterization results, not tested in production.

Table 25. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	12	19	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	8	10	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	9	16	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	5	7	

1. Guaranteed by characterization results, not tested in production.

Table 30. HSE 4-26 MHz oscillator characteristics(1) (2)

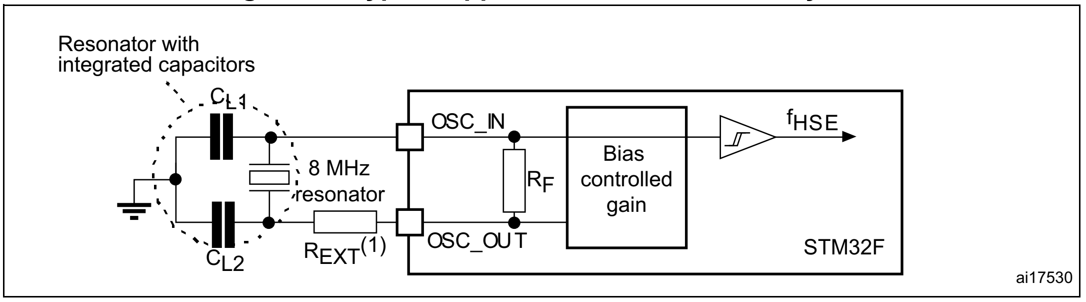
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, ESR= 30 Ω, C_L=5 pF@25 MHz	-	449	-	µA
		V_{DD}=3.3 V, ESR= 30 Ω, C_L=10 pF@25 MHz	-	532	-	
g_m	Oscillator transconductance	Startup	5	-	-	mA/V
$t_{SU(HSE}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results, not tested in production.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 32*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 32. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 34. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results, not tested in production.

Table 35. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-	0.95(2)	1	2.10(2)	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-	-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output	-	192	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-2	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 47. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS ports I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL ports I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL} (2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL} (2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 48. I/O AC characteristics(1)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns

Table 48. I/O AC characteristics(1) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-3	6	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100(3)	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	120(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. The maximum frequency is defined in *Figure 39*.
3. For maximum frequencies above 50 MHz and V_{DD} above 2.4 V, the compensation cell should be used.

I²S - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 54* for SPI or in *Table 55* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 54. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	SPI1 master/slave mode	-	30	MHz
		SPI2/SPI3 master/slave mode	-	15	
$t_{r(SCL)}$ $t_{f(SCL)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF, f_{PCLK} = 30 MHz	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLH)}$ (1) $t_{w(SCLL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 30 MHz, presc = 2	t_{PCLK}-3	t_{PCLK}+3	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	5	-	
		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 30 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

1. Guaranteed by characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Table 66. ADC characteristics

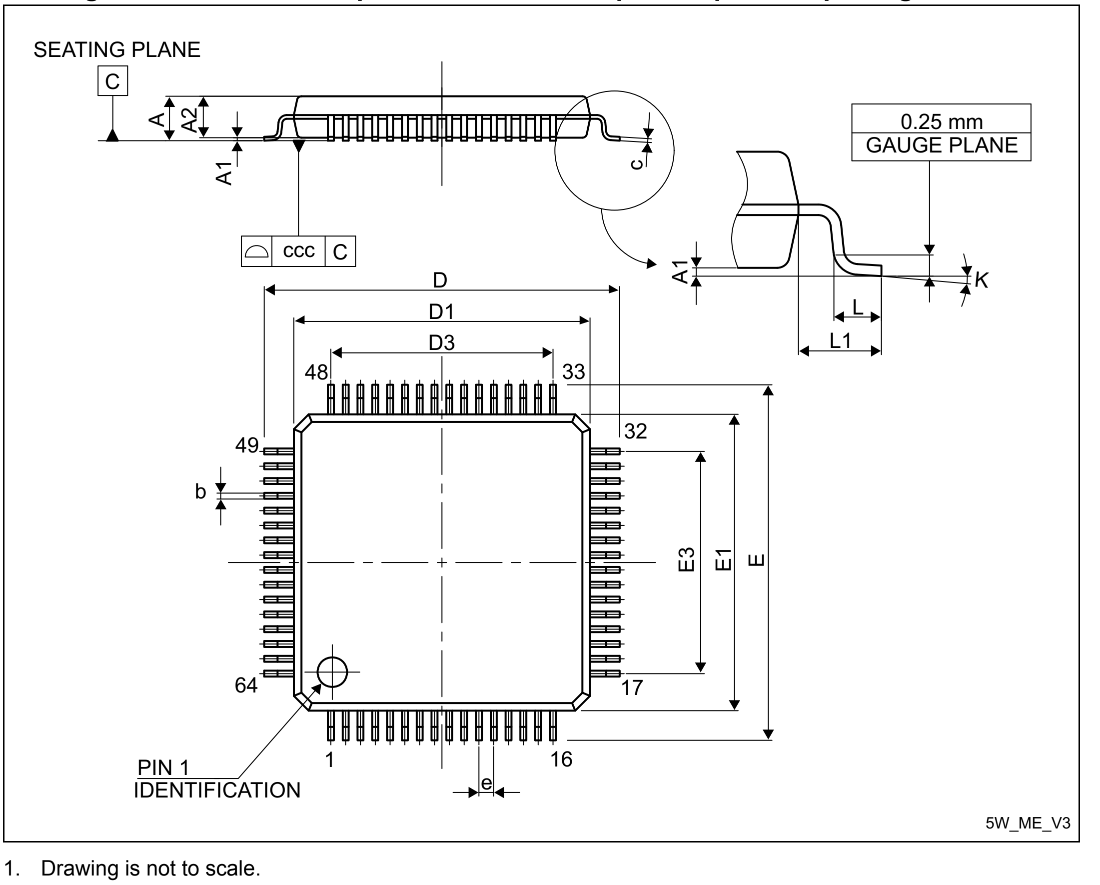
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	$1.8^{(1)}$	-	3.6	V
V_{REF+}	Positive reference voltage	-	$1.8^{(1)(2)}$	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	$V_{DDA} = 1.8^{(1)}$ to 2.4 V	0.6	-	15	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	-	30	MHz
$f_{TRIG}^{(3)}$	External trigger frequency	f_{ADC} = 30 MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range$^{(4)}$	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(3)}$	External input impedance	See *Equation 1* for details	-	-	50	kΩ
$R_{ADC}^{(3)(5)}$	Sampling switch resistance	-	1.5	-	6	kΩ
$C_{ADC}^{(3)}$	Internal sample and hold capacitor	-	-	4	-	pF
$t_{lat}^{(3)}$	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	$3^{(6)}$	$1/f_{ADC}$
$t_{latr}^{(3)}$	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	$2^{(6)}$	$1/f_{ADC}$
$t_S^{(3)}$	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
$t_{STAB}^{(3)}$	Power-up time	-	-	2	3	µs
$t_{CONV}^{(3)}$	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.5	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.3	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

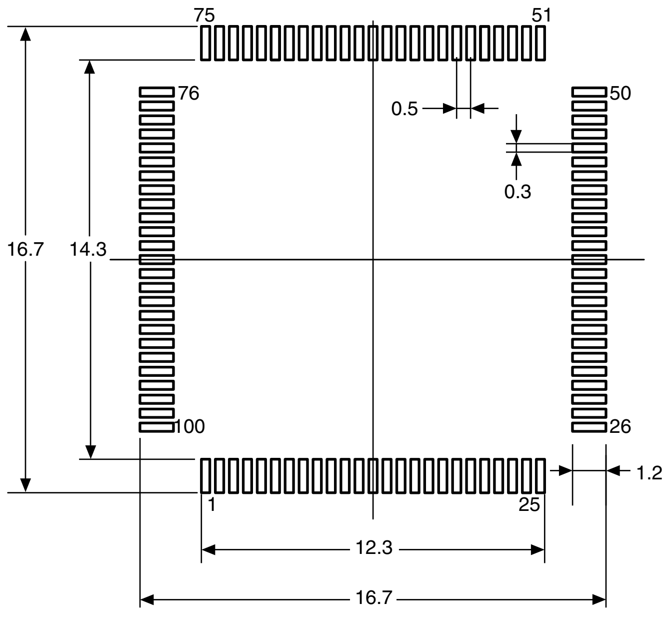
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 90. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

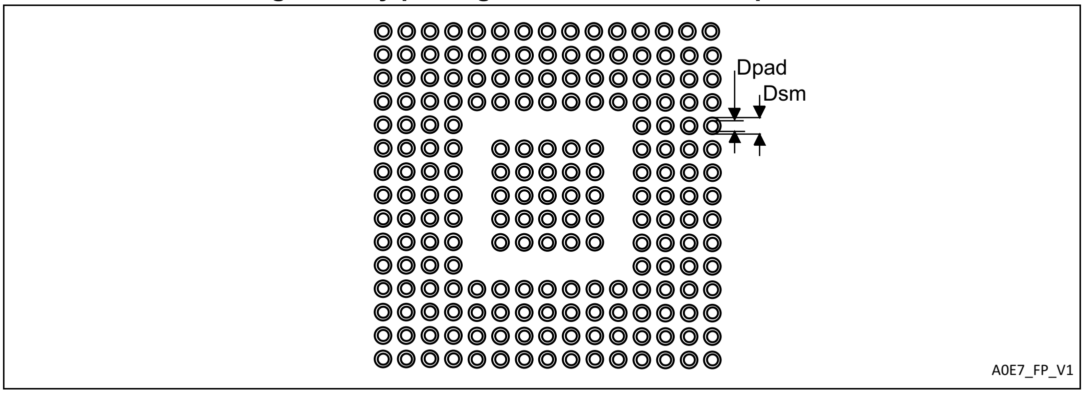


Table 94. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Table 97. Document revision history (continued)

Date	Revision	Changes
25-Nov-2010	5	Update I/Os in *Section : Features*. Added WLCSP64+2 package. Added note 1 related to LQFP176 on cover page. Added trademark for ART accelerator. Updated *Section 3.2: Adaptive real-time memory accelerator (ART Accelerator™)*. Updated *Figure 5: Multi-AHB matrix*. Added case of BOR inactivation using IRROFF on WLCSP devices in *Section 3.15: Power supply supervisor*. Reworked *Section 3.16: Voltage regulator* to clarify regulator off modes. Renamed PDROFF, IRROFF in the whole document. Added *Section 3.19: VBAT operation*. Updated LIN and IrDA features for UART4/5 in *Table 6: USART feature comparison*. *Table 8: STM32F20x pin and ball definitions*: Modified V_{DD_3} pin, and added note related to the FSMC_NL pin; renamed BYPASS-REG REGOFF, and add IRROFF pin; renamed USART4/5 UART4/5. USART4 pins renamed UART4. Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use. Updated maximum HSE crystal frequency to 26 MHz. *Section 6.2: Absolute maximum ratings*: Updated V_{IN} minimum and maximum values and note related to five-volt tolerant inputs in *Table 11: Voltage characteristics*. Updated $I_{INJ(PIN)}$ maximum values and related notes in *Table 12: Current characteristics*. Updated V_{DDA} minimum value in *Table 14: General operating conditions*. Added Note 2 and updated Maximum CPU frequency in *Table 15: Limitations depending on the operating power supply range*, and added *Figure 21: Number of wait states versus fCPU and VDD range*. Added brownout level 1, 2, and 3 thresholds in *Table 19: Embedded reset and power control block characteristics*. Changed f_{OSC_IN} maximum value in *Table 30: HSE 4-26 MHz oscillator characteristics*. Changed f_{PLL_IN} maximum value in *Table 34: Main PLL characteristics*, and updated jitter parameters in *Table 35: PLLI2S (audio PLL) characteristics*. *Section 6.3.16: I/O port characteristics*: updated V_{IH} and V_{IL} in *Table 48: I/O AC characteristics*. Added *Note 1* below *Table 47: Output voltage characteristics*. Updated R_{PD} and R_{PU} parameter description in *Table 57: USB OTG FS DC electrical characteristics*. Updated V_{REF+} minimum value in *Table 66: ADC characteristics*. Updated *Table 71: Embedded internal reference voltage*. Removed Ethernet and USB2 for 64-pin devices in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Added *A.2: USB OTG full speed (FS) interface solutions*, removed “OTG FS connection with external PHY” figure, updated *Figure 87*, *Figure 88*, and *Figure 90* to add STULPI01B.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in *Table 52: I2C characteristics* and in *Figure 41: I2C bus AC waveforms and measurement circuit*. Added *Table 57: USB OTG FS DC electrical characteristics* and updated *Table 58: USB OTG FS electrical characteristics*. Updated V_{DD} minimum value in *Table 62: Ethernet DC electrical characteristics*. Updated *Table 66: ADC characteristics* and R_{AIN} equation. Updated R_{AIN} equation. Updated *Table 68: DAC characteristics*. Updated t_{START} in *Table 69: Temperature sensor characteristics*. Updated R typical value in *Table 70: VBAT monitoring characteristics*. Updated *Table 71: Embedded internal reference voltage*. Modified FSMC_NOE waveform in *Figure 57: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms*. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in *Figure 61: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 62: Synchronous multiplexed PSRAM write timings*, *Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Figure 64: Synchronous non-multiplexed PSRAM write timings*, Changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Updated note 2 in *Table 72*, *Table 73*, *Table 74*, *Table 75*, *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Modified $t_{h(NIOWR-D)}$ in *Figure 70: PC Card/CompactFlash controller waveforms for I/O space write access*. Modified FSMC_NCEx signal in *Figure 71: NAND controller waveforms for read access*, *Figure 72: NAND controller waveforms for write access*, *Figure 73: NAND controller waveforms for common memory read access*, and *Figure 74: NAND controller waveforms for common memory write access* Specified Full speed (FS) mode for *Figure 89: USB OTG HS peripheral-only connection in FS mode* and *Figure 90: USB OTG HS host-only connection in FS mode*.