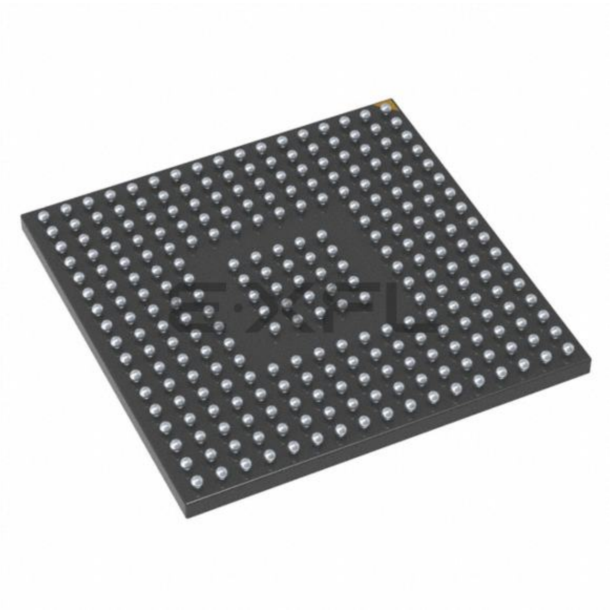
STMicroelectronics - STM32F207IEH6TR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207ieh6tr

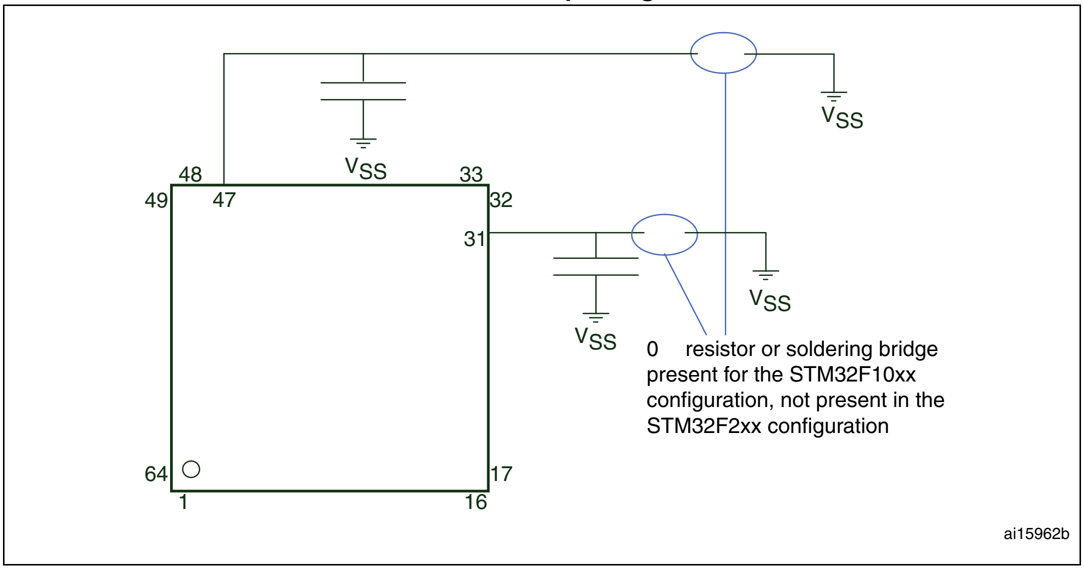
2.1 Full compatibility throughout the family

The STM32F205xx and STM32F207xx constitute the STM32F20x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F205xx and STM32F207xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F205xx and STM32F207xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F20x family remains simple as only a few pins are impacted.

Figure 1, *Figure 2* and *Figure 3* provide compatible board designs between the STM32F20x and the STM32F10xxx family.

Figure 1. Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package



3.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All STM32F20x products embed:

- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.
The counter can be frozen in debug mode.

3.20.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.21 Inter-integrated circuit interface (I²C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

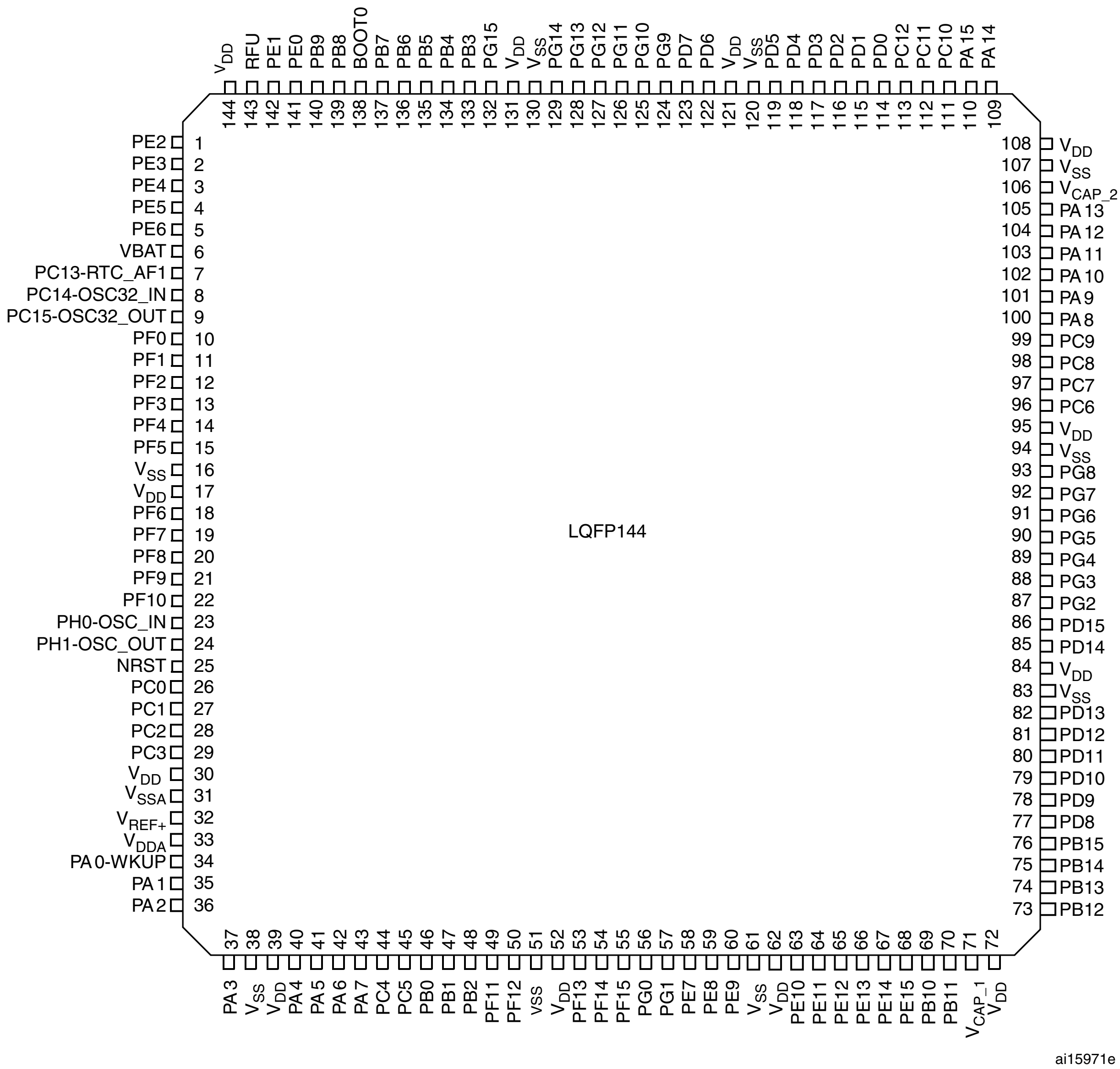
3.22 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F20x devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Figure 13. STM32F20x LQFP144 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
22	H5	31	42	52	P3	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6
23	J7	32	43	53	R3	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
24	H4	33	44	54	N5	PC4	I/O	FT	(4)	ETH_RMII_RXD0, ETH_MII_RXD0, EVENTOUT	ADC12_IN14
25	G3	34	45	55	P5	PC5	I/O	FT	(4)	ETH_RMII_RXD1, ETH_MII_RXD1, EVENTOUT	ADC12_IN15
26	J6	35	46	56	R5	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
27	J5	36	47	57	R4	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
28	J4	37	48	58	M6	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	49	59	R6	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	50	60	P6	PF12	I/O	FT	-	FSMC_A6, EVENTOUT	-
-	-	-	51	61	M8	V_{SS}	S		-	-	-
-	-	-	52	62	N8	V_{DD}	S		-	-	-
-	-	-	53	63	N6	PF13	I/O	FT	-	FSMC_A7, EVENTOUT	-
-	-	-	54	64	R7	PF14	I/O	FT	-	FSMC_A8, EVENTOUT	-
-	-	-	55	65	P7	PF15	I/O	FT	-	FSMC_A9, EVENTOUT	-
-	-	-	56	66	N7	PG0	I/O	FT	-	FSMC_A10, EVENTOUT	-
-	-	-	57	67	M7	PG1	I/O	FT	-	FSMC_A11, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	131	159	C7	V_{DD}	S	-	-	-	-
-	-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCMI_D13, EVENTOUT	-
55	A4	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/ TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	B4	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	A5	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT	-
58	B5	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL,, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT	-
59	A6	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL[6], DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	B6	94	138	166	D6	BOOT0	I	B	-	-	V_{PP}
61	B7	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	A7	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT	-

Table 9. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE5	-	A21	A21	-	Yes
PE6	-	A22	A22	-	Yes
PF0	A0	A0	-	-	-
PF1	A1	A1	-	-	-
PF2	A2	A2	-	-	-
PF3	A3	A3	-	-	-
PF4	A4	A4	-	-	-
PF5	A5	A5	-	-	-
PF6	NIORD	-	-	-	-
PF7	NREG	-	-	-	-
PF8	NIOWR	-	-	-	-
PF9	CD	-	-	-	-
PF10	INTR	-	-	-	-
PF12	A6	A6	-	-	-
PF13	A7	A7	-	-	-
PF14	A8	A8	-	-	-
PF15	A9	A9	-	-	-
PG0	A10	A10	-	-	-
PG1	-	A11	-	-	-
PE7	D4	D4	DA4	D4	Yes
PE8	D5	D5	DA5	D5	Yes
PE9	D6	D6	DA6	D6	Yes
PE10	D7	D7	DA7	D7	Yes
PE11	D8	D8	DA8	D8	Yes
PE12	D9	D9	DA9	D9	Yes
PE13	D10	D10	DA10	D10	Yes
PE14	D11	D11	DA11	D11	Yes
PE15	D12	D12	DA12	D12	Yes
PD8	D13	D13	DA13	D13	Yes
PD9	D14	D14	DA14	D14	Yes
PD10	D15	D15	DA15	D15	Yes
PD11	-	A16	A16	CLE	Yes
PD12	-	A17	A17	ALE	Yes

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH _MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	-	OTG_HS_ULPI_D2	ETH _MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_SCK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	-	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT	-	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NL	DCMI_VSYNC	-	EVENTOUT
Port B	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH _MII_TXD3	SDIO_D4	DCMI_D6	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_SCK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_ MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_SCK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	-	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_50Hz	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port C	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_ STP	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ULPI_ DIR	ETH _MII_TXD2	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI	-	-	-	-	OTG_HS_ULPI_ NXT	ETH _MII_TX_CLK	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_RXD1 ETH _RMII_RXD1	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	I2S3_CKIN	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK I2S3_SCK	USART3_TX	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	-	EVENTOUT
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14-OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15-OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)(1)	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(2)	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4(3)	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(3)	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

Figure 25. Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON

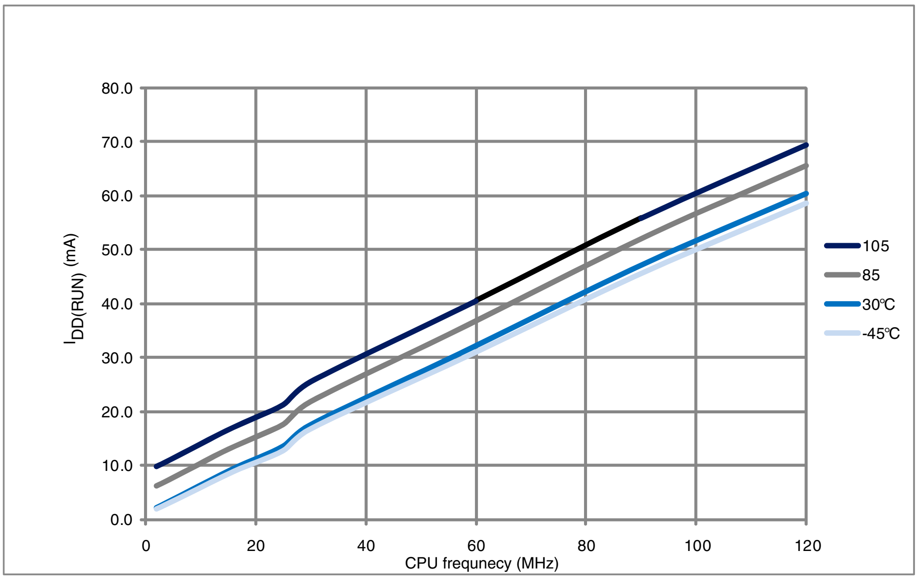


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Figure 26. Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals OFF

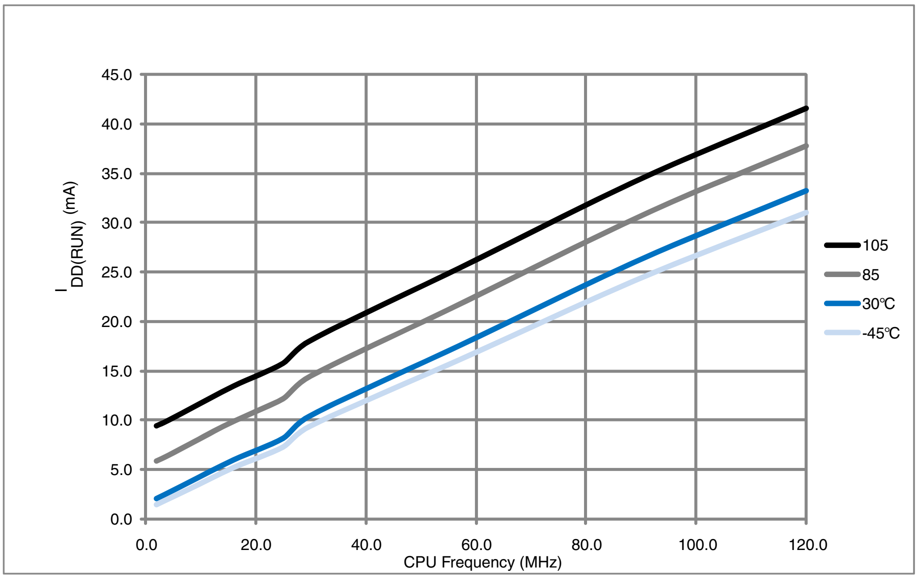

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Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator and RTC ON	3.0	3.4	4.0	15.1	25.8	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	2.4	2.7	3.3	12.4	20.5	
		Backup SRAM ON, RTC OFF	2.4	2.6	3.0	12.5	24.8	
		Backup SRAM OFF, RTC OFF	1.7	1.9	2.2	9.8	19.2	

1. Guaranteed by characterization results, not tested in production.

Table 25. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	12	19	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	8	10	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	9	16	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	5	7	

1. Guaranteed by characterization results, not tested in production.

Table 26. Peripheral current consumption (continued)

Peripheral(1)		Typical consumption at 25 °C	Unit
APB2	SDIO	0.69	mA
	TIM1	1.06	
	TIM8	1.03	
	TIM9	0.58	
	TIM10	0.37	
	TIM11	0.39	
	ADC1(4)	2.13	
	ADC2(4)	2.04	
	ADC3(4)	2.12	
	SPI1	1.20	
	USART1	0.38	
	USART6	0.37	

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC_CR register.
3. EN2 bit is set in DAC_CR register.
4. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

6.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	1	-	µs
t_{WUSTOP}(2)	Wakeup from Stop mode (regulator in Run mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

Table 39. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 40. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

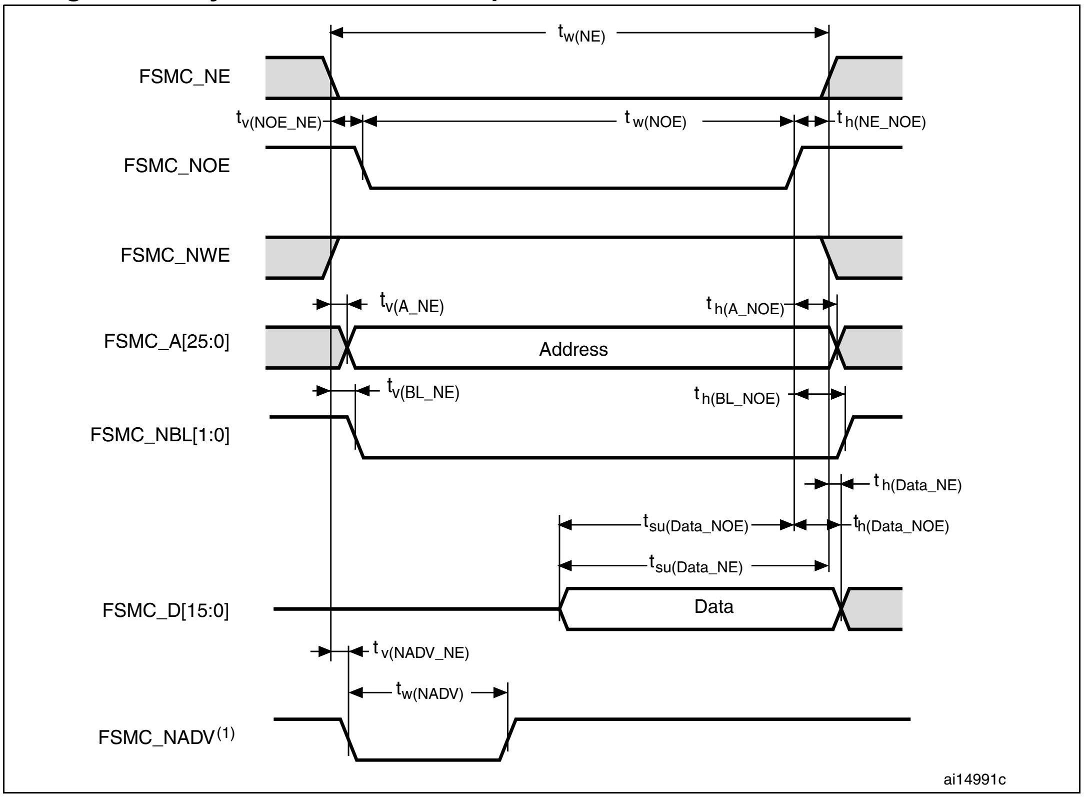
Table 46. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design, not tested in production.
2. Guaranteed by tests in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 45: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 45: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.

Figure 57. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2T_{HCLK}- 0.5$	$2T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	2.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$2T_{HCLK}- 1$	$2T_{HCLK}+ 0.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	4	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$T_{HCLK}+ 0.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$T_{HCLK}+ 2.5$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK}- 0.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Table 76. Synchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	5	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 62. Synchronous multiplexed PSRAM write timings

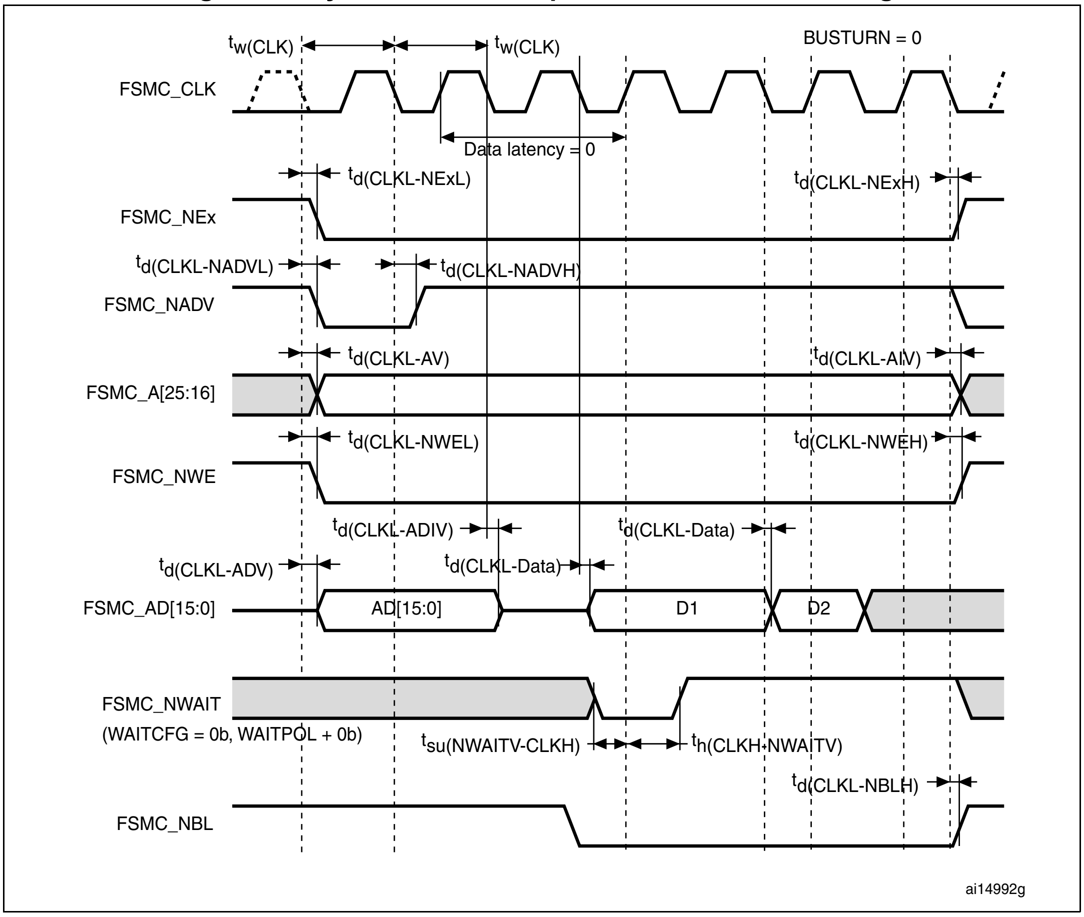
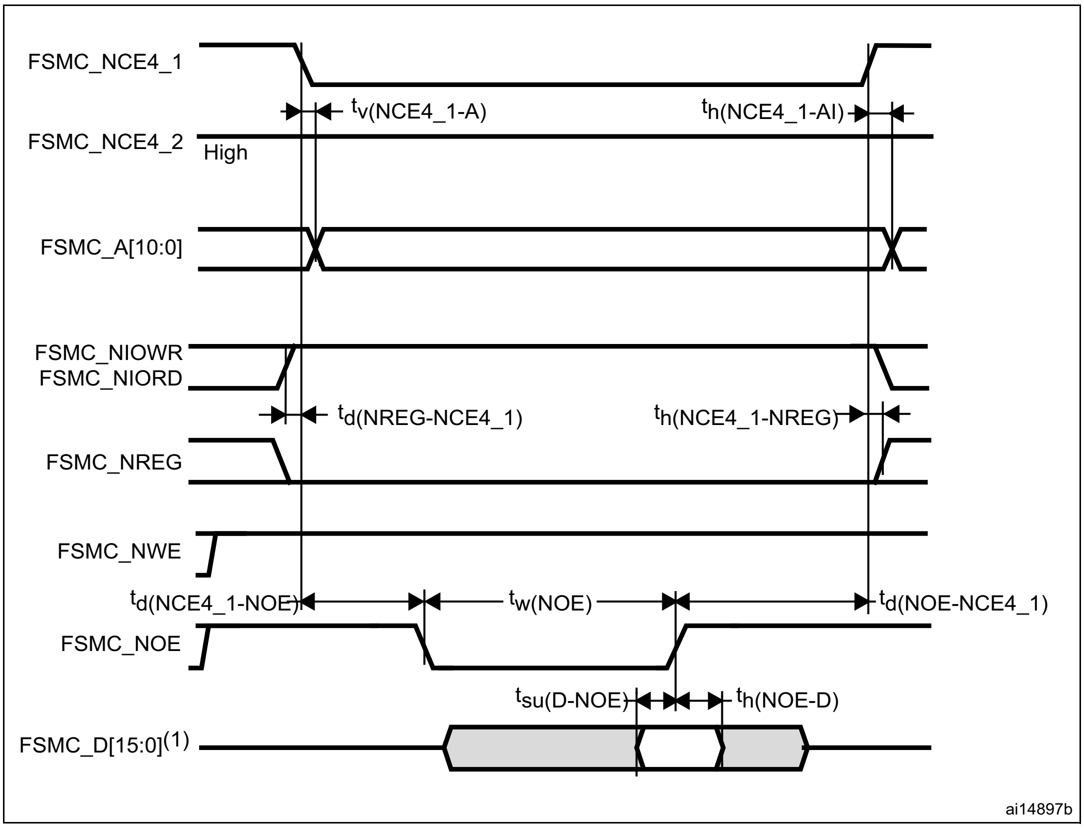


Table 77. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	7	-	ns

Figure 67. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 95. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch	51	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in *Table 52: I2C characteristics* and in *Figure 41: I2C bus AC waveforms and measurement circuit*. Added *Table 57: USB OTG FS DC electrical characteristics* and updated *Table 58: USB OTG FS electrical characteristics*. Updated V_{DD} minimum value in *Table 62: Ethernet DC electrical characteristics*. Updated *Table 66: ADC characteristics* and R_{AIN} equation. Updated R_{AIN} equation. Updated *Table 68: DAC characteristics*. Updated t_{START} in *Table 69: Temperature sensor characteristics*. Updated R typical value in *Table 70: VBAT monitoring characteristics*. Updated *Table 71: Embedded internal reference voltage*. Modified FSMC_NOE waveform in *Figure 57: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms*. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in *Figure 61: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 62: Synchronous multiplexed PSRAM write timings*, *Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Figure 64: Synchronous non-multiplexed PSRAM write timings*, Changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Updated note 2 in *Table 72*, *Table 73*, *Table 74*, *Table 75*, *Table 76*, *Table 77*, *Table 78*, and *Table 79*. Modified $t_{h(NIOWR-D)}$ in *Figure 70: PC Card/CompactFlash controller waveforms for I/O space write access*. Modified FSMC_NCEx signal in *Figure 71: NAND controller waveforms for read access*, *Figure 72: NAND controller waveforms for write access*, *Figure 73: NAND controller waveforms for common memory read access*, and *Figure 74: NAND controller waveforms for common memory write access* Specified Full speed (FS) mode for *Figure 89: USB OTG HS peripheral-only connection in FS mode* and *Figure 90: USB OTG HS host-only connection in FS mode*.