

**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 140 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 132K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207ift6 |

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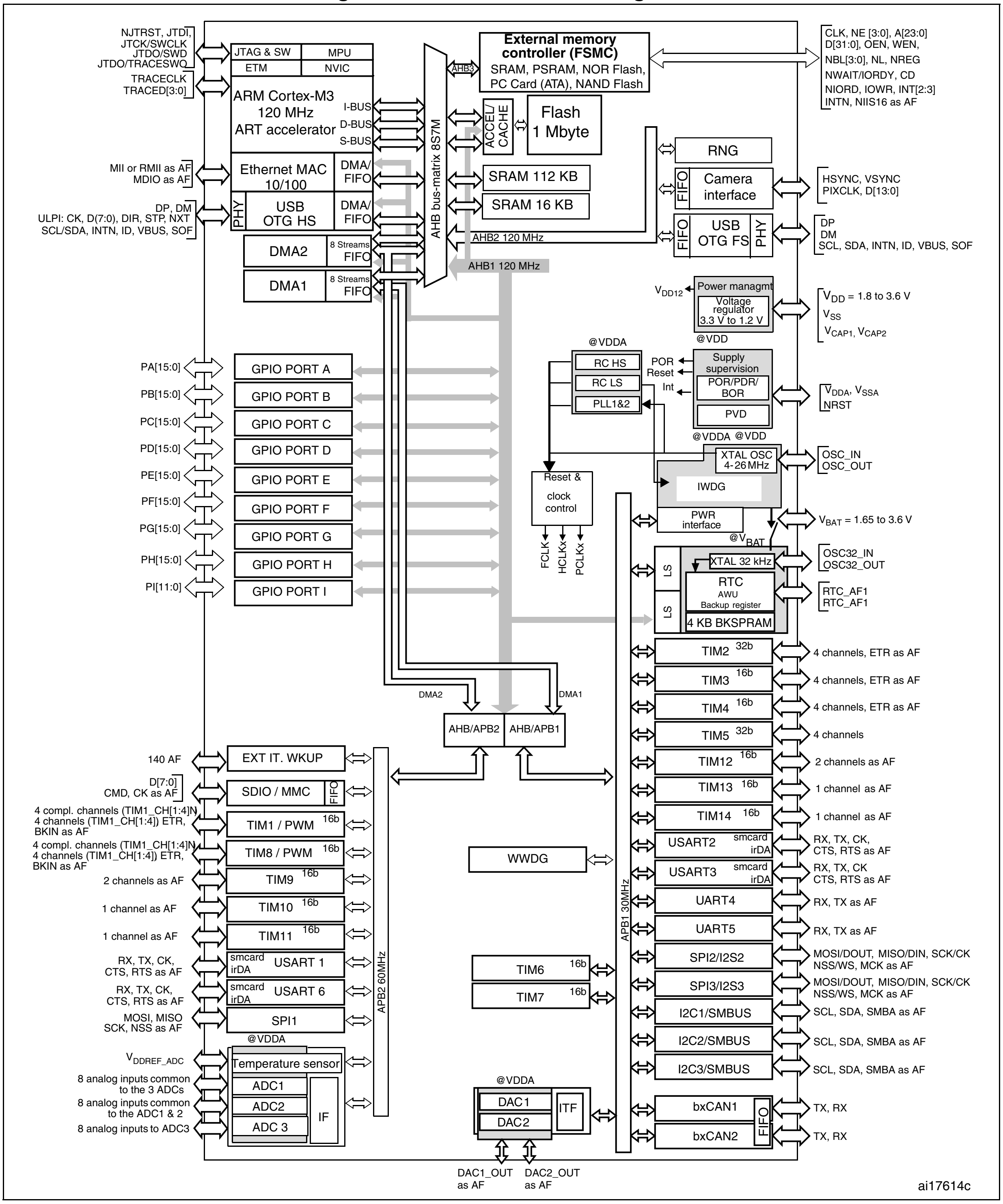
**Table 3. STM32F207xx features and peripheral counts (continued)**

| Peripherals | | STM32F207Vx | STM32F207Zx | STM32F207Ix |
|---|---|---|---|---|
| Comm. interfaces | SPI/($I^2S$) | 3/(2)[2] | | |
| | $I^2C$ | 3 | | |
| | USART<br>UART | 4<br>2 | | |
| | USB OTG FS | Yes | | |
| | USB OTG HS | Yes | | |
| | CAN | 2 | | |
| Camera interface | | Yes | | |
| GPIOs | | 82 | 114 | 140 |
| SDIO | | Yes | | |
| 12-bit ADC<br>Number of channels | | 3 | | |
| | | 16 | 24 | 24 |
| 12-bit DAC<br>Number of channels | | Yes<br>2 | | |
| Maximum CPU frequency | | 120 MHz | | |
| Operating voltage | | 1.8 V to 3.6 V[3] | | |
| Operating temperatures | | Ambient temperatures: –40 to +85 °C/–40 to +105 °C | | |
| | | Junction temperature: –40 to + 125 °C | | |
| Package | | LQFP100 | LQFP144 | LQFP176/<br>UFBGA176 |

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to $V_{DD}$, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

## Figure 4. STM32F20x block diagram




1. The timers connected to APB2 are clocked from TIMxCLK up to 120 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 60 MHz.
2. The camera interface and Ethernet are available only in STM32F207xx devices.

**Table 6. USART feature comparison**

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X | X | X | X | X | 1.87 | 7.5 | APB2 (max. 60 MHz) |
| USART2 | X | X | X | X | X | X | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| USART3 | X | X | X | X | X | X | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| UART4 | X | - | X | - | X | - | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| UART5 | X | - | X | - | X | - | 3.75 | 3.75 | APB1 (max. 30 MHz) |
| USART6 | X | X | X | X | X | X | 3.75 | 7.5 | APB2 (max. 60 MHz) |

## 3.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

## 3.24 Inter-integrated sound ($I^2S$)

Two standard $I^2S$ interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx interfaces can be served by the DMA controller.

## 3.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

## 3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

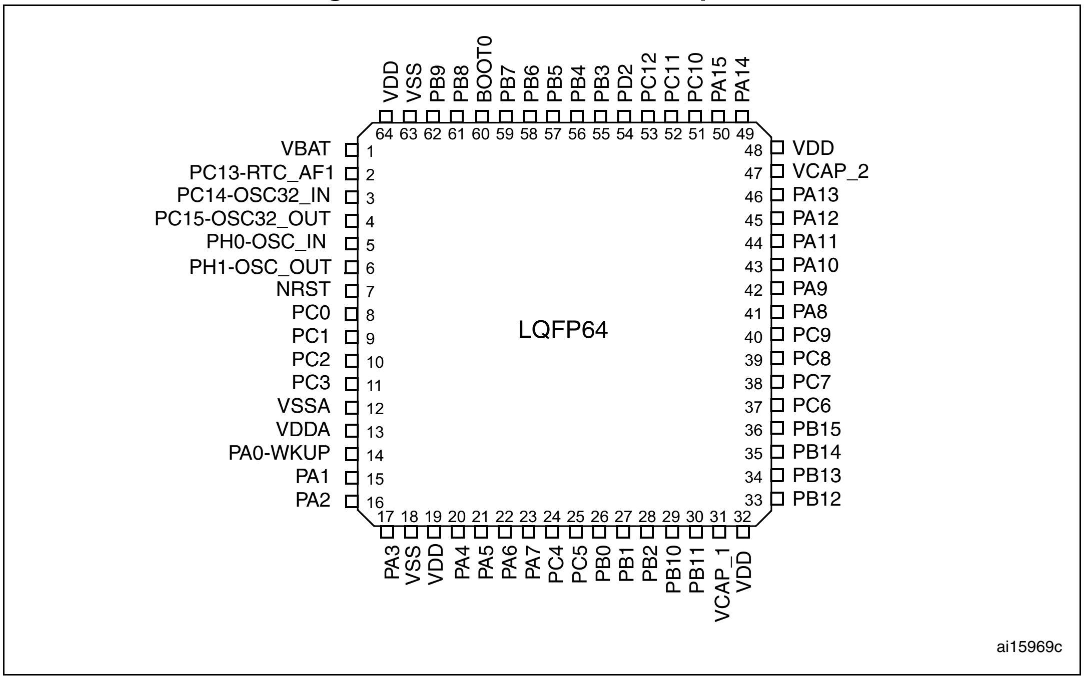
## 3.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F20x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

# 4 Pinouts and pin description

**Figure 10. STM32F20x LQFP64 pinout**




1. The above figure shows the package top view.

**Figure 11. STM32F20x WLCSP64+2 ballout**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | PA14 | PA15 | PC12 | PB3 | PB5 | PB7 | PB9 | VDD | $V_{BAT}$ |
| B | VSS | PA13 | PC10 | PB4 | PB6 | BOOT0 | PB8 | PC13 | PC14 |
| C | PA12 | VCAP_2 | PC11 | | | | PD2 | IRROFF | PC15 |
| D | PC9 | PA11 | PA10 | | | | PC2 | VSS | VDD |
| E | VDD | PA8 | PA9 | | | | PA0 | NRST | PH0-OSC_IN |
| F | VSS | PC7 | PC8 | | | | VREF+ | PC1 | PH1-OSC_OUT |
| G | PB15 | PC6 | PC5 | | | | PA3 | PC3 | PC0 |
| H | PB14 | PB13 | PB10 | PC4 | PA6 | PA5 | REGOFF | PA1 | VSS_5 |
| J | PB12 | PB11 | VCAP_1 | PB2 | PB1 | PB0 | PA7 | PA4 | PA2 |

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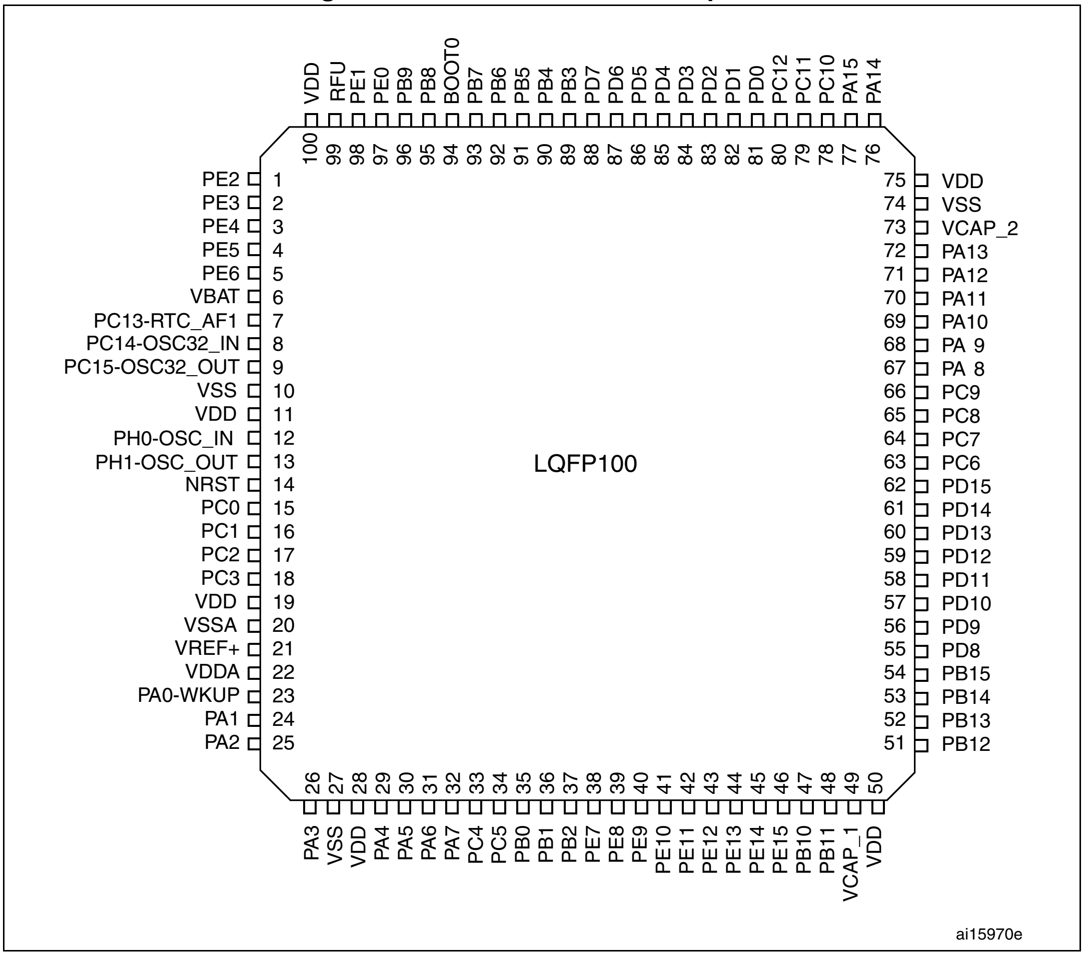
1. The above figure shows the package top view.

**Figure 12. STM32F20x LQFP100 pinout**




1. RFU means "reserved for future use". This pin can be tied to $V_{DD}$,$V_{SS}$ or left unconnected.
2. The above figure shows the package top view.

## Figure 15. STM32F20x UFBGA176 ballout

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PE3 | PE2 | PE1 | PE0 | PB8 | PB5 | PG14 | PG13 | PB4 | PB3 | PD7 | PC12 | PA15 | PA14 | PA13 |
| B | PE4 | PE5 | PE6 | PB9 | PB7 | PB6 | PG15 | PG12 | PG11 | PG10 | PD6 | PD0 | PC11 | PC10 | PA12 |
| C | VBAT | PI7 | PI6 | PI5 | VDD | RFU | VDD | VDD | VDD | PG9 | PD5 | PD1 | PI3 | PI2 | PA11 |
| D | PC13-TAMP1 | PI8-TAMP2 | PI9 | PI4 | VSS | BOOT0 | VSS | VSS | VSS | PD4 | PD3 | PD2 | PH15 | PI1 | PA10 |
| E | PC14-OSC32_IN | PF0 | PI10 | PI11 | | | | | | | | PH13 | PH14 | PI0 | PA9 |
| F | PC15-OSC32_OUT | VSS | VDD | PH2 | | VSS | VSS | VSS | VSS | VSS | | VSS | VCAP_2 | PC9 | PA8 |
| G | PH0-OSC_IN | VSS | VDD | PH3 | | VSS | VSS | VSS | VSS | VSS | | VSS | VDD | PC8 | PC7 |
| H | PH1-OSC_OUT | PF2 | PF1 | PH4 | | VSS | VSS | VSS | VSS | VSS | | VSS | VDD | PG8 | PC6 |
| J | NRST | PF3 | PF4 | PH5 | | VSS | VSS | VSS | VSS | VSS | | VDD | VDD | PG7 | PG6 |
| K | PF7 | PF6 | PF5 | VDD | | VSS | VSS | VSS | VSS | VSS | | PH12 | PG5 | PG4 | PG3 |
| L | PF10 | PF9 | PF8 | REGOFF | | | | | | | | PH11 | PH10 | PD15 | PG2 |
| M | VSSA | PC0 | PC1 | PC2 | PC3 | PB2 | PG1 | VSS | VSS | VCAP_1 | PH6 | PH8 | PH9 | PD14 | PD13 |
| N | VREF- | PA1 | PA0-WKUP | PA4 | PC4 | PF13 | PG0 | VDD | VDD | VDD | PE13 | PH7 | PD12 | PD11 | PD10 |
| P | VREF+ | PA2 | PA6 | PA5 | PC5 | PF12 | PF15 | PE8 | PE9 | PE11 | PE14 | PB12 | PB13 | PD9 | PD8 |
| R | VDDA | PA3 | PA7 | PB1 | PB0 | PF11 | PF14 | PE7 | PE10 | PE12 | PE15 | PB10 | PB11 | PB14 | PB15 |

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1. RFU means “reserved for future use”. This pin can be tied to $V_{DD}$,$V_{SS}$ or left unconnected.
2. The above figure shows the package top view.

## Table 7. Legend/abbreviations used in the pinout table

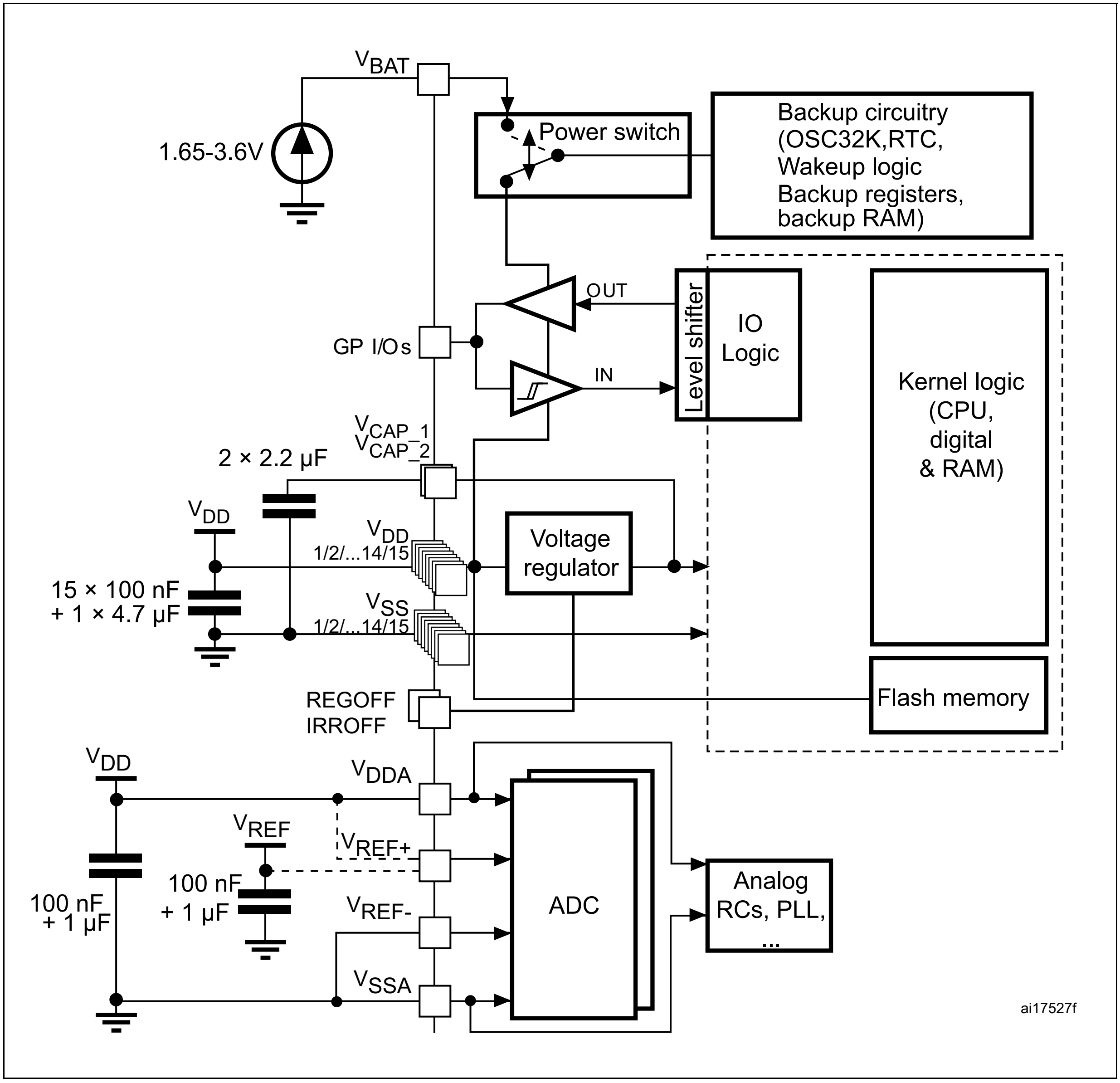
| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input/ output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | TTa | 3.3 V tolerant I/O |
| | B | Dedicated BOOT0 pin |
| | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Alternate functions | Functions selected through GPIOx_AFR registers | |
| Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 8. STM32F20x pin and ball definitions (continued)**

| Pins | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | 131 | 159 | C7 | $V_{DD}$ | S | - | - | - | - |
| - | - | - | 132 | 160 | B7 | PG15 | I/O | FT | - | USART6_CTS, DCMI_D13, EVENTOUT | - |
| 55 | A4 | 89 | 133 | 161 | A10 | PB3 (JTDO/TRACESWO) | I/O | FT | - | JTDO/ TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT | - |
| 56 | B4 | 90 | 134 | 162 | A9 | PB4 | I/O | FT | - | NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT | - |
| 57 | A5 | 91 | 135 | 163 | A6 | PB5 | I/O | FT | - | I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCMI_D10, I2S3_SD, EVENTOUT | - |
| 58 | B5 | 92 | 136 | 164 | B6 | PB6 | I/O | FT | - | I2C1_SCL,, TIM4_CH1, CAN2_TX, DCMI_D5,USART1_TX, EVENTOUT | - |
| 59 | A6 | 93 | 137 | 165 | B5 | PB7 | I/O | FT | - | I2C1_SDA, FSMC_NL(6), DCMI_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT | - |
| 60 | B6 | 94 | 138 | 166 | D6 | BOOT0 | I | B | - | - | $V_{PP}$ |
| 61 | B7 | 95 | 139 | 167 | A5 | PB8 | I/O | FT | - | TIM4_CH3,SDIO_D4, TIM10_CH1, DCMI_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT | - |
| 62 | A7 | 96 | 140 | 168 | B4 | PB9 | I/O | FT | - | SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCMI_D7, I2C1_SDA, CAN1_TX, EVENTOUT | - |
| - | - | 97 | 141 | 169 | A4 | PE0 | I/O | FT | - | TIM4_ETR, FSMC_NBL0, DCMI_D2, EVENTOUT | - |

### 6.1.6 Power supply scheme

**Figure 19. Power supply scheme**




1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect REGOFF and IRROFF pins, refer to *Section 3.16: Voltage regulator*.
3. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
4. The 4.7 µF ceramic capacitor must be connected to one of the $V_{DD}$ pin.

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB, to ensure good device operation. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect device operation.

**Table 15. Limitations depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency ($f_{Flashmax}$) | Number of wait states at maximum CPU frequency ($f_{CPUmax}$= 120 MHz)(1) | I/O operation | FSMC_CLK frequency for synchronous accesses | Possible Flash memory operations |
|---|---|---|---|---|---|---|
| $V_{DD}$ =1.8 to 2.1 V(2) | Conversion time up to 1 Msps | 16 MHz with no Flash memory wait state | 7(3) | – Degraded speed performance<br>– No I/O compensation | Up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1 Msps | 18 MHz with no Flash memory wait state | 6(3) | – Degraded speed performance<br>– No I/O compensation | Up to 30 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2 Msps | 24 MHz with no Flash memory wait state | 4(3) | – Degraded speed performance<br>– I/O compensation works | Up to 48 MHz | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(4) | Conversion time up to 2 Msps | 30 MHz with no Flash memory wait state | 3(3) | – Full-speed operation<br>– I/O compensation works | – Up to 60 MHz when $V_{DD}$ = 3.0 to 3.6 V<br>– Up to 48 MHz when $V_{DD}$ = 2.7 to 3.0 V | 32-bit erase and program operations |

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to $V_{DD}$, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

### 6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for $T_A$.

**Table 17. Operating conditions at power-up / power-down (regulator ON)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | 20 | ∞ | |

### 6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for $T_A$.

**Table 18. Operating conditions at power-up / power-down (regulator OFF)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | Power-up | 20 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | Power-down | 20 | ∞ | |
| $t_{VCAP}$ | $V_{CAP\_1}$ and $V_{CAP\_2}$ rise time rate | Power-up | 20 | ∞ | |
| | $V_{CAP\_1}$ and $V_{CAP\_2}$ fall time rate | Power-down | 20 | ∞ | |

Table 19. Embedded reset and power control block characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BOR2}$ | Brownout level 2 threshold | Falling edge | 2.44 | 2.50 | 2.56 | V |
| | | Rising edge | 2.53 | 2.59 | 2.63 | V |
| $V_{BOR3}$ | Brownout level 3 threshold | Falling edge | 2.75 | 2.83 | 2.88 | V |
| | | Rising edge | 2.85 | 2.92 | 2.97 | V |
| $V_{BORhyst}$(1) | BOR hysteresis | - | - | 100 | - | mV |
| $T_{RSTTEMPO}$(1)(2) | Reset temporization | - | 0.5 | 1.5 | 3.0 | ms |
| $I_{RUSH}$(1) | InRush current on voltage regulator power-on (POR or wakeup from Standby) | - | - | 160 | 200 | mA |
| $E_{RUSH}$(1) | InRush energy on voltage regulator power-on (POR or wakeup from Standby) | $V_{DD}$ = 1.8 V, $T_A$ = 105 °C, $I_{RUSH}$ = 171 mA for 31 µs | - | - | 5.4 | µC |

1. Guaranteed by design, not tested in production.
2. The reset temporization is measured from the power-on (POR reset or wakeup from $V_{BAT}$) to the instant when first instruction is read by the user application code.

### 6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 20: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using CoreMark code.

**Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | Max[1] | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | External clock[2], all peripherals enabled[3] | 120 MHz | 61 | 81 | 93 | mA |
| | | | 90 MHz | 48 | 68 | 80 | |
| | | | 60 MHz | 33 | 53 | 65 | |
| | | | 30 MHz | 18 | 38 | 50 | |
| | | | 25 MHz | 14 | 34 | 46 | |
| | | | 16 MHz[4] | 10 | 30 | 42 | |
| | | | 8 MHz | 6 | 26 | 38 | |
| | | | 4 MHz | 4 | 24 | 36 | |
| | | | 2 MHz | 3 | 23 | 35 | |
| | | External clock[2], all peripherals disabled | 120 MHz | 33 | 54 | 66 | |
| | | | 90 MHz | 27 | 47 | 59 | |
| | | | 60 MHz | 19 | 39 | 51 | |
| | | | 30 MHz | 11 | 31 | 43 | |
| | | | 25 MHz | 8 | 28 | 41 | |
| | | | 16 MHz[4] | 6 | 26 | 38 | |
| | | | 8 MHz | 4 | 24 | 36 | |
| | | | 4 MHz | 3 | 23 | 35 | |
| | | | 2 MHz | 2 | 23 | 34 | |

1. Guaranteed by characterization results, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 44. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*.

**Table 45. I/O current injection susceptibility(1)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 pin | –0 | NA | mA |
| | Injected current on NRST pin | –0 | NA | |
| | Injected current on TTa pins: PA4 and PA5 | –0 | +5 | |
| | Injected current on all FT pins | –5 | NA | |

1. NA stands for “not applicable”.

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

## 6.3.16 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in Table 50 are derived from tests performed under the conditions summarized in Table 14: General operating conditions.

All I/Os are CMOS and TTL compliant.

**Table 46. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | FT, TTa and NRST I/O input low level voltage | 1.7 V≤$V_{DD}$≤3.6 V | - | - | $0.35V_{DD}$–0.04(1) | V |
| | | | | | $0.3V_{DD}$(2) | |
| | BOOT0 I/O input low level voltage | 1.75 V≤$V_{DD}$ ≤3.6 V, –40 °C≤$T_A$ ≤105 °C | - | - | $0.1V_{DD}$+0.1(1) | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤105 °C | - | - | | |
| $V_{IH}$ | FT, TTa and NRST I/O input high level voltage(5) | 1.7 V≤$V_{DD}$≤3.6 V | $0.45V_{DD}$+0.3(1) | - | - | V |
| | | | $0.7V_{DD}$(2) | | | |
| | BOOT0 I/O input high level voltage | 1.75 V≤$V_{DD}$ ≤3.6 V, –40 °C≤$T_A$ ≤105 °C | $0.17V_{DD}$+0.7(1) | - | - | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤105 °C | | | | |
| $V_{HYS}$ | FT, TTa and NRST I/O input hysteresis | 1.7 V≤$V_{DD}$≤3.6 V | $0.45V_{DD}$+0.3(1) | - | - | V |
| | BOOT0 I/O input hysteresis | 1.75 V≤$V_{DD}$ ≤3.6 V, –40 °C≤$T_A$ ≤105 °C | 10%$V_{DDIO}$(1)(3) | - | - | |
| | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤105 °C | 100(1) | - | - | |
| $I_{lkg}$ | I/O input leakage current (4) | $V_{SS}$ ≤$V_{IN}$ ≤$V_{DD}$ | - | - | ±1 | µA |
| | I/O FT input leakage current (5) | $V_{IN}$ = 5 V | - | - | 3 | |

**Table 46. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(6) | All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | - | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor(7) | All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | - | 7 | 10 | 14 | |
| $C_{IO}$(8) | I/O pin capacitance | | - | - | 5 | - | pF |

1. Guaranteed by design, not tested in production.
2. Guaranteed by tests in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 45: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 45: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 38*.

**Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | ns |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | ns |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results, not tested in production.

**Figure 60. Asynchronous multiplexed PSRAM/NOR write waveforms**

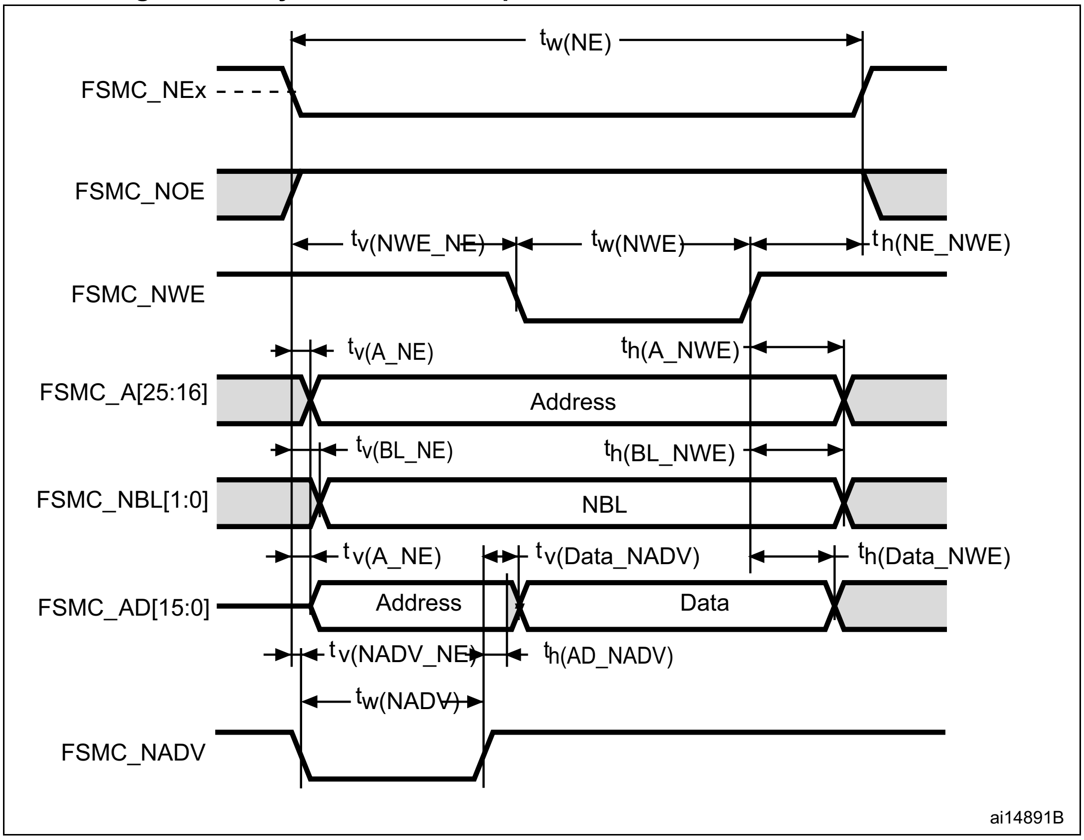
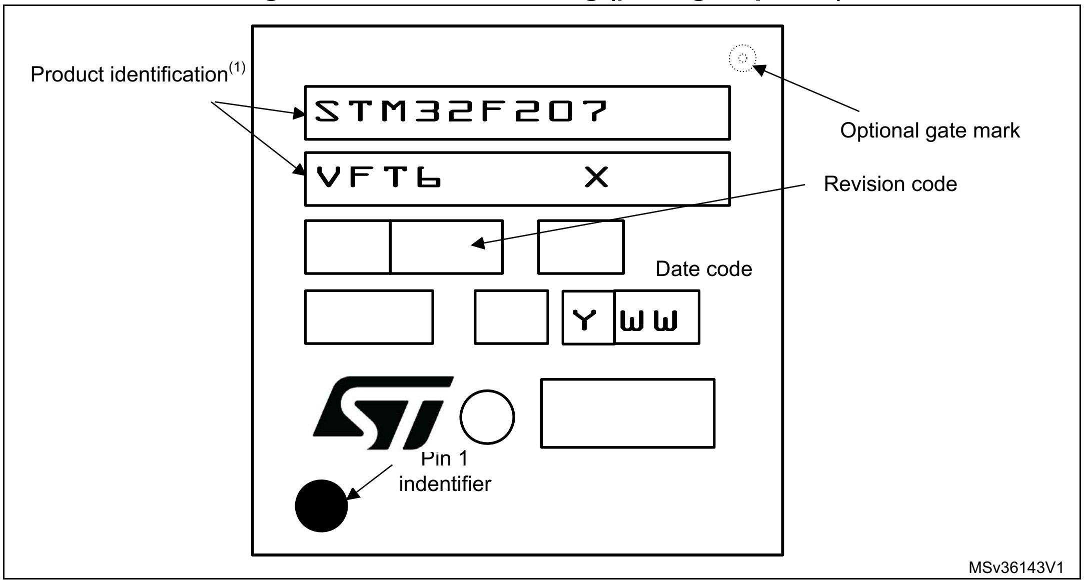



**Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $4T_{HCLK}$-1 | $4T_{HCLK}$+1 | ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK}$- 1 | $T_{HCLK}$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low tim e | $2T_{HCLK}$ | $2T_{HCLK}$+1 | ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK}$- 1 | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | 1 | 2 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK}$– 2 | $T_{HCLK}$+ 2 | ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD(adress) valid hold time after FSMC_NADV high) | $T_{HCLK}$ | - | ns |

## Device marking

**Figure 83. LQFP100 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.