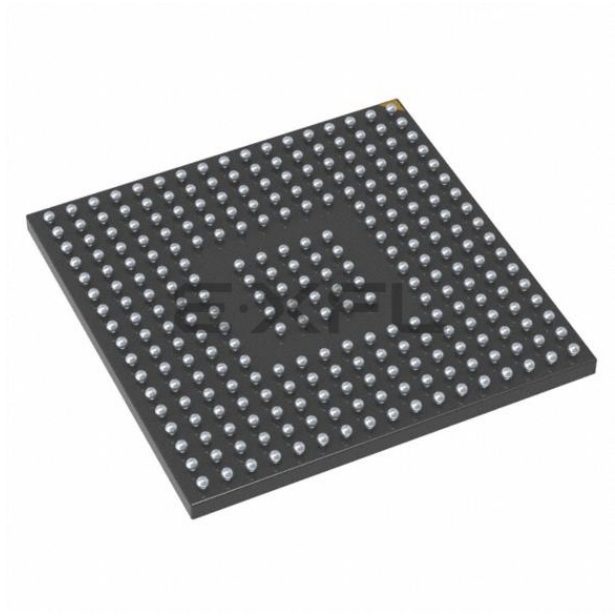

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207igh6

List of tables

2.1 Full compatibility throughout the family

The STM32F205xx and STM32F207xx constitute the STM32F20x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F205xx and STM32F207xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F205xx and STM32F207xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F20x family remains simple as only a few pins are impacted.

Figure 1, *Figure 2* and *Figure 3* provide compatible board designs between the STM32F20x and the STM32F10xxx family.

Figure 1. Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package

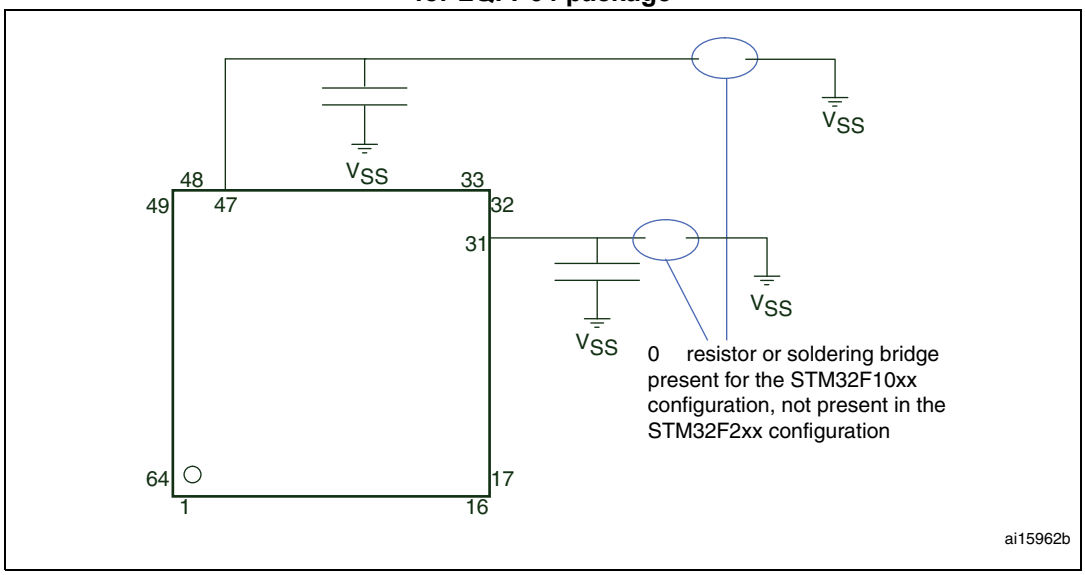
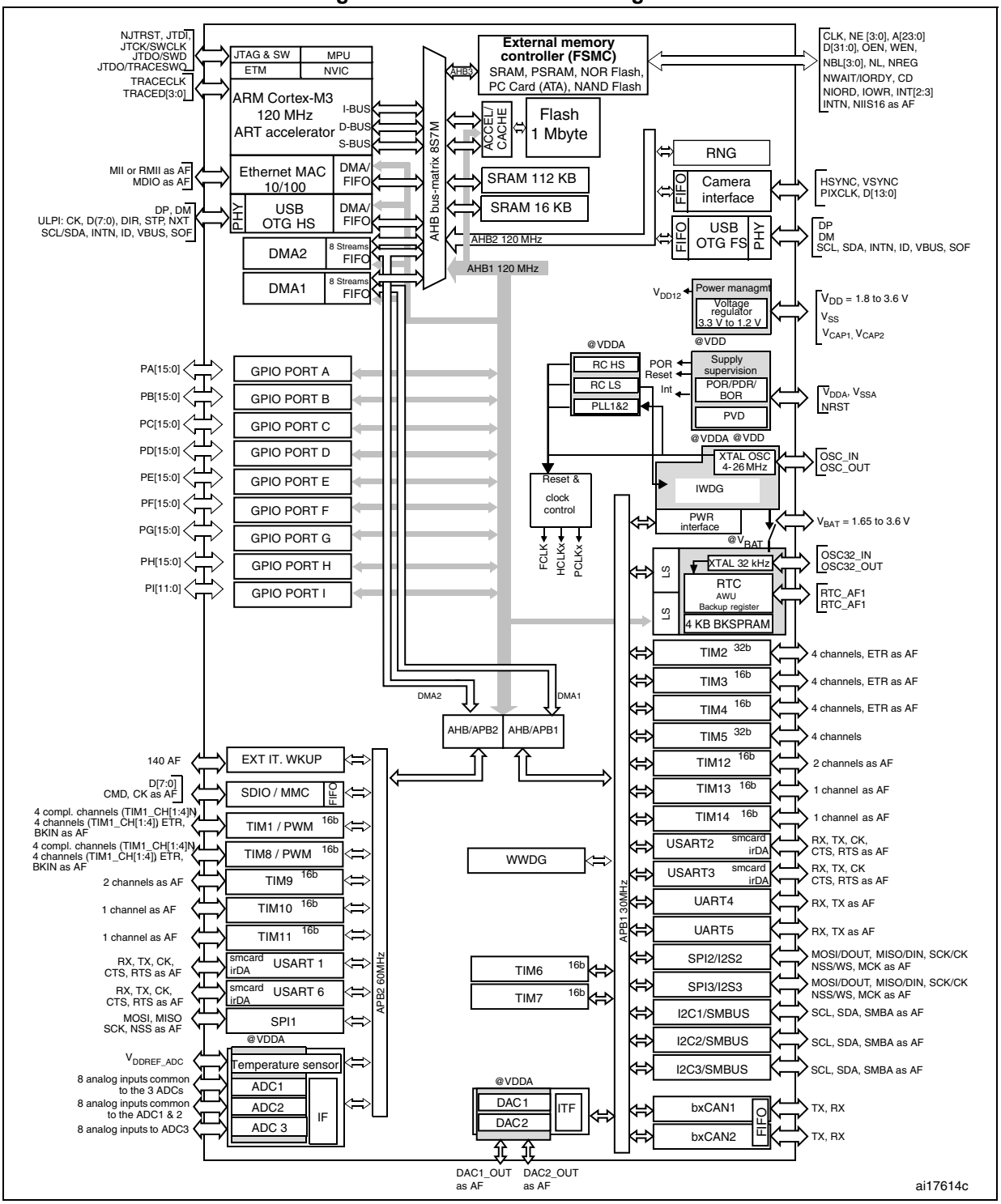
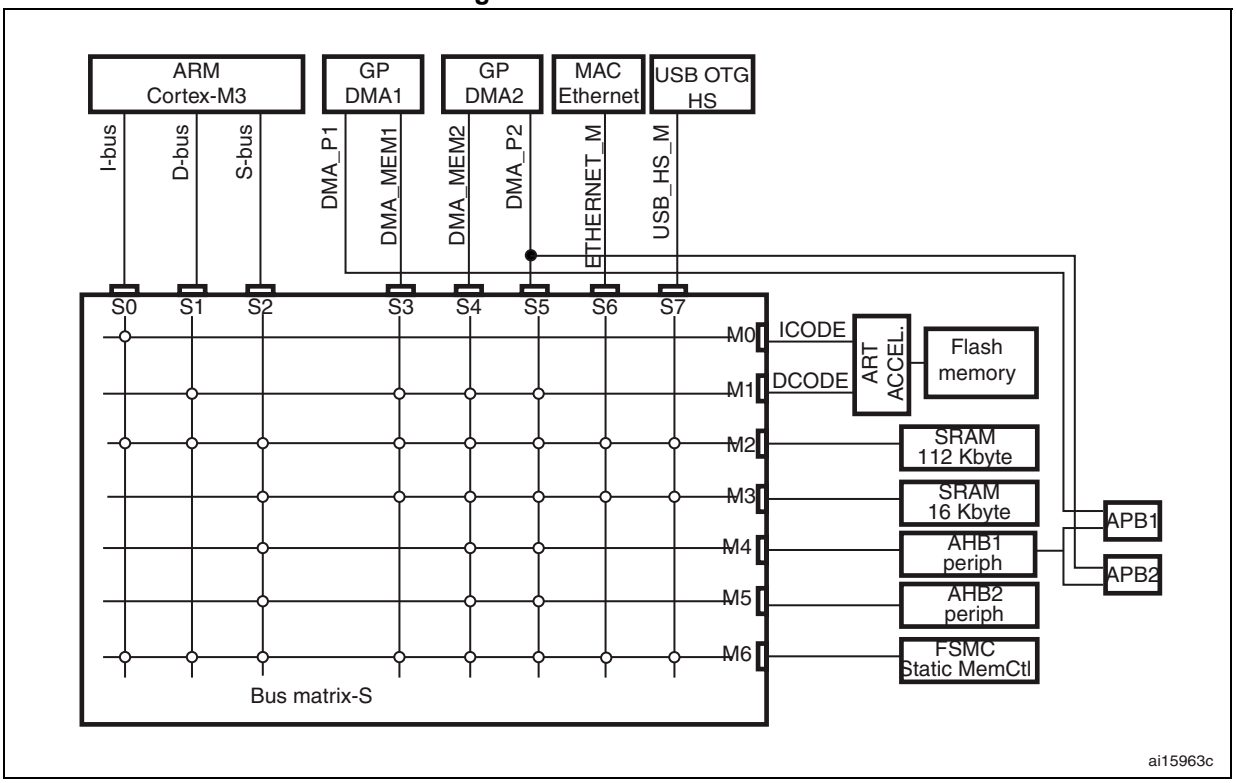


Figure 4. STM32F20x block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 120 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 60 MHz.
2. The camera interface and Ethernet are available only in STM32F207xx devices.

Figure 5. Multi-AHB matrix



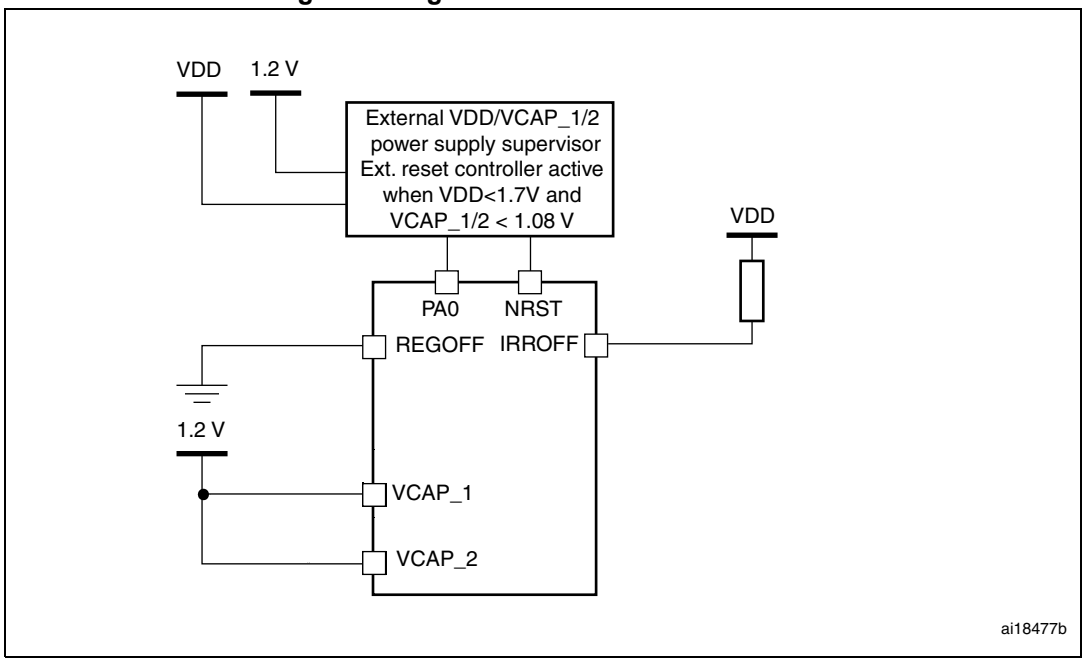
3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

Figure 7. Regulator OFF/internal reset OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains (see *Figure 8*).
- PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V, and until V_{DD} reaches 1.7 V.
- NRST should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.7 V (see *Figure 9*).

In this mode, when the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry is disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see *Table 5* for differences).

TIM2, TIM3, TIM4, TIM5

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

3.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.
The counter can be frozen in debug mode.

3.20.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.21 Inter-integrated circuit interface (I²C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

3.22 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F20x devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

3.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

3.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F20x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024× 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-
-	-	-	-	85	M12	PH8	I/O	FT	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	86	M13	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	-
-	-	-	-	87	L13	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	88	L12	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	89	K12	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	90	H12	V_{SS}	S	-	-	-	-
-	-	-	-	91	J12	V_{DD}	S	-	-	-	-
33	J1	51	73	92	P12	PB12	I/O	FT	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-
34	H2	52	74	93	P13	PB13	I/O	FT	-	SPI2_SCK, I2S2_SCK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_ VBUS
35	H1	53	75	94	R14	PB14	I/O	FT	-	SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM USART3_RTS, TIM8_CH2N, EVENTOUT	-
36	G1	54	76	95	R15	PB15	I/O	FT	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, RTC_50Hz, EVENTOUT	-
-	-	55	77	96	P15	PD8	I/O	FT	-	FSMC_D13, USART3_TX, EVENTOUT	-

Figure 16. Memory map

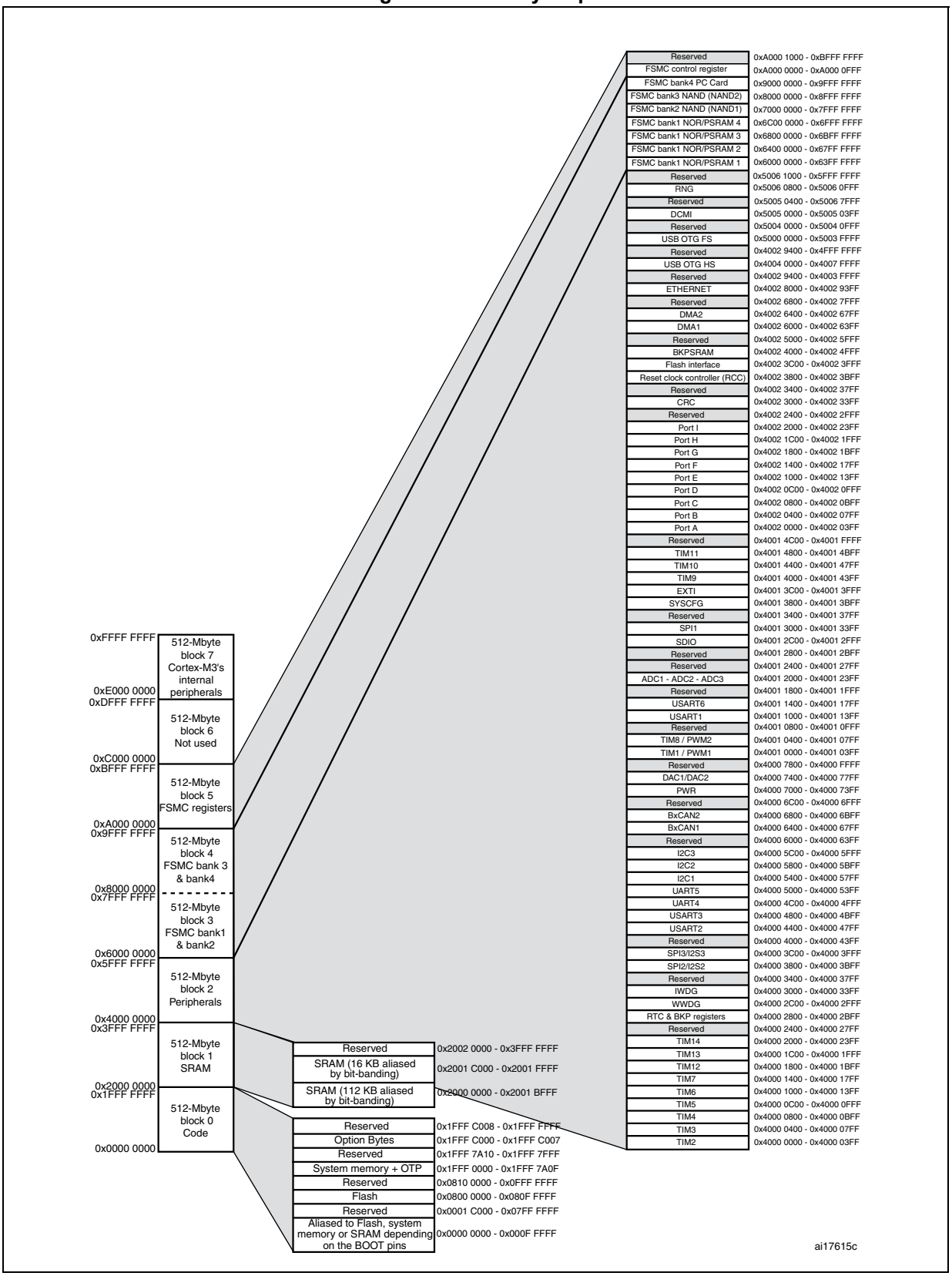


Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8(1)	3.6	V
V_{DDA}(2)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(3)	1.8(1)	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP64	-	444	mW
		WLCSP64+2	-	392	
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 26*. The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- The code is running from Flash memory and the Flash memory access time is equal to 3 wait states at 120 MHz
- Prefetch and Cache ON
- When the peripherals are enabled, HCLK = 120MHz, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$
- The typical values are obtained for V_{DD} = 3.3 V and T_A= 25 °C, unless otherwise specified.

Table 26. Peripheral current consumption

Peripheral(1)		Typical consumption at 25 °C	Unit
AHB1	GPIO A	0.45	mA
	GPIO B	0.43	
	GPIO C	0.46	
	GPIO D	0.44	
	GPIO E	0.44	
	GPIO F	0.42	
	GPIO G	0.44	
	GPIO H	0.42	
	GPIO I	0.43	
	OTG_HS + ULPI	3.64	
	CRC	1.17	
	BKPSRAM	0.21	
	DMA1	2.76	
	DMA2	2.85	
	ETH_MAC + ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	2.99	
AHB2	OTG_FS	3.16	
	DCMI	0.60	
AHB3	FSMC	1.74	

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 14: General operating conditions*.

All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

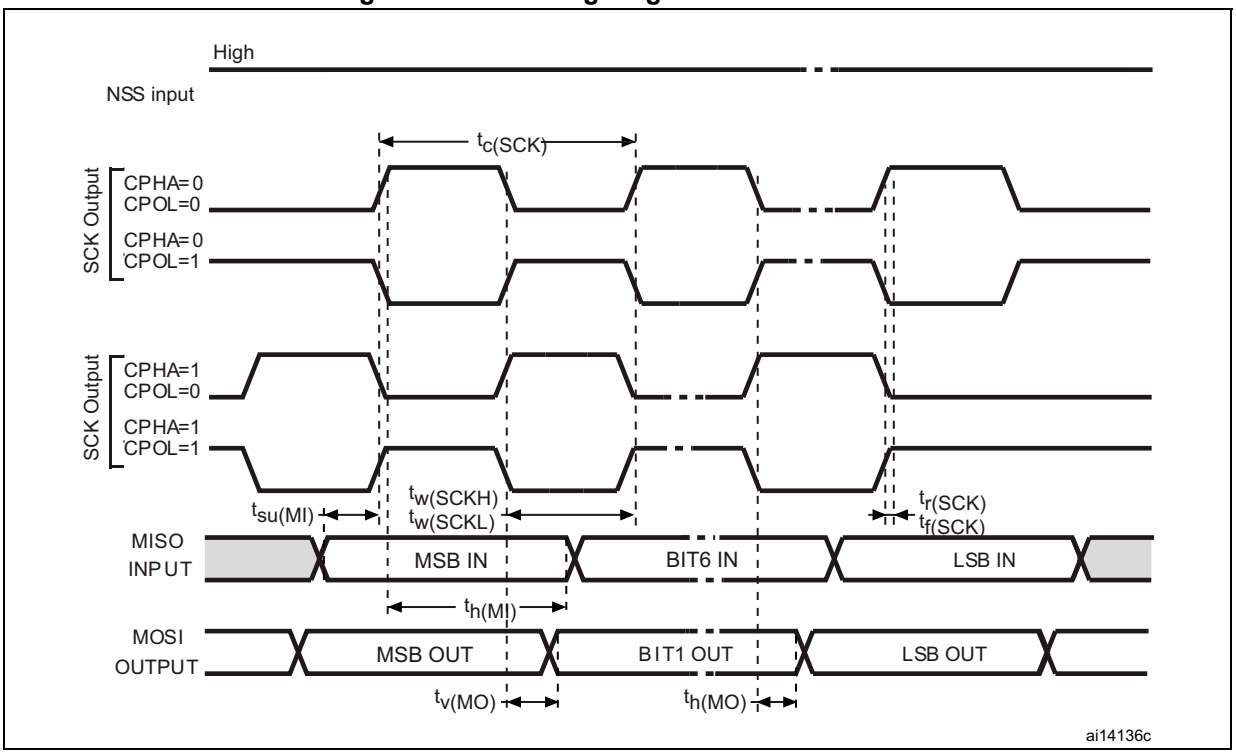
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04^{(1)}$ $0.3V_{DD}^{(2)}$	V
	BOOT0 I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	-	$0.1V_{DD}+0.1^{(1)}$	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3^{(1)}$ $0.7V_{DD}^{(2)}$	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7^{(1)}$	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3^{(1)}$	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$10\%V_{DDIO}^{(1)(3)}$	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	$100^{(1)}$	-	-	
I_{lkg}	I/O input leakage current (4)	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)	V_{IN} = 5 V	-	-	3	

Table 48. I/O AC characteristics(1) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-3	6	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100(3)	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50(3)	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	120(3)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100(3)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. The maximum frequency is defined in *Figure 39*.
3. For maximum frequencies above 50 MHz and V_{DD} above 2.4 V, the compensation cell should be used.

Figure 44. SPI timing diagram - master mode



6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8(1)	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)(2)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(1) to 2.4 V	0.6	-	15	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	-	30	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 30 MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(4)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(3)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(3)(5)	Sampling switch resistance	-	1.5	-	6	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	4	-	pF
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(6)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(6)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	2	3	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.5	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.3	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 66. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S (3)	Sampling rate (f_{ADC} = 30 MHz)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+} (3)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA} (3)	ADC VDDA DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. It is recommended to maintain the voltage difference between V_{REF+} and V_{DDA} below 1.8 V.
3. Guaranteed by characterization results, not tested in production.
4. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
5. R_{ADC} maximum value is given for V_{DD}=1.8 V, and minimum value for V_{DD}=3.3 V.
6. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 66*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 67. ADC accuracy (1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{PCLK2} = 60 MHz, f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.8(3) to 3.6 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results, not tested in production.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

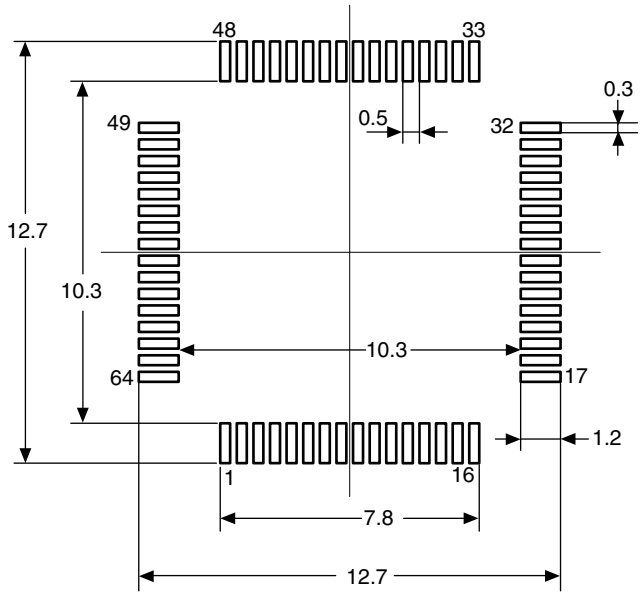
Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

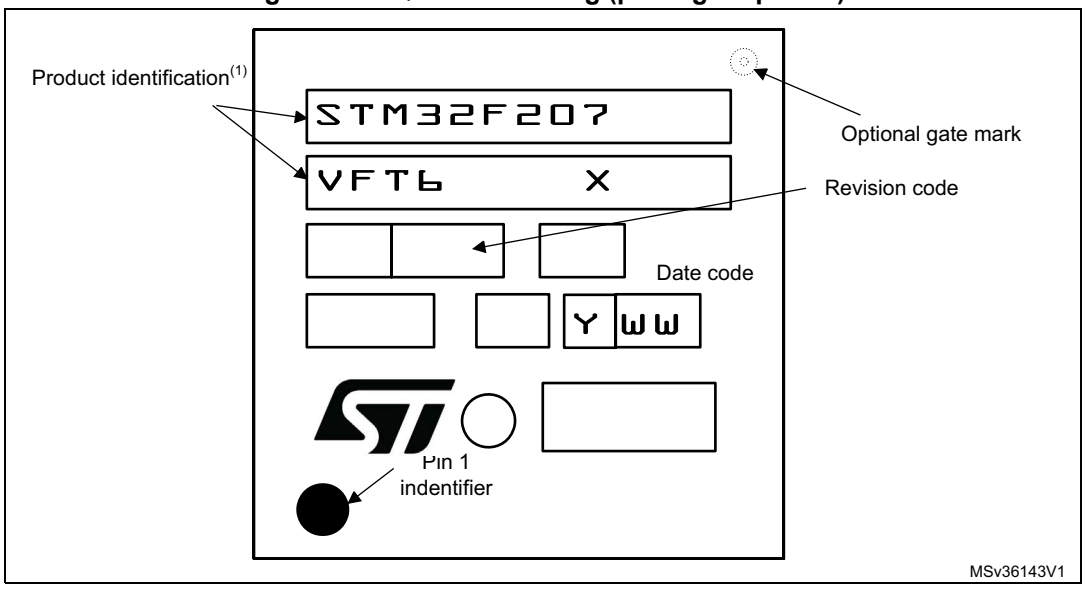
Figure 78. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

Figure 83. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Part numbering

Table 96. Ordering information scheme

Example: STM32 F 205 R E T 6 Vxxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

205 = STM32F20x, connectivity

207= STM32F20x, connectivity, camera interface, Ethernet

Pin count

R = 64 pins or 66 pins(1)

V = 100 pins

Z = 144 pins

I = 176 pins

Flash memory size

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

F = 768 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

T = LQFP

H = UFBGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Software option

Internal code or Blank

Options

xxx = programmed parts

TR = tape and reel

1. The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.