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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

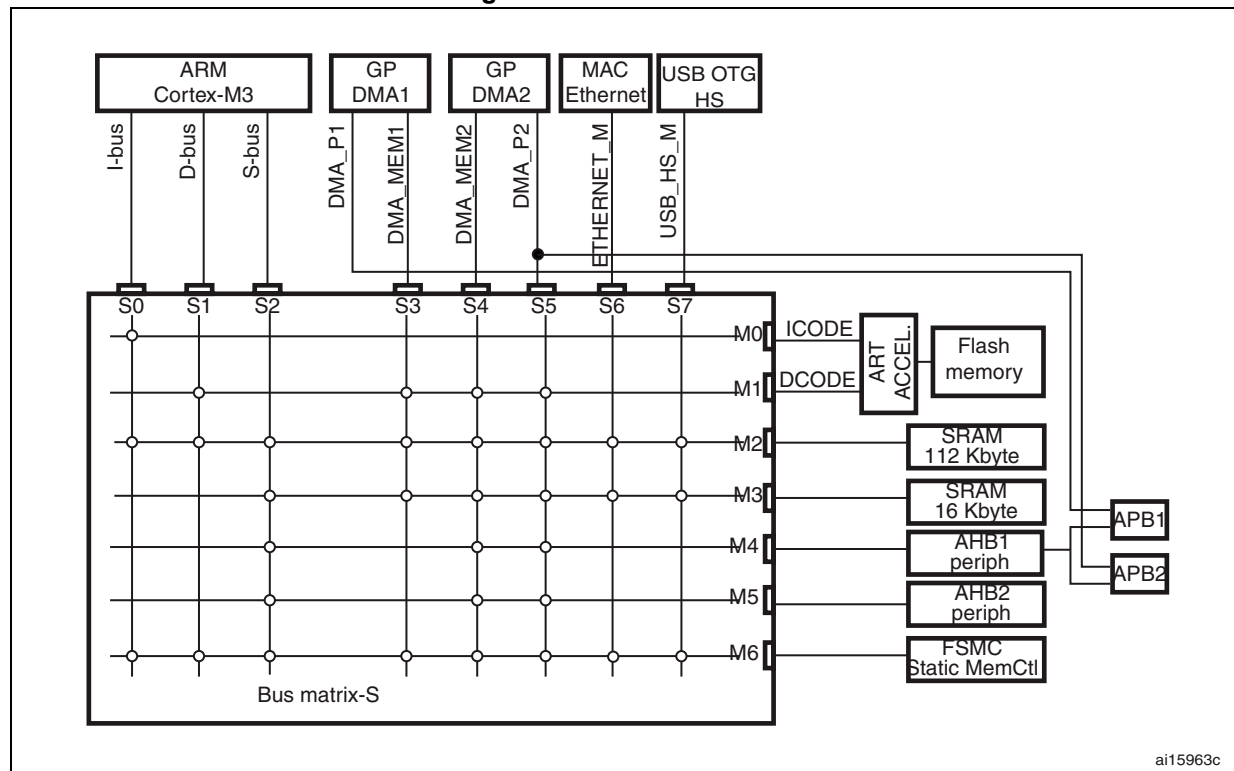
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFPGA
Supplier Device Package	176+25UFPGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207igh6j

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Figure 5. Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).

- V_{SSA} , V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 19: Power supply scheme](#) for more details.

3.15 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry.

At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit. On devices in WLCSP64+2 package, the BOR, POR and PDR features can be disabled by setting IRROFF pin to V_{DD} . In this mode an external power supply supervisor is required (see [Section 3.16](#)).

The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.16 Voltage regulator

The regulator has five operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low-power regulator (LPR)
 - Power-down
- Regulator OFF
 - Regulator OFF/internal reset ON
 - Regulator OFF/internal reset OFF

3.16.1 Regulator ON

The regulator ON modes are activated by default on LQFP packages. On WLCSP64+2 package, they are activated by connecting both REGOFF and IRROFF pins to V_{SS} , while only REGOFF must be connected to V_{SS} on UFBGA176 package (IRROFF is not available).

V_{DD} minimum value is 1.8 V.

Table 6. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	IrDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	1.87	7.5	APB2 (max. 60 MHz)
USART2	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
USART3	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
UART4	X	-	X	-	X	-	1.87	3.75	APB1 (max. 30 MHz)
UART5	X	-	X	-	X	-	3.75	3.75	APB1 (max. 30 MHz)
USART6	X	X	X	X	X	X	3.75	7.5	APB2 (max. 60 MHz)

3.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.24 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx interfaces can be served by the DMA controller.

3.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
22	H5	31	42	52	P3	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6
23	J7	32	43	53	R3	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
24	H4	33	44	54	N5	PC4	I/O	FT	(4)	ETH_RMII_RXD0, ETH_MII_RXD0, EVENTOUT	ADC12_IN14
25	G3	34	45	55	P5	PC5	I/O	FT	(4)	ETH_RMII_RXD1, ETH_MII_RXD1, EVENTOUT	ADC12_IN15
26	J6	35	46	56	R5	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
27	J5	36	47	57	R4	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
28	J4	37	48	58	M6	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	49	59	R6	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	50	60	P6	PF12	I/O	FT	-	FSMC_A6, EVENTOUT	-
-	-	-	51	61	M8	V _{SS}	S		-	-	-
-	-	-	52	62	N8	V _{DD}	S		-	-	-
-	-	-	53	63	N6	PF13	I/O	FT	-	FSMC_A7, EVENTOUT	-
-	-	-	54	64	R7	PF14	I/O	FT	-	FSMC_A8, EVENTOUT	-
-	-	-	55	65	P7	PF15	I/O	FT	-	FSMC_A9, EVENTOUT	-
-	-	-	56	66	N7	PG0	I/O	FT	-	FSMC_A10, EVENTOUT	-
-	-	-	57	67	M7	PG1	I/O	FT	-	FSMC_A11, EVENTOUT	-

Table 9. FSMC pin definition (continued)

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE5	-	A21	A21	-	Yes
PE6	-	A22	A22	-	Yes
PF0	A0	A0	-	-	-
PF1	A1	A1	-	-	-
PF2	A2	A2	-	-	-
PF3	A3	A3	-	-	-
PF4	A4	A4	-	-	-
PF5	A5	A5	-	-	-
PF6	NIORD	-	-	-	-
PF7	NREG	-	-	-	-
PF8	NIOWR	-	-	-	-
PF9	CD	-	-	-	-
PF10	INTR	-	-	-	-
PF12	A6	A6	-	-	-
PF13	A7	A7	-	-	-
PF14	A8	A8	-	-	-
PF15	A9	A9	-	-	-
PG0	A10	A10	-	-	-
PG1	-	A11	-	-	-
PE7	D4	D4	DA4	D4	Yes
PE8	D5	D5	DA5	D5	Yes
PE9	D6	D6	DA6	D6	Yes
PE10	D7	D7	DA7	D7	Yes
PE11	D8	D8	DA8	D8	Yes
PE12	D9	D9	DA9	D9	Yes
PE13	D10	D10	DA10	D10	Yes
PE14	D11	D11	DA11	D11	Yes
PE15	D12	D12	DA12	D12	Yes
PD8	D13	D13	DA13	D13	Yes
PD9	D14	D14	DA14	D14	Yes
PD10	D15	D15	DA15	D15	Yes
PD11	-	A16	A16	CLE	Yes
PD12	-	A17	A17	ALE	Yes

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_HS	DCMI		
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FSMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FSMC_D3	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	-	-	FSMC_CLK	-	-	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FSMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	FSMC_NWAIT	-	-	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FSMC_NE1/ FSMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FSMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FSMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FSMC_D15	-	-	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	FSMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	FSMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FSMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FSMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FSMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	-	FSMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	-	-	-	-	-	-	ETH_MII_TXD3	FSMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	-	FSMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	-	-	-	-	-	-	-	FSMC_A20	DCMI_D4	-	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	-	-	-	-	-	-	-	FSMC_A21	DCMI_D6	-	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	-	-	-	-	-	-	-	FSMC_A22	DCMI_D7	-	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FSMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	FSMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	FSMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	FSMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	FSMC_D8	-	-	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-	-	FSMC_D9	-	-	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	FSMC_D10	-	-	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	-	-	-	-	-	-	-	FSMC_D11	-	-	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FSMC_D12	-	-	EVENTOUT

Figure 27. Typical current consumption vs. temperature in Sleep mode, peripherals ON

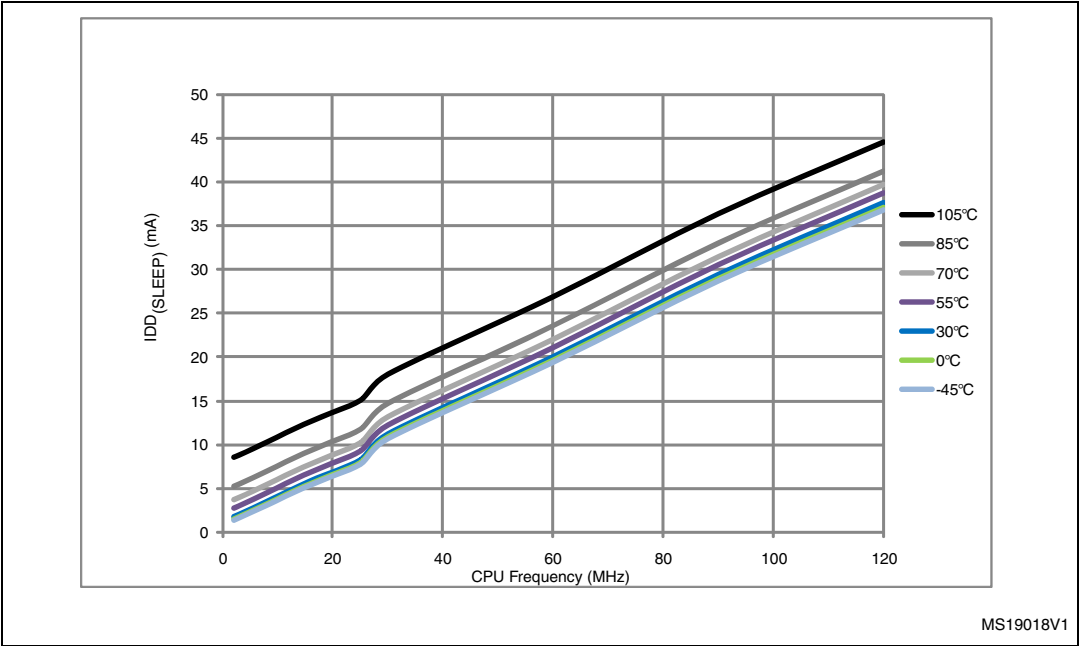


Figure 28. Typical current consumption vs. temperature in Sleep mode, peripherals OFF

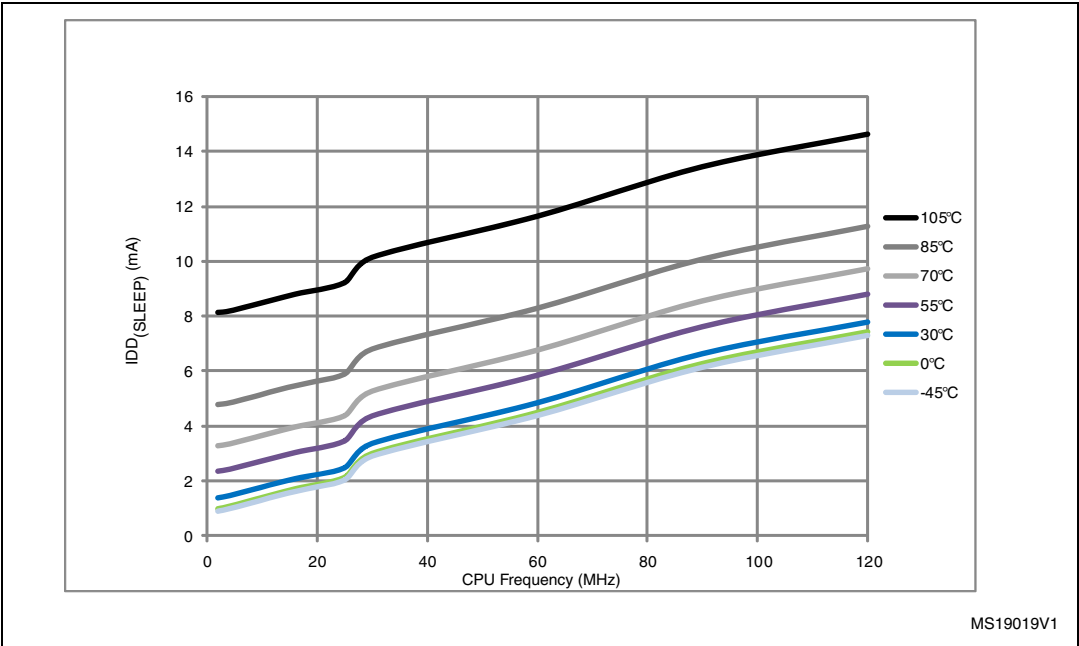


Table 26. Peripheral current consumption (continued)

Peripheral ⁽¹⁾		Typical consumption at 25 °C	Unit
APB2	SDIO	0.69	mA
	TIM1	1.06	
	TIM8	1.03	
	TIM9	0.58	
	TIM10	0.37	
	TIM11	0.39	
	ADC1 ⁽⁴⁾	2.13	
	ADC2 ⁽⁴⁾	2.04	
	ADC3 ⁽⁴⁾	2.12	
	SPI1	1.20	
	USART1	0.38	
	USART6	0.37	

1. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
2. EN1 bit is set in DAC_CR register.
3. EN2 bit is set in DAC_CR register.
4. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

6.3.7 Wakeup time from low-power mode

The wakeup times given in [Table 27](#) is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep mode	-	1	-	μs
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode (regulator in Run mode)	-	13	-	μs
	Wakeup from Stop mode (regulator in low-power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}^{(2)(3)}$	Wakeup from Standby mode	260	375	480	μs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and -45 °C, respectively.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 42: EMI characteristics](#)). It is available only on the main PLL.

Table 36. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = \text{round}[f_{PLL_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If $f_{PLL_IN} = 1$ MHz and $f_{MOD} = 1$ kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = \text{round}[(2^{15} - 1) \times md \times PLLN] / (100 \times 5 \times MODEPER)$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ± 2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = \text{round}[(2^{15} - 1) \times 2 \times 240] / (100 \times 5 \times 250) = 126md(\text{quantitized})\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODEPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{\text{quantized}}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%(\text{peak})$$

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in [Table 45](#).

Table 45. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	–0	NA	mA
	Injected current on NRST pin	–0	NA	
	Injected current on TTa pins: PA4 and PA5	–0	+5	
	Injected current on all FT pins	–5	NA	

1. NA stands for “not applicable”.

Note: *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

Table 46. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	k Ω
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor ⁽⁷⁾	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
$C_{IO}^{(8)}$	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design, not tested in production.
2. Guaranteed by tests in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to [Table 45: I/O current injection susceptibility](#)
5. To sustain a voltage higher than $V_{DD} + 0.3$ V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 45: I/O current injection susceptibility](#)
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in [Figure 38](#).

Figure 42. SPI timing diagram - slave mode and CPHA = 0

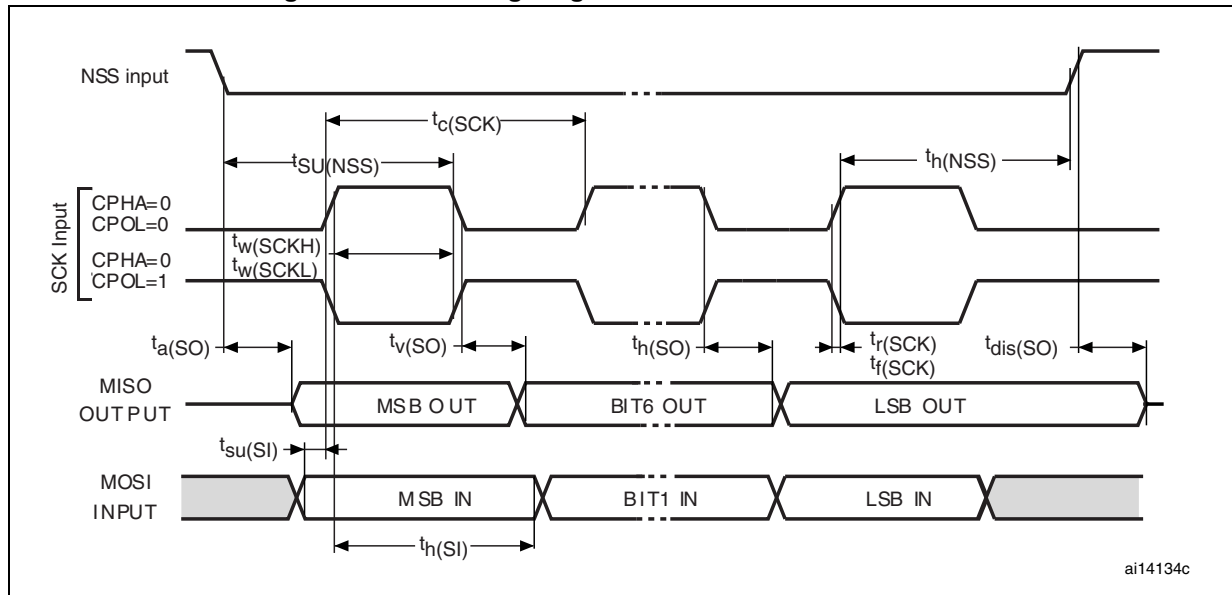
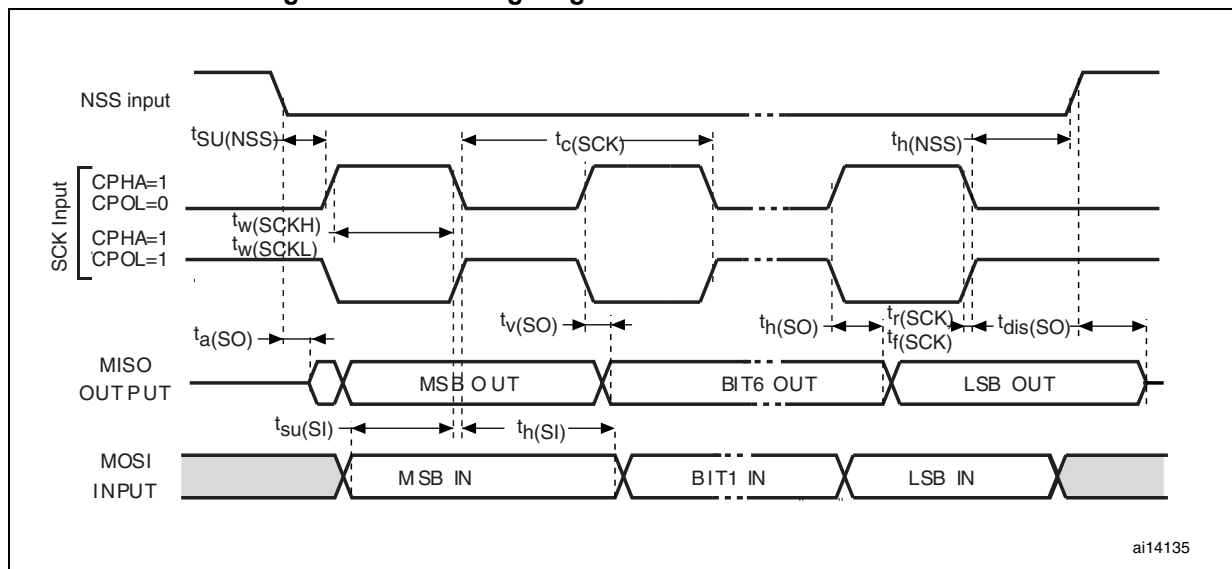


Figure 43. SPI timing diagram - slave mode and CPHA = 1



USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 56. USB OTG FS startup time

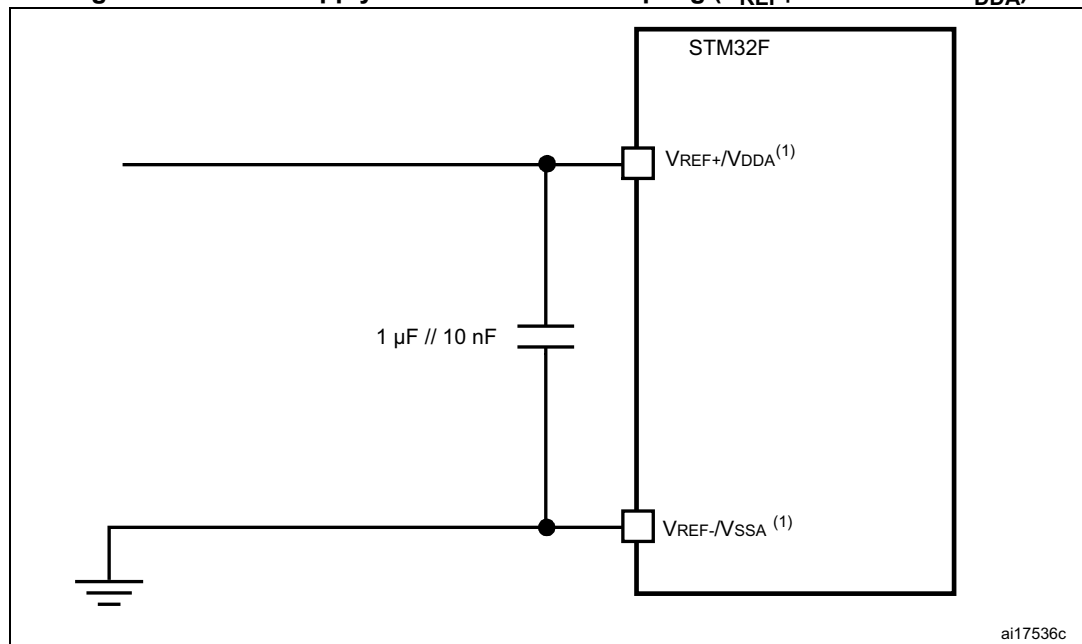
Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB OTG FS transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

Table 57. USB OTG FS DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾	Typ.	Max. ⁽¹⁾	Unit
Input levels	V_{DD}	USB OTG FS operating voltage	3.0 ⁽²⁾	-	3.6	V
	$V_{\text{DI}}^{(3)}$	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	-	-	V
	$V_{\text{CM}}^{(3)}$	Differential common mode range	Includes V_{DI} range	-	2.5	
	$V_{\text{SE}}^{(3)}$	Single ended receiver threshold		-	2.0	
Output levels	V_{OL}	Static output level low	R_{L} of 1.5 k Ω to 3.6 V ⁽⁴⁾	-	0.3	V
	V_{OH}	Static output level high	R_{L} of 15 k Ω to $V_{\text{SS}}^{(4)}$	-	3.6	
R_{PD}	PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{\text{IN}} = V_{\text{DD}}$	17	21	24	k Ω
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}	PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{\text{IN}} = V_{\text{SS}}$	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{\text{IN}} = V_{\text{SS}}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_{L} is the load connected on the USB OTG FS drivers

Figure 55. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

6.3.21 DAC electrical characteristics

Table 68. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8 ⁽¹⁾	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.8 ⁽¹⁾	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
$R_{LOAD}^{(2)}$	Resistive load with buffer ON	5	-	-	k Ω	-
$R_O^{(2)}$	Impedance output with buffer OFF	-	-	15	k Ω	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
$C_{LOAD}^{(2)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x1C7) to (0xE38) at $V_{REF+} = 1.8$ V
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	

Table 81. Switching characteristics for PC Card/CF read and write cycles in I/O space⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK} - 0.5$	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK} - 1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK} - 3$	-	ns
$t_{d(NCE4_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK} + 1.5$	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK} + 1$	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD valid	$5T_{HCLK} - 0.5$	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK} + 1$	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 71 through Figure 74 represent synchronous waveforms, together with Table 82 and Table 83 provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 76. SD default mode

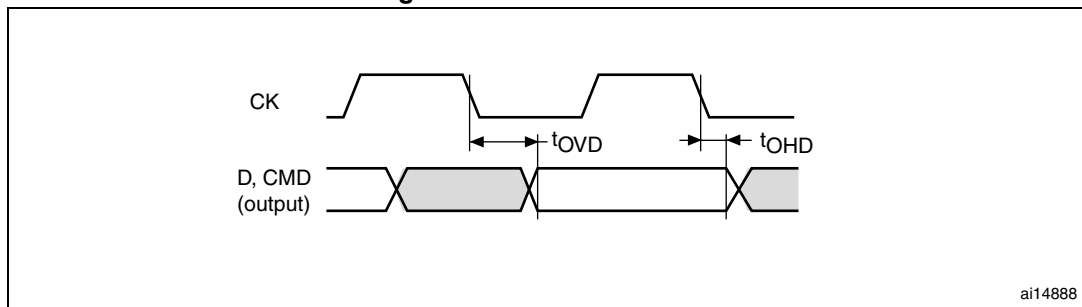


Table 85. SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f _{PP}	Clock frequency in data transfer mode	C _L ≤ 30 pF	0	48	MHz
-	SDIO_CK/f _{PCLK2} frequency ratio	-	-	8/3	-
t _{W(CKL)}	Clock low time, f _{PP} = 16 MHz	C _L ≤ 30 pF	32	-	ns
t _{W(CKH)}	Clock high time, f _{PP} = 16 MHz	C _L ≤ 30 pF	31	-	
t _r	Clock rise time	C _L ≤ 30 pF	-	3.5	
t _f	Clock fall time	C _L ≤ 30 pF	-	5	
CMD, D inputs (referenced to CK)					
t _{ISU}	Input setup time	C _L ≤ 30 pF	2	-	ns
t _{IH}	Input hold time	C _L ≤ 30 pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t _{OV}	Output valid time	C _L ≤ 30 pF	-	6	ns
t _{OH}	Output hold time	C _L ≤ 30 pF	0.3	-	
CMD, D outputs (referenced to CK) in SD default mode ⁽¹⁾					
t _{OVD}	Output valid default time	C _L ≤ 30 pF	-	7	ns
t _{OHD}	Output hold default time	C _L ≤ 30 pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

6.3.28 RTC characteristics

Table 86. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Table 97. Document revision history (continued)

Date	Revision	Changes
25-Nov-2010	5	<p>Update I/Os in Section : Features.</p> <p>Added WLCSP64+2 package. Added note 1 related to LQFP176 on cover page.</p> <p>Added trademark for ART accelerator. Updated Section 3.2: Adaptive real-time memory accelerator (ART Accelerator™).</p> <p>Updated Figure 5: Multi-AHB matrix.</p> <p>Added case of BOR inactivation using IRROFF on WLCSP devices in Section 3.15: Power supply supervisor.</p> <p>Reworked Section 3.16: Voltage regulator to clarify regulator off modes. Renamed PDROFF, IRROFF in the whole document.</p> <p>Added Section 3.19: VBAT operation.</p> <p>Updated LIN and IrDA features for UART4/5 in Table 6: USART feature comparison.</p> <p>Table 8: STM32F20x pin and ball definitions: Modified V_{DD_3} pin, and added note related to the FSMC_NL pin; renamed BYPASS-REG REGOFF, and add IRROFF pin; renamed USART4/5 UART4/5. USART4 pins renamed UART4.</p> <p>Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use.</p> <p>Updated maximum HSE crystal frequency to 26 MHz.</p> <p>Section 6.2: Absolute maximum ratings: Updated V_{IN} minimum and maximum values and note related to five-volt tolerant inputs in Table 11: Voltage characteristics. Updated I_{INJ(PIN)} maximum values and related notes in Table 12: Current characteristics.</p> <p>Updated V_{DDA} minimum value in Table 14: General operating conditions.</p> <p>Added Note 2 and updated Maximum CPU frequency in Table 15: Limitations depending on the operating power supply range, and added Figure 21: Number of wait states versus fCPU and VDD range.</p> <p>Added brownout level 1, 2, and 3 thresholds in Table 19: Embedded reset and power control block characteristics.</p> <p>Changed f_{OSC_IN} maximum value in Table 30: HSE 4-26 MHz oscillator characteristics.</p> <p>Changed f_{PLL_IN} maximum value in Table 34: Main PLL characteristics, and updated jitter parameters in Table 35: PLLI2S (audio PLL) characteristics.</p> <p>Section 6.3.16: I/O port characteristics: updated V_{IH} and V_{IL} in Table 48: I/O AC characteristics.</p> <p>Added Note 1 below Table 47: Output voltage characteristics.</p> <p>Updated R_{PD} and R_{PU} parameter description in Table 57: USB OTG FS DC electrical characteristics.</p> <p>Updated V_{REF+} minimum value in Table 66: ADC characteristics.</p> <p>Updated Table 71: Embedded internal reference voltage.</p> <p>Removed Ethernet and USB2 for 64-pin devices in Table 101: Main applications versus package for STM32F2xxx microcontrollers.</p> <p>Added A.2: USB OTG full speed (FS) interface solutions, removed “OTG FS connection with external PHY” figure, updated Figure 87, Figure 88, and Figure 90 to add STULPI01B.</p>

Table 97. Document revision history (continued)

Date	Revision	Changes
14-Jun-2011	7	<p>Added SDIO in Table 2: STM32F205xx features and peripheral counts.</p> <p>Updated V_{IN} for 5V tolerant pins in Table 11: Voltage characteristics.</p> <p>Updated jitter parameters description in Table 34: Main PLL characteristics.</p> <p>Remove jitter values for system clock in Table 35: PLLI2S (audio PLL) characteristics.</p> <p>Updated Table 42: EMI characteristics.</p> <p>Update Note 2 in Table 52: I2C characteristics.</p> <p>Updated Avg_Slope typical value and T_{S_temp} minimum value in Table 69: Temperature sensor characteristics.</p> <p>Updated T_{S_vbat} minimum value in Table 70: VBAT monitoring characteristics.</p> <p>Updated $T_{S_vrefint}$ minimum value in Table 71: Embedded internal reference voltage.</p> <p>Added Software option in Section 8: Part numbering.</p> <p>In Table 101: Main applications versus package for STM32F2xxx microcontrollers, renamed USB1 and USB2, USB OTG FS and USB OTG HS, respectively; and removed USB OTG FS and camera interface for 64-pin package; added USB OTG HS on 64-pin package; added Note 1 and Note 2.</p>
20-Dec-2011	8	<p>Updated SDIO register addresses in Figure 16: Memory map.</p> <p>Updated Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package, Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package, Figure 1: Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package, and added Figure 4: Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package.</p> <p>Updated Section 3.3: Memory protection unit.</p> <p>Updated Section 3.6: Embedded SRAM.</p> <p>Updated Section 3.28: Universal serial bus on-the-go full-speed (OTG_FS) to remove external FS OTG PHY support.</p> <p>In Table 8: STM32F20x pin and ball definitions: changed SPI2_MCK and SPI3_MCK to I2S2_MCK and I2S3_MCK, respectively. Added ETH_RMII_TX_EN alternate function to PG11. Added EVENTOUT in the list of alternate functions for I/O pin/balls. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions.</p> <p>In Table 10: Alternate function mapping: changed I2S3_SCK to I2S3_MCK for PC7/AF6, added FSMC_NCE3 for PG9, FSMC_NE3 for PG10, and FSMC_NCE2 for PD7. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. Changed I2S3_SCK into I2S3_MCK for PC7/AF6. Updated peripherals corresponding to AF12.</p> <p>Removed CEXT and ESR from Table 14: General operating conditions.</p>

Table 97. Document revision history (continued)

Date	Revision	Changes
29-Oct-2012	10 (continued)	<p>Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in Table 76: Synchronous multiplexed NOR/PSRAM read timings, Table 78: Synchronous non-multiplexed NOR/PSRAM read timings, Figure 61: Synchronous multiplexed NOR/PSRAM read timings and Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings.</p> <p>Added Figure 87: LQFP176 recommended footprint.</p> <p>Added Note 2 below Figure 86: Regulator OFF/internal reset ON.</p> <p>Updated device subfamily in Table 96: Ordering information scheme.</p> <p>Remove reference to note 2 for USB IOTG FS in Table 101: Main applications versus package for STM32F2xxx microcontrollers.</p>