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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207igt6

3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

The devices embed a dedicate PLL (PLLI2S) which allow to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

3.14 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates

3.20 Timers and watchdogs

The STM32F20x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	30 MHz	60 MHz
General purpose	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	60 MHz	120 MHz
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	60 MHz	120 MHz
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	30 MHz	60 MHz
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	30 MHz	60 MHz

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

3.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.31 Digital camera interface (DCMI)

The camera interface is not available in STM32F205xx devices.

STM32F207xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.32 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

3.33 GPIOs (general-purpose inputs/outputs)

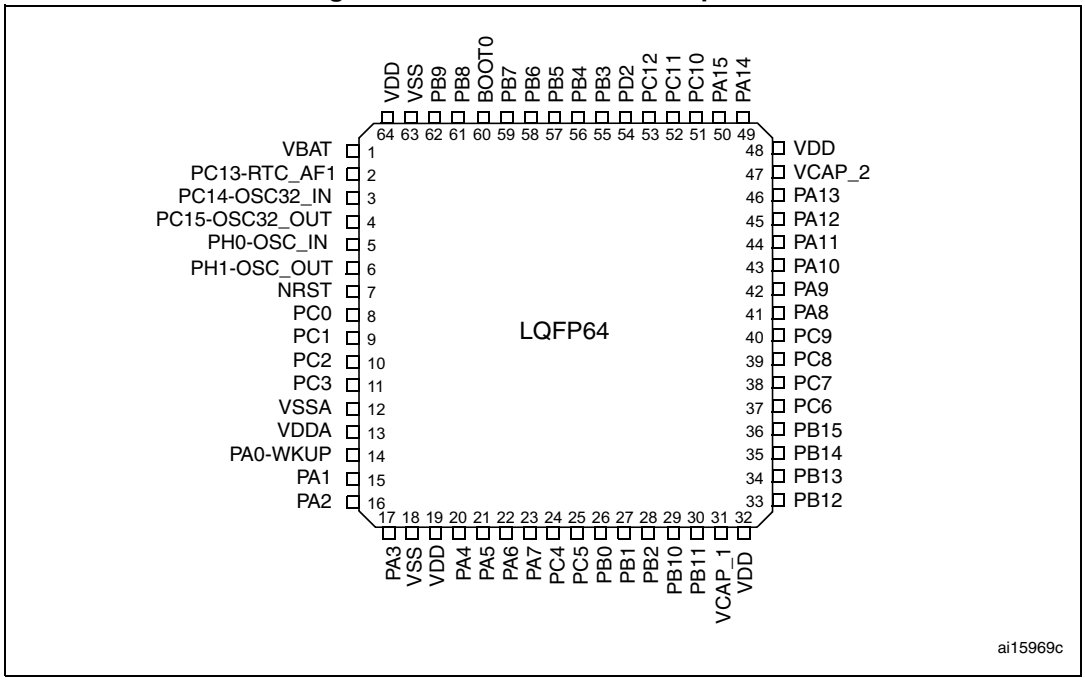
Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

4 Pinouts and pin description

Figure 10. STM32F20x LQFP64 pinout



1. The above figure shows the package top view.

Figure 11. STM32F20x WLCSP64+2 ballout

	1	2	3	4	5	6	7	8	9
A	PA14	PA15	PC12	PB3	PB5	PB7	PB9	VDD	V_{BAT}
B	VSS	PA13	PC10	PB4	PB6	BOOT0	PB8	PC13	PC14
C	PA12	VCAP_2	PC11				PD2	IRROFF	PC15
D	PC9	PA11	PA10				PC2	VSS	VDD
E	VDD	PA8	PA9				PA0	NRST	PH0-OSC_IN
F	VSS	PC7	PC8				VREF+	PC1	PH1-OSC_OUT
G	PB15	PC6	PC5				PA3	PC3	PC0
H	PB14	PB13	PB10	PC4	PA6	PA5	REGOFF	PA1	VSS_5
J	PB12	PB11	VCAP_1	PB2	PB1	PB0	PA7	PA4	PA2

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1. The above figure shows the package top view.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	14	20	J3	PF4	I/O	FT	(4)	FSMC_A4, EVENTOUT	ADC3_IN14
-	-	-	15	21	K3	PF5	I/O	FT	(4)	FSMC_A5, EVENTOUT	ADC3_IN15
-	H9	10	16	22	G2	V_{SS}	S	-	-	-	-
-	-	11	17	23	G3	V_{DD}	S	-	-	-	-
-	-	-	18	24	K2	PF6	I/O	FT	(4)	TIM10_CH1, FSMC_NIORD, EVENTOUT	ADC3_IN4
-	-	-	19	25	K1	PF7	I/O	FT	(4)	TIM11_CH1,FSMC_NREG, EVENTOUT	ADC3_IN5
-	-	-	20	26	L3	PF8	I/O	FT	(4)	TIM13_CH1, FSMC_NIOWR, EVENTOUT	ADC3_IN6
-	-	-	21	27	L2	PF9	I/O	FT	(4)	TIM14_CH1, FSMC_CD, EVENTOUT	ADC3_IN7
-	-	-	22	28	L1	PF10	I/O	FT	(4)	FSMC_INTR, EVENTOUT	ADC3_IN8
5	E9	12	23	29	G1	PH0/OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN(4)
6	F9	13	24	30	H1	PH1/OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT(4)
7	E8	14	25	31	J1	NRST	I/O		-	-	-
8	G9	15	26	32	M2	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP, EVENTOUT	ADC123_ IN10
9	F8	16	27	33	M3	PC1	I/O	FT	(4)	ETH_MDC, EVENTOUT	ADC123_ IN11
10	D7	17	28	34	M4	PC2	I/O	FT	(4)	SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, EVENTOUT	ADC123_ IN12
11	G8	18	29	35	M5	PC3	I/O	FT	(4)	SPI2_MOSI, I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, EVENTOUT	ADC123_ IN13
-	-	19	30	36	-	V_{DD}	S	-	-	-	-
12	-	20	31	37	M1	V_{SSA}	S	-	-	-	-
-	-	-	-	-	N1	V_{REF-}	S	-	-	-	-
-	F7	21	32	38	P1	V_{REF+}	S	-	-	-	-

Table 8. STM32F20x pin and ball definitions (continued)

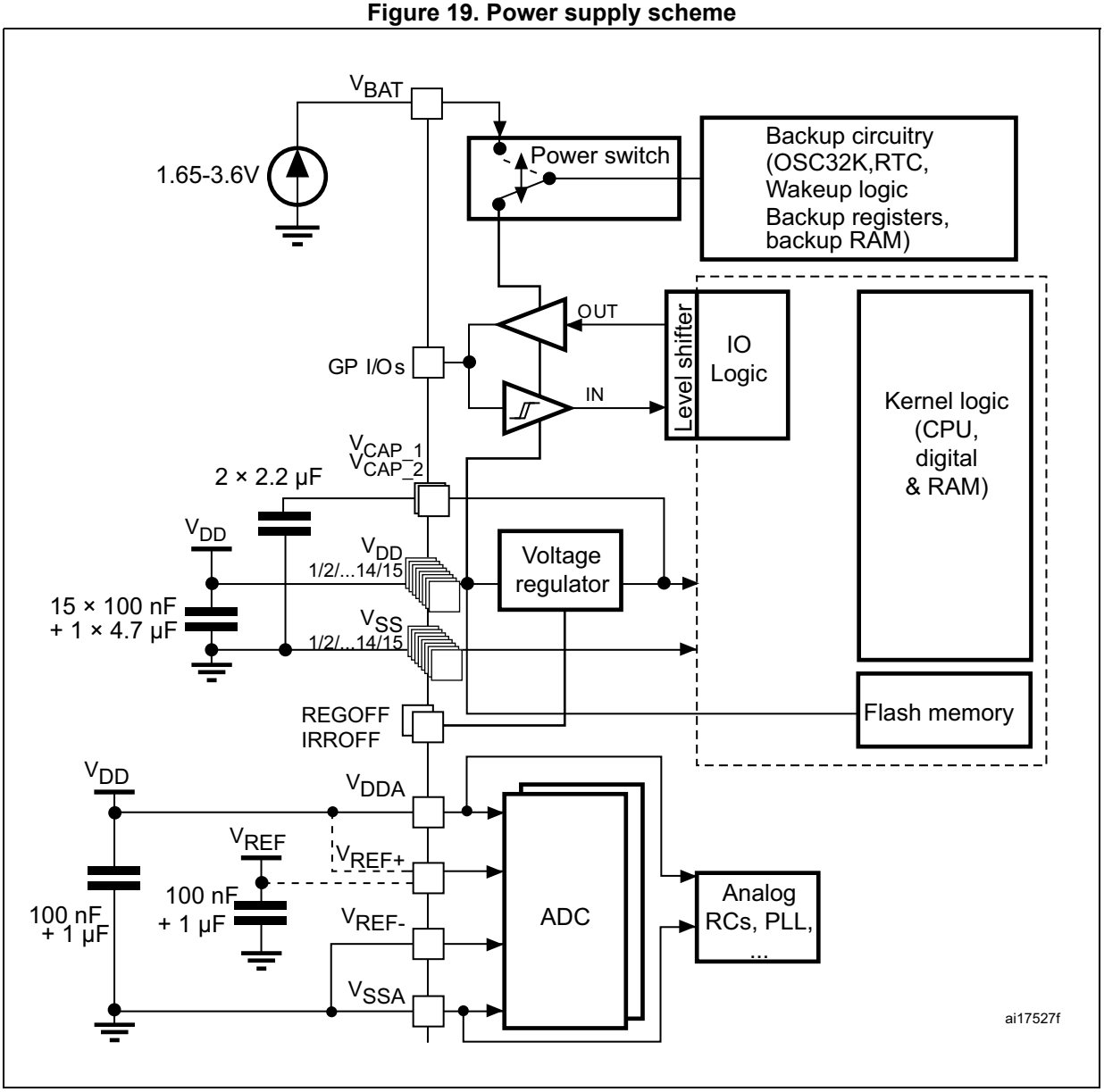
Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
13	-	22	33	39	R1	V_{DDA}	S	-	-	-	-
14	E7	23	34	40	N3	PA0-WKUP (PA0)	I/O	FT	(4)(5)	USART2_CTS, UART4_TX, ETH_MII_CRS, TIM2_CH1_ETR, TIM5_CH1, TIM8_ETR, EVENTOUT	ADC123_IN0, WKUP
15	H8	24	35	41	N2	PA1	I/O	FT	(4)	USART2_RTS, UART4_RX, ETH_RMII_REF_CLK, ETH_MII_RX_CLK, TIM5_CH2, TIM2_CH2, EVENTOUT	ADC123_IN1
16	J9	25	36	42	P2	PA2	I/O	FT	(4)	USART2_TX,TIM5_CH3, TIM9_CH1, TIM2_CH3, ETH_MDIO, EVENTOUT	ADC123_IN2
-	-	-	-	43	F4	PH2	I/O	FT	-	ETH_MII_CRS, EVENTOUT	-
-	-	-	-	44	G4	PH3	I/O	FT	-	ETH_MII_COL, EVENTOUT	-
-	-	-	-	45	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	-	46	J4	PH5	I/O	FT	-	I2C2_SDA, EVENTOUT	-
17	G7	26	37	47	R2	PA3	I/O	FT	(4)	USART2_RX, TIM5_CH4, TIM9_CH2, TIM2_CH4, OTG_HS_ULPI_D0, ETH_MII_COL, EVENTOUT	ADC123_IN3
18	F1	27	38	48	-	V_{SS}	S	-	-	-	-
	H7				L4	REGOFF	I/O	-	-	-	-
19	E1	28	39	49	K4	V_{DD}	S	-	-	-	-
20	J8	29	40	50	N4	PA4	I/O	TTa	(4)	SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC, OTG_HS_SOF, I2S3_WS, EVENTOUT	ADC12_IN4, DAC_OUT1
21	H6	30	41	51	P4	PA5	I/O	TTa	(4)	SPI1_SCK, OTG_HS_ULPI_CK, TIM2_CH1_ETR, TIM8_CH1N, EVENTOUT	ADC12_IN5, DAC_OUT2

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
54	C7	83	116	144	D12	PD2	I/O	FT	-	TIM3_ETR,UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	-	84	117	145	D11	PD3	I/O	FT	-	FSMC_CLK,USART2_CTS, EVENTOUT	-
-	-	85	118	146	D10	PD4	I/O	FT	-	FSMC_NOE, USART2_RTS, EVENTOUT	-
-	-	86	119	147	C11	PD5	I/O	FT	-	FSMC_NWE,USART2_TX, EVENTOUT	-
-	-	-	120	148	D8	V_{SS}	S	-	-	-	-
-	-	-	121	149	C8	V_{DD}	S	-	-	-	-
-	-	87	122	150	B11	PD6	I/O	FT	-	FSMC_NWAIT, USART2_RX, EVENTOUT	-
-	-	88	123	151	A11	PD7	I/O	FT	-	USART2_CK,FSMC_NE1, FSMC_NCE2, EVENTOUT	-
-	-	-	124	152	C10	PG9	I/O	FT	-	USART6_RX, FSMC_NE2,FSMC_NCE3, EVENTOUT	-
-	-	-	125	153	B10	PG10	I/O	FT	-	FSMC_NCE4_1, FSMC_NE3, EVENTOUT	-
-	-	-	126	154	B9	PG11	I/O	FT	-	FSMC_NCE4_2, ETH_MII_TX_EN , ETH _RMII_TX_EN, EVENTOUT	-
-	-	-	127	155	B8	PG12	I/O	FT	-	FSMC_NE4, USART6_RTS, EVENTOUT	-
-	-	-	128	156	A8	PG13	I/O	FT	-	FSMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-
-	-	-	129	157	A7	PG14	I/O	FT	-	FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT	-
-	-	-	130	158	D7	V_{SS}	S	-	-	-	-

6.1.6 Power supply scheme

Figure 19. Power supply scheme

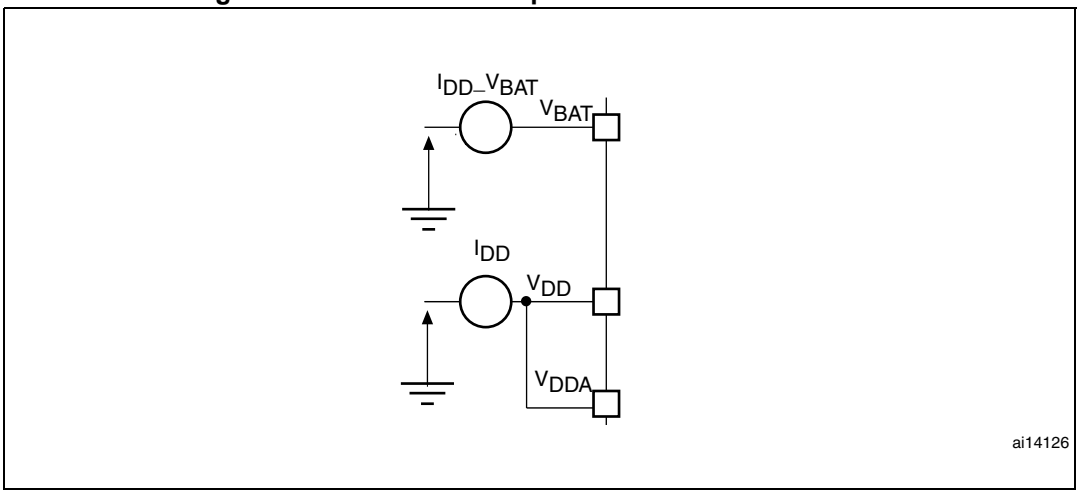


1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect REGOFF and IRROFF pins, refer to *Section 3.16: Voltage regulator*.
3. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
4. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB, to ensure good device operation. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect device operation.

6.1.7 Current consumption measurement

Figure 20. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 12* for the values of the maximum allowed injected current.

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8(1)	3.6	V
V_{DDA}(2)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(3)	1.8(1)	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	5.5	
		1.7 V ≤ V_{DD} ≤ 2 V	–0.3	5.2	
	Input voltage on TTa pins	-	–0.3	V_{DD}+0.3	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP64	-	444	mW
		WLCSP64+2	-	392	
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	Reset temporization	-	0.5	1.5	3.0	ms
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design, not tested in production.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

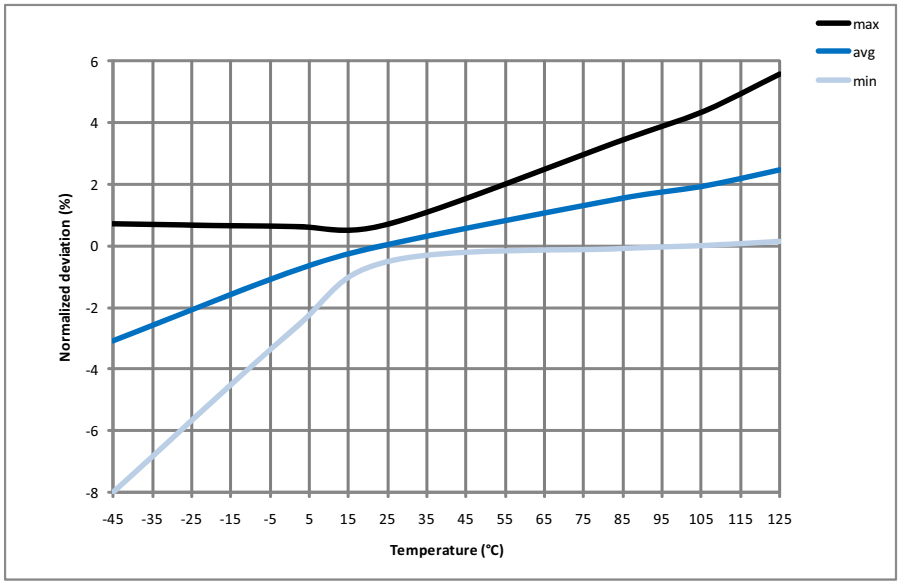
6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 20: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using CoreMark code.

Figure 34. ACC_{HSI} versus temperature



Low-speed internal (LSI) RC oscillator

Table 33. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC® code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 42. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/120 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, peripheral clock disabled	0.1 to 30 MHz	25	dBµV
			30 to 130 MHz		
			130 MHz to 1GHz		
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, PLL spread spectrum enabled, peripheral clock disabled	0.1 to 30 MHz	28	dBµV
			30 to 130 MHz	26	
			130 MHz to 1GHz	22	
			SAE EMI level	4	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Guaranteed by characterization results, not tested in production.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 14: General operating conditions*.

All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04^{(1)}$ $0.3V_{DD}^{(2)}$	V
	BOOT0 I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	-	$0.1V_{DD}+0.1^{(1)}$	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3^{(1)}$ $0.7V_{DD}^{(2)}$	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7^{(1)}$	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3^{(1)}$	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$10\%V_{DDIO}^{(1)(3)}$	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	$100^{(1)}$	-	-	
I_{lkg}	I/O input leakage current (4)	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)	V_{IN} = 5 V	-	-	3	

Table 51. Characteristics of TIMx connected to the APB2 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB2 prescaler distinct from 1, $f_{TIMxCLK}$ = 120 MHz	1	-	$t_{TIMxCLK}$
			8.3	-	ns
		AHB/APB2 prescaler = 1, $f_{TIMxCLK}$ = 60 MHz	1	-	$t_{TIMxCLK}$
			16.7	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 120 MHz APB2 = 60 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	60	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0083	546	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	35.79	s

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.

6.3.19 Communications interfaces

I^2C interface characteristics

STM32F205xx and STM32F207xx I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 52*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 56. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 57. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Table 74. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 60. Asynchronous multiplexed PSRAM/NOR write waveforms

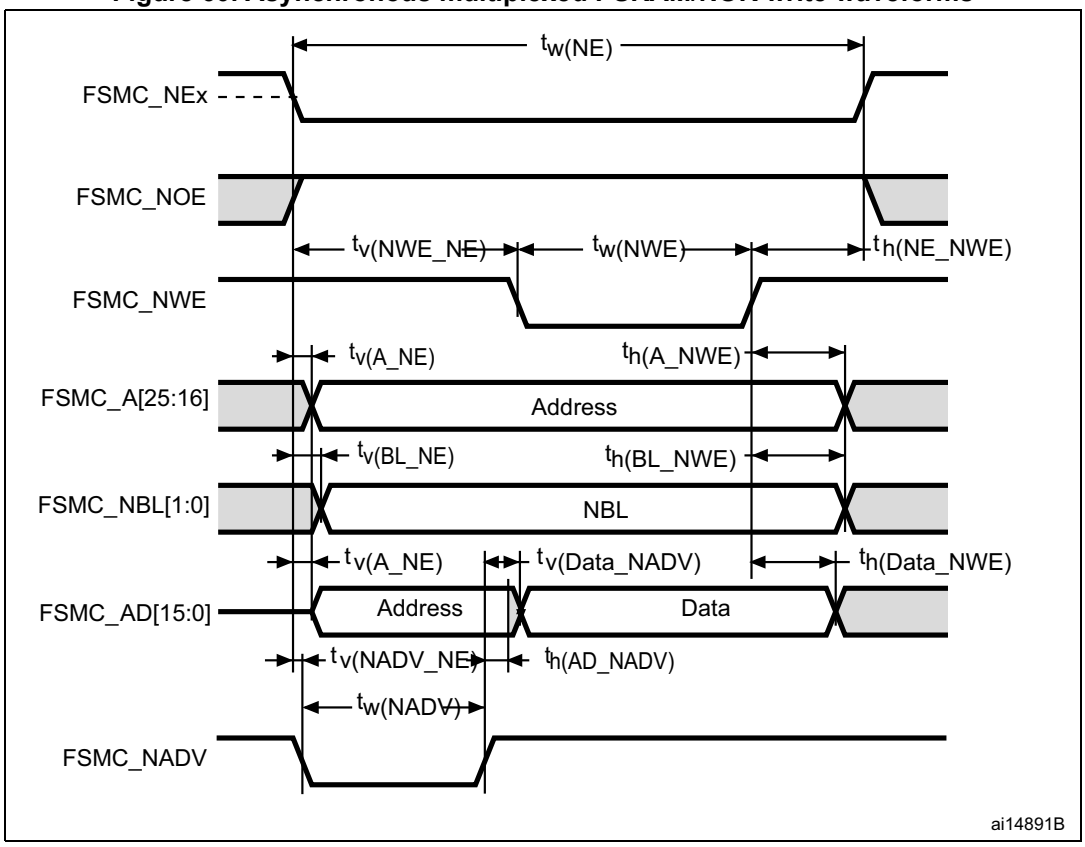
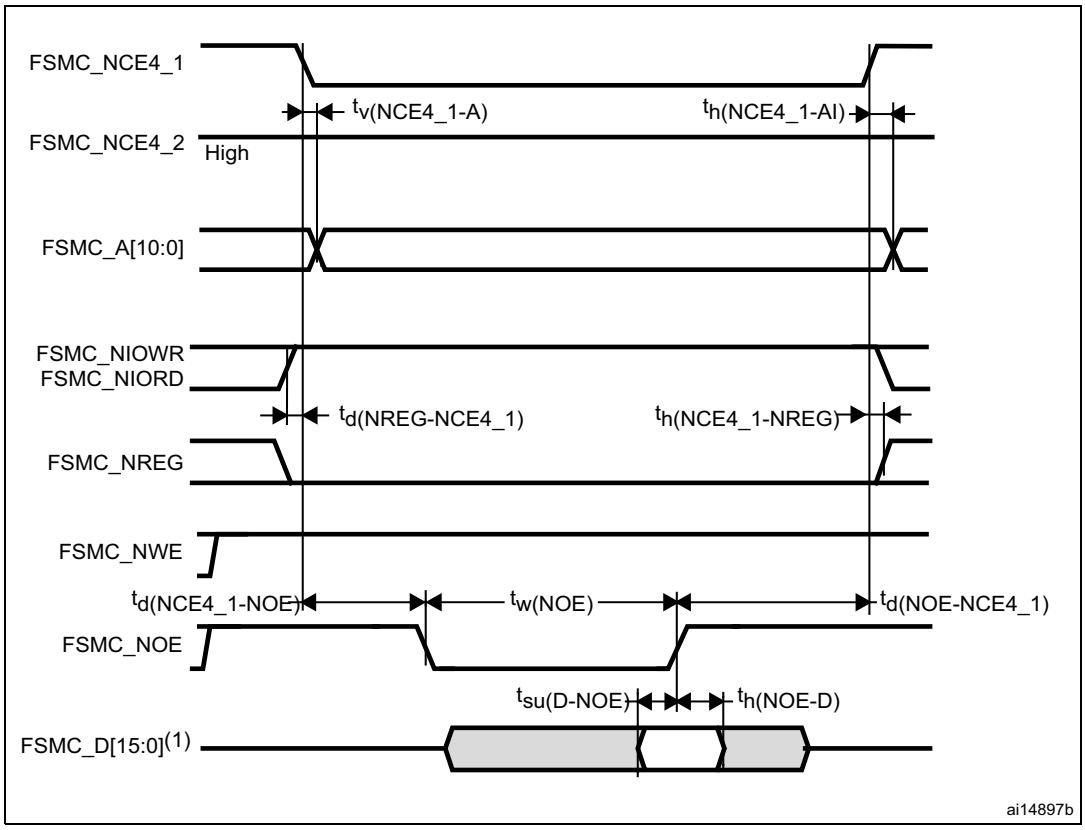


Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4T_{HCLK}$-1	$4T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}- 1	T_{HCLK}	ns
$t_{w(NWE)}$	FSMC_NWE low tim e	$2T_{HCLK}$	$2T_{HCLK}$+1	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}- 1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 2	T_{HCLK}+ 2	ns
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	ns

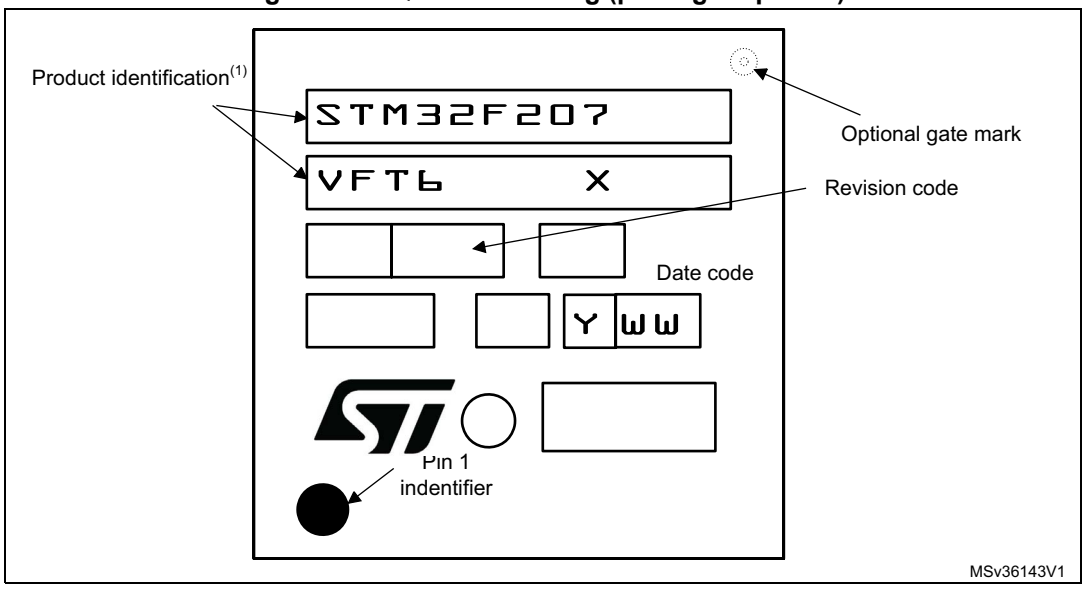
Figure 67. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Device marking

Figure 83. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Updated *Typical and maximum current consumption* conditions, as well as *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure 23*, *Figure 24*, *Figure 25*, and *Figure 26*. Updated *Table 22: Typical and maximum current consumption in Sleep mode*, and added *Figure 27* and *Figure 28*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Added *Figure 29: Typical current consumption vs. temperature in Stop mode*. Updated *Table 24: Typical and maximum current consumptions in Standby mode* and *Table 25: Typical and maximum current consumptions in VBAT mode*. Updated *On-chip peripheral current consumption* conditions and *Table 26: Peripheral current consumption*. Updated $t_{WUSTDBY}$ and t_{WUSTOP}, and added *Note 3* in *Table 27: Low-power mode wakeup timings*. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in *Table 28: High-speed external user clock characteristics*. Updated C and g_m in *Table 30: HSE 4-26 MHz oscillator characteristics*. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in *Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added *Note 1* and updated ACC_{HSI}, $IDD_{(HSI}$, and $t_{su(HSI)}$ in *Table 32: HSI oscillator characteristics*. Added *Figure 34: ACCHSI versus temperature*. Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in *Table 33: LSI oscillator characteristics*. Added *Figure 35: ACCLSI versus temperature* *Table 34: Main PLL characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added *Note 2* for f_{PLL_IN} minimum and maximum values. *Table 35: PLLI2S (audio PLL) characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added *Note 2* for f_{PLLI2S_IN} minimum and maximum values. Added *Note 1* in *Table 36: SSCG parameters constraint*. Updated *Table 37: Flash memory characteristics*. Modified *Table 38: Flash memory programming* and added *Note 2* for t_{prog}. Updated t_{prog} and added *Note 1* in *Table 39: Flash memory programming with VPP*. Modified *Figure 40: Recommended NRST pin protection*. Updated *Table 42: EMI characteristics* and EMI monitoring conditions in *Section : Electromagnetic Interference (EMI)*. Added *Note 2* related to $V_{ESD(HBM)}$in *Table 43: ESD absolute maximum ratings*. Updated *Table 48: I/O AC characteristics*. Added *Section 6.3.15: I/O current injection characteristics*. Modified maximum frequency values and conditions in *Table 48: I/O AC characteristics*. Updated $t_{res(TIM)}$ in *Table 50: Characteristics of TIMx connected to the APB1 domain*. Modified $t_{res(TIM)}$ and f_{EXT} *Table 51: Characteristics of TIMx connected to the APB2 domain*.