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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Det	ails
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Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207vct7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 Description

The STM32F20x family is based on the high-performance ARM[®] Cortex[®]-M3 32-bit RISC core operating at a frequency of up to 120 MHz. The family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 128 Kbytes of system SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator[™]) which allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz. This performance has been validated using the CoreMark benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true number random generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), and a camera interface for CMOS sensors. The devices also feature standard peripherals.

- Up to three I²Cs
- Three SPIs, two I²Ss. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external PLL to allow synchronization.
- 4 USARTs and 2 UARTs
- A USB OTG high-speed with full-speed capability (with the ULPI)
- A second USB OTG (full-speed)
- Two CANs
- An SDIO interface
- Ethernet and camera interface available on STM32F207xx devices only.

Note: The STM32F205xx and STM32F207xx devices operate in the -40 to +105 °C temperature range from a 1.8 V to 3.6 V power supply. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD} , the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see Section 3.16).

A comprehensive set of power-saving modes allow the design of low-power applications.

STM32F205xx and STM32F207xx devices are offered in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen. These features make the STM32F205xx and STM32F207xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.



There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes

The LP regulator mode is configured by software when entering Stop mode.

• Power-down is used in Standby mode.

The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP 1} and V_{CAP 2} pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS}. On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP 1} and V_{CAP 2} pins, in addition to V_{DD}.



3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

	Table 4. Regulator On/OFF and internal reset On/OFF availability							
Package	Regulator ON/internal reset ON	Regulator OFF/internal reset ON	Regulator OFF/internal reset OFF					
LQFP64 LQFP100 LQFP144 LQFP176	Yes	No	No					
WLCSP 64+2	Yes REGOFF and IRROFF set to V _{SS}	Yes REGOFF set to V _{DD} and IRROFF set to V _{SS}	Yes REGOFF set to V _{SS} and IRROFF set to V _{DD}					
UFBGA176	Yes REGOFF set to V _{SS}	Yes REGOFF set to V _{DD}	No					

 Table 4. Regulator ON/OFF and internal reset ON/OFF availability

3.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F20x devices includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Its main features are the following:

- Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.
- It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal lowpower RC oscillator or the high-speed external clock divided by 128. The internal lowspeed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.
- Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.
- A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The 4-Kbyte backup SRAM is an EEPROM-like area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled to minimize power consumption (see *Section 3.18: Low-power modes*). It can be enabled by software.



3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.20.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.21 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

3.22 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F20x devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
А	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
в	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
с	VBAT	PI7	PI6	PI5	VDD	RFU	VDD	VDD	VDD	PG9	PD5	PD1	PI3	Pl2	PA11
D	PC13- TAMP1	PI8- TAMP2	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
Е	PC14- OSC32_IN	PF0	PI10	PI11								PH13	PH14	P10	PA9
F	PC15- OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP_2	PC9	PA8
G	PH0- OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
н	PH1- OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
к	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	REGOFF								PH11	PH10	PD15	PG2
М	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0- WKUP	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
Ρ	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

Figure 15. STM32F20x UFBGA176 ballout

1. RFU means "reserved for future use". This pin can be tied to $V_{\text{DD}}, V_{\text{SS}}$ or left unconnected.

2. The above figure shows the package top view.

Table 7. Leo	end/abbreviations	used in	the	pinout	table
10.010 11 202				pinoat	

Name	Abbreviation	Definition					
Pin name	Unless otherwise reset is the same	specified in brackets below the pin name, the pin function during and after as the actual pin name					
	S	Supply pin					
Pin type	I	Input only pin					
	I/O	Input/ output pin					
	FT	5 V tolerant I/O					
I/O structure	ТТа	3.3 V tolerant I/O					
NO structure	В	Dedicated BOOT0 pin					
	RST	Bidirectional reset pin with embedded weak pull-up resistor					
Notes	Unless otherwise	specified by a note, all I/Os are set as floating inputs during and after reset					
Alternate functions	Functions selected through GPIOx_AFR registers						
Additional functions	Functions directly	unctions directly selected/enabled through peripheral registers					



		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		
	Port	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	12C1/12C2/12C3	SPI1/SPI2/I2S2	SPI3/I2S3	USART1/2/3	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ЕТН	FSMC/SDIO/ OTG_HS	DCMI	AF014	AF15
	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	-	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_SCK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	-	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	-	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NL	DCMI_VSYNC	-	EVENTOUT
Port B	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	DCMI_D6	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_SCK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0 ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_SCK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1 ETH_RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	-	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_50Hz	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Table 10. Alternate function mapping (continued)

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Figure 23. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals ON

Figure 24. Typical current consumption vs. temperature, Run mode, code with data processing running from RAM, and peripherals OFF







Figure 25. Typical current consumption vs. temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON









Figure 27. Typical current consumption vs. temperature in Sleep mode, peripherals ON

Figure 28. Typical current consumption vs. temperature in Sleep mode, peripherals OFF





			Тур		Мах		
Symbol	Parameter	Conditions	T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	Unit
	Supply current	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.55	1.2	11.00	20.00	
with main regulator in Run mode	with main regulator in Run mode	Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.50	1.2	11.00	20.00	m۸
'DD_STOP	STOP Supply current in Stop mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.35	1.1	8.00	15.00	
	regulator in Low-power mode	Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.30	1.1	8.00	15.00	

Table 23. Typical and maximum current consumptions in Stop mode

Figure 29. Typical current consumption vs. temperature in Stop mode



All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part
of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect
these changes





Figure 35. ACC_{LSI} versus temperature

6.3.10 PLL characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
f _{PLL_IN}	PLL input clock ⁽¹⁾	-	0.95 ⁽²⁾	1	2.10 ⁽²⁾	MHz
f _{PLL_OUT}	PLL multiplier output clock	-	24	-	120	MHz
f _{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	-	48	MHz
f _{VCO_OUT}	PLL VCO output	-	192	-	432	MHz
t	PLL lock time	VCO freq = 192 MHz	75	-	200	116
LOCK		VCO freq = 432 MHz	100	-	300	μο

Table 34. Main PLL characteristics



6.3.18 TIM timer characteristics

The parameters given in *Table 50* and *Table 51* are guaranteed by design.

Refer to Section 6.3.16: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions	Min	Мах	Unit
		AHB/APB1	1	-	t _{TIMxCLK}
t _{res(TIM)}	Timer resolution time	from 1, f _{TIMxCLK} = 60 MHz	16.7	-	ns
		AHB/APB1	1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 30 MHz	33.3	-	ns
feve	Timer external clock		0	f _{TIMxCLK} /2	MHz
'EXT	frequency on CH1 to CH4		0	30	MHz
Res _{TIM}	Timer resolution		-	16/32	bit
	16-bit counter clock period		1	65536	t _{TIMxCLK}
toouware	selected	f _{TIMxCLK} = 60 MHz	0.0167	1092	μs
COUNTER	32-bit counter clock period		1	-	t _{TIMxCLK}
	selected		0.0167	71582788	μs
two count	Maximum possible count		-	65536 × 65536	t _{TIMxCLK}
MAX_COUNT			-	71.6	s

Table 50. Characteristics of TIMx connected to the APB1 domain	¹⁾ ו)
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1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.





Figure 41. I²C bus AC waveforms and measurement circuit

- 1. R_S = series protection resistor.
- 2. R_P = external pull-up resistor.
- 3. $V_{DD_{12C}}$ is the I²C bus power supply.

f (kH=)	I2C_CCR value
ISCL (KIIZ)	R _P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

Table 53. SCL frequency (f_{PCLK1}= 30 MHz., V_{DD} = 3.3 V)⁽¹⁾⁽²⁾

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,

For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.



USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Symbol	Parameter	Мах	Unit		
t _{STARTUP} ⁽¹⁾	USB OTG FS transceiver startup time	1	μs		

Table 56. USB OTG FS startup time

1. Guaranteed by design, not tested in production.

Sym	bol	Parameter	Conditions	Min. ⁽¹⁾	Тур.	Max. ⁽¹⁾	Unit
	V _{DD}	USB OTG FS operating voltage		3.0 ⁽²⁾	-	3.6	V
Input	V _{DI} ⁽³⁾	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	
levels	V _{CM} ⁽³⁾	Differential common mode range	Includes V _{DI} range	0.8	-	2.5	V
	$V_{SE}^{(3)}$	Single ended receiver threshold		1.3	-	2.0	
Output	V _{OL}	Static output level low	$\rm R_L$ of 1.5 k\Omega to 3.6 $\rm V^{(4)}$	-	-	0.3	V
levels	V _{OH}	Static output level high	${\sf R}_{\sf L}$ of 15 k Ω to ${\sf V}_{\sf SS}{}^{(4)}$	2.8	-	3.6	v
R _{PD} R _{PU}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	V _{IN} = V _{DD}	17	21	24	
	2 P	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	kΩ
		PA12, PB15 (USB_FS_DP, USB_HS_DP)	V _{IN} = V _{SS}	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V _{IN} = V _{SS}	0.25	0.37	0.55	-	

Table 57. USB OTG FS DC electrical characteristics

1. All the voltages are measured from the local ground potential.

2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.

3. Guaranteed by design, not tested in production.

4. R_L is the load connected on the USB OTG FS drivers



6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DDA}	Power supply	-	1.8 ⁽¹⁾	-	3.6	V
V _{REF+}	Positive reference voltage	-	1.8 ⁽¹⁾⁽²⁾	-	V _{DDA}	V
4		V_{DDA} = 1.8 ⁽¹⁾ to 2.4 V	0.6	-	15	MHz
'ADC		V _{DDA} = 2.4 to 3.6 V	0.6	-	30	MHz
f _{TRIG} ⁽³⁾	External trigger frequency	f _{ADC} = 30 MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	1/f _{ADC}
V _{AIN}	Conversion voltage range ⁽⁴⁾	-	0 (V _{SSA} or V _{REF-} tied to ground)	-	V_{REF} +	V
R _{AIN} ⁽³⁾	External input impedance	See <i>Equation 1</i> for details	-	-	50	kΩ
$R_{ADC}^{(3)(5)}$	Sampling switch resistance	-	1.5	-	6	kΩ
C _{ADC} ⁽³⁾	Internal sample and hold capacitor	-	-	4	-	pF
+ (3)	Injection trigger conversion latency	f _{ADC} = 30 MHz	-	-	0.100	μs
"Iat"		-	-	-	3 ⁽⁶⁾	1/f _{ADC}
t ₁₋₁ (3)	Regular trigger conversion latency	f _{ADC} = 30 MHz	-	-	0.067	μs
Patr		-	-	-	2 ⁽⁶⁾	1/f _{ADC}
$t_{0}^{(3)}$	Sampling time	f _{ADC} = 30 MHz	0.100	-	16	μs
•5		-	3	-	480	1/f _{ADC}
t _{STAB} ⁽³⁾	Power-up time	-	-	2	3	μs
		f _{ADC} = 30 MHz 12-bit resolution	0.5	-	16.40	μs
t _{conv} (3)		f _{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	μs
	Total conversion time (including sampling time)	f _{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	μs
		f _{ADC} = 30 MHz 6-bit resolution	0.3	-	16.20	μs
		9 to 492 (t _S for sampling +n-bit resolution for successive approximation)				1/f _{ADC}



6.3.23 V_{BAT} monitoring characteristics

Table 70. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Тур	Мах	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V _{BAT} measurement	-	2	-	
Er ⁽¹⁾	Error on Q	–1	-	+1	%
T _{S_vbat} ⁽²⁾⁽²⁾	ADC sampling time when reading the V _{BAT} (1 mV accuracy)	5	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Embedded reference voltage

The parameters given in *Table 71* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{REFINT}	Internal reference voltage	–40 °C < T _A < +105 °C	1.18	1.21	1.24	V
T _{S_vrefint} ⁽¹⁾	ADC sampling time when reading the internal reference voltage	-	10	-	-	μs
V _{RERINT_s}	Internal reference voltage spread over the temperature range	V _{DD} = 3 V	-	3	5	mV
T _{Coeff} ⁽²⁾	Temperature coefficient	-	-	30	50	ppm/°C
t _{START} ⁽²⁾	Startup time	-	_	6	10	μs

Table 71. Embedded internal reference voltage

1. Shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design, not tested in production.

6.3.25 FSMC characteristics

Asynchronous waveforms and timings

Figure 57 through *Figure 60* represent asynchronous waveforms and *Table 72* through *Table 75* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 1
- DataSetupTime = 1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.





Figure 59. Asynchronous multiplexed PSRAM/NOR read waveforms

Table 74. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Мах	Unit
t _{w(NE)}	FSMC_NE low time	3T _{HCLK} -1	3T _{HCLK} +1	ns
t _{v(NOE_NE)}	FSMC_NEx low to FSMC_NOE low	2T _{HCLK}	2T _{HCLK} +0.5	ns
t _{w(NOE)}	FSMC_NOE low time	T _{HCLK} -1	T _{HCLK} +1	ns
t _{h(NE_NOE)}	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
t _{v(A_NE)}	FSMC_NEx low to FSMC_A valid	-	2	ns
t _{v(NADV_NE)}	FSMC_NEx low to FSMC_NADV low	1	2.5	ns
t _{w(NADV)}	FSMC_NADV low time	T _{HCLK} – 1.5	T _{HCLK}	ns
t _{h(AD_NADV)}	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T _{HCLK}	-	ns
t _{h(A_NOE)}	Address hold time after FSMC_NOE high	T _{HCLK}	-	ns
t _{h(BL_NOE)}	FSMC_BL time after FSMC_NOE high	0	-	ns
t _{v(BL_NE)}	FSMC_NEx low to FSMC_BL valid	-	1	ns
t _{su(Data_NE)}	Data to FSMC_NEx high setup time	T _{HCLK} + 2	-	ns
t _{su(Data_NOE)}	Data to FSMC_NOE high setup time	T _{HCLK} + 3	-	ns



			(*******	
Symbol	Parameter	Min	Мах	Unit
t _{su(ADV-CLKH)}	FSMC_A/D[15:0] valid data before FSMC_CLK high	5	-	ns
t _{h(CLKH-ADV)}	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns

Table 76. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.



Figure 62. Synchronous multiplexed PSRAM write timings

Table 77. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Мах	Unit
t _{w(CLK)}	FSMC_CLK period	2T _{HCLK} - 1	-	ns
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x=02)	-	0	ns
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x= 02)	2	-	ns
t _{d(CLKL-NADVL)}	FSMC_CLK low to FSMC_NADV low	-	2	ns
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	3	-	ns
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x=1625)	-	0	ns
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x=1625)	7	-	ns

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Symbol	Parameter	Min	Max	Unit
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	4	-	ns
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x=1625)	-	0	ns
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x=1625)	3	-	ns
t _{d(CLKH-NOEL)}	FSMC_CLK high to FSMC_NOE low	-	1	ns
t _{d(CLKL-NOEH)}	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
t _{su(DV-CLKH)}	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
t _{h(CLKH-DV)}	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.



Figure 64. Synchronous non-multiplexed PSRAM write timings

Table 79. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
t _{w(CLK)}	FSMC_CLK period	2T _{HCLK} - 1	-	ns
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x=02)	-	1	ns
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x= 02)	1	-	ns





Figure 73. NAND controller waveforms for common memory read access

Figure 74. NAND controller waveforms for common memory write access



Table 82. Switching characteristics for NAND Flash read cycles⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
t _{w(N0E)}	FSMC_NOE low width	4T _{HCLK} - 1	4T _{HCLK} + 2	ns
t _{su(D-NOE)}	FSMC_D[15-0] valid data before FSMC_NOE high	9	-	ns
t _{h(NOE-D})	FSMC_D[15-0] valid data after FSMC_NOE high	3	-	ns
t _{d(ALE-NOE)}	FSMC_ALE valid before FSMC_NOE low	-	3T _{HCLK}	ns
t _{h(NOE-ALE)}	FSMC_NWE high to FSMC_ALE invalid	3T _{HCLK} + 2	-	ns

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.

