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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207vgt6

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in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).

- V_{SSA} , V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 19: Power supply scheme](#) for more details.

3.15 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry.

At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit. On devices in WLCSP64+2 package, the BOR, POR and PDR features can be disabled by setting IRROFF pin to V_{DD} . In this mode an external power supply supervisor is required (see [Section 3.16](#)).

The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.16 Voltage regulator

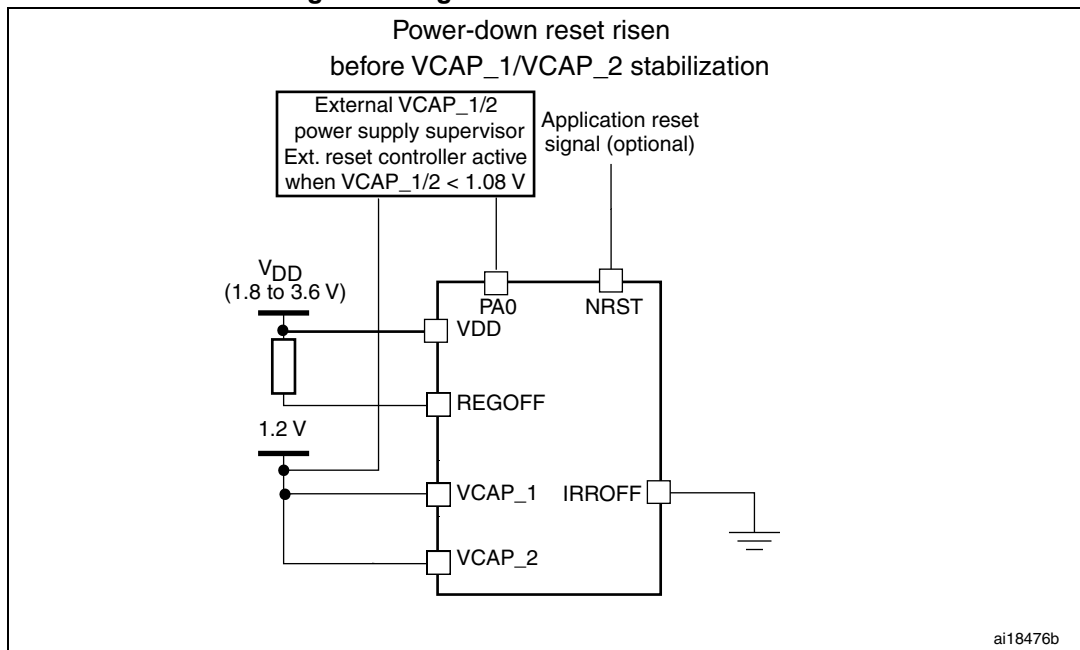
The regulator has five operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low-power regulator (LPR)
 - Power-down
- Regulator OFF
 - Regulator OFF/internal reset ON
 - Regulator OFF/internal reset OFF

3.16.1 Regulator ON

The regulator ON modes are activated by default on LQFP packages. On WLCSP64+2 package, they are activated by connecting both REGOFF and IRROFF pins to V_{SS} , while only REGOFF must be connected to V_{SS} on UFBGA176 package (IRROFF is not available).

V_{DD} minimum value is 1.8 V.

Figure 6. Regulator OFF/internal reset ON

The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see [Figure 8](#)).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see [Figure 9](#)).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD} . IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 3.18: Low-power modes](#)).

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or the V_{BAT} pin.

3.18 Low-power modes

The STM32F20x family supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

3.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

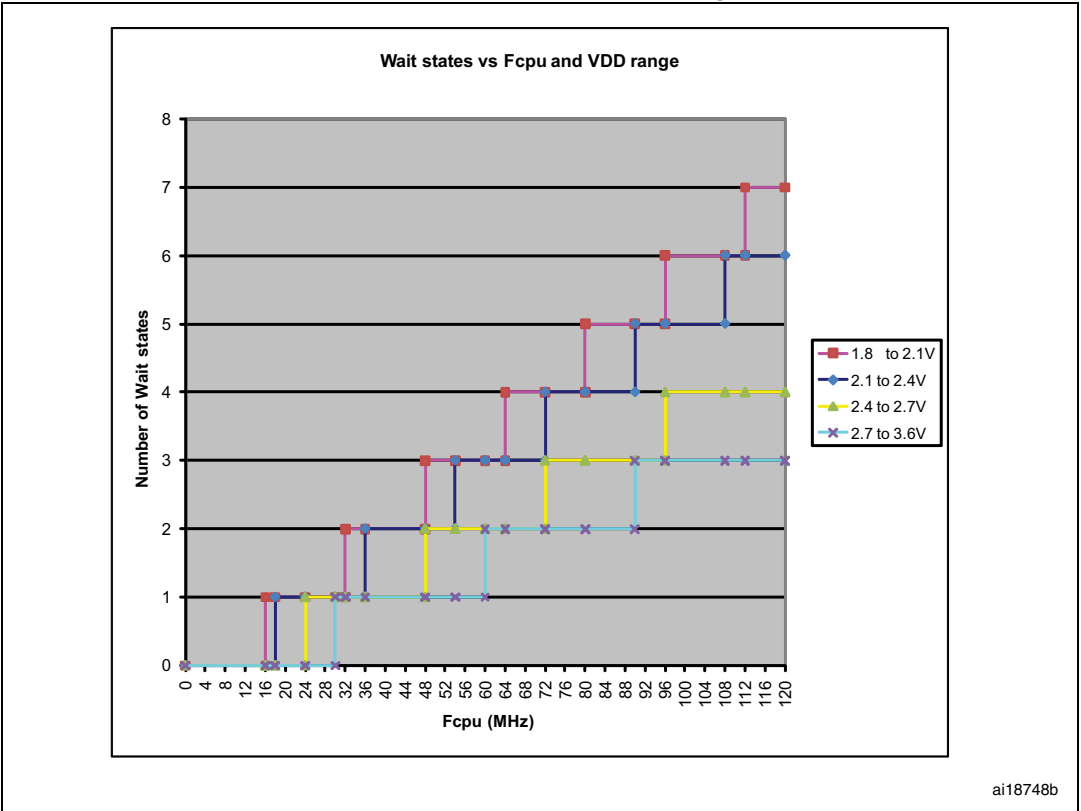
Note: When the microcontroller is supplied from V_{BAT} , external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When using WLCSP64+2 package, if IRROFF pin is connected to V_{DD} , the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
22	H5	31	42	52	P3	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6
23	J7	32	43	53	R3	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
24	H4	33	44	54	N5	PC4	I/O	FT	(4)	ETH_RMII_RXD0, ETH_MII_RXD0, EVENTOUT	ADC12_IN14
25	G3	34	45	55	P5	PC5	I/O	FT	(4)	ETH_RMII_RXD1, ETH_MII_RXD1, EVENTOUT	ADC12_IN15
26	J6	35	46	56	R5	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
27	J5	36	47	57	R4	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
28	J4	37	48	58	M6	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	49	59	R6	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	50	60	P6	PF12	I/O	FT	-	FSMC_A6, EVENTOUT	-
-	-	-	51	61	M8	V _{SS}	S		-	-	-
-	-	-	52	62	N8	V _{DD}	S		-	-	-
-	-	-	53	63	N6	PF13	I/O	FT	-	FSMC_A7, EVENTOUT	-
-	-	-	54	64	R7	PF14	I/O	FT	-	FSMC_A8, EVENTOUT	-
-	-	-	55	65	P7	PF15	I/O	FT	-	FSMC_A9, EVENTOUT	-
-	-	-	56	66	N7	PG0	I/O	FT	-	FSMC_A10, EVENTOUT	-
-	-	-	57	67	M7	PG1	I/O	FT	-	FSMC_A11, EVENTOUT	-

Figure 21. Number of wait states versus f_{CPU} and V_{DD} range

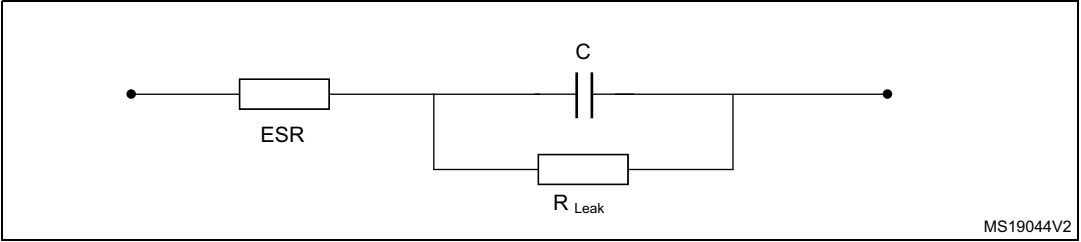


1. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V_{DD} .

6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor to the VCAP1/VCAP2 pins. C_{EXT} is specified in [Table 16](#).

Figure 22. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 16. VCAP1/VCAP2 operating conditions⁽¹⁾

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 μ F
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 μ F V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A .

Table 17. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A .

Table 18. Operating conditions at power-up / power-down (regulator OFF)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}^{(1)}$	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}^{(1)(2)}$	Reset temporization	-	0.5	1.5	3.0	ms
$I_{RUSH}^{(1)}$	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
$E_{RUSH}^{(1)}$	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	$V_{DD} = 1.8\text{ V}$, $T_A = 105\text{ }^{\circ}\text{C}$, $I_{RUSH} = 171\text{ mA}$ for $31\text{ }\mu\text{s}$	-	-	5.4	μC

1. Guaranteed by design, not tested in production.

2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 20: Current consumption measurement scheme](#).

All Run mode current consumption measurements given in this section are performed using CoreMark code.

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f _{HCLK}	Typ	Max ⁽¹⁾		Unit
				T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled ⁽³⁾	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz ⁽⁴⁾	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock ⁽²⁾ , all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz ⁽⁴⁾	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Table 22. Typical and maximum current consumption in Sleep mode

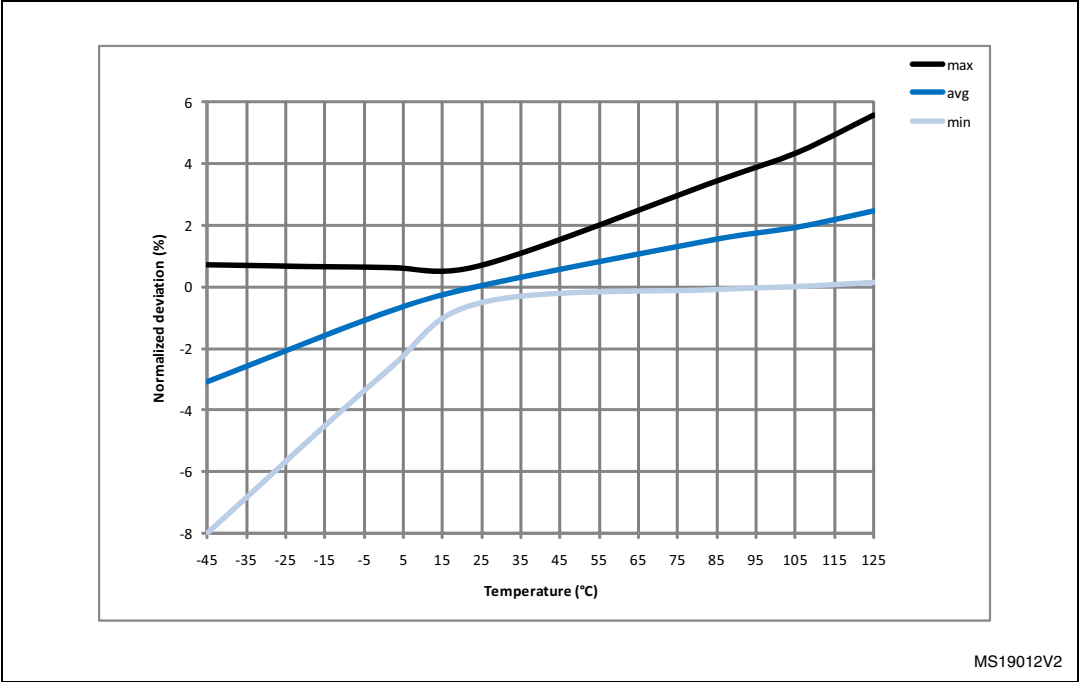
Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max ⁽¹⁾		Unit
				$T_A = 25\text{ °C}$	$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
I_{DD}	Supply current in Sleep mode	External clock ⁽²⁾ , all peripherals enabled ⁽³⁾	120 MHz	38	51	61	mA
			90 MHz	30	43	53	
			60 MHz	20	33	43	
			30 MHz	11	25	35	
			25 MHz	8	21	31	
			16 MHz	6	19	29	
			8 MHz	3.6	17.0	27.0	
			4 MHz	2.4	15.4	25.3	
			2 MHz	1.9	14.9	24.7	
		External clock ⁽²⁾ , all peripherals disabled	120 MHz	8	21	31	
			90 MHz	7	20	30	
			60 MHz	5	18	28	
			30 MHz	3.5	16.0	26.0	
			25 MHz	2.5	16.0	25.0	
			16 MHz	2.1	15.1	25.0	
			8 MHz	1.7	15.0	25.0	
			4 MHz	1.5	14.6	24.6	
			2 MHz	1.4	14.2	24.3	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK} > 25$ MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 26. Peripheral current consumption (continued)

Peripheral ⁽¹⁾		Typical consumption at 25 °C	Unit
APB1	TIM2	0.61	mA
	TIM3	0.49	
	TIM4	0.54	
	TIM5	0.62	
	TIM6	0.20	
	TIM7	0.20	
	TIM12	0.36	
	TIM13	0.28	
	TIM14	0.25	
	USART2	0.25	
	USART3	0.25	
	UART4	0.25	
	UART5	0.26	
	I2C1	0.25	
	I2C2	0.25	
	I2C3	0.25	
	SPI2	0.20/0.10	
	SPI3	0.18/0.09	
	CAN1	0.31	
	CAN2	0.30	
	DAC channel 1 ⁽²⁾	1.11	
	DAC channel 1 ⁽³⁾	1.11	
	PWR	0.15	
	WWDG	0.15	

Figure 34. ACC_{HSI} versus temperature



Low-speed internal (LSI) RC oscillator

Table 33. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	17	32	47	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	15	40	μs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.4	0.6	μA

- $V_{DD} = 3 V$, $T_A = -40$ to $105^\circ C$ unless otherwise specified.
- Guaranteed by characterization results, not tested in production.
- Guaranteed by design, not tested in production.

Figure 36 and Figure 37 show the main PLL output clock waveforms in center spread and down spread modes, where:

F_0 is $f_{\text{PLL_OUT}}$ nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 36. PLL output clock waveforms in center spread mode

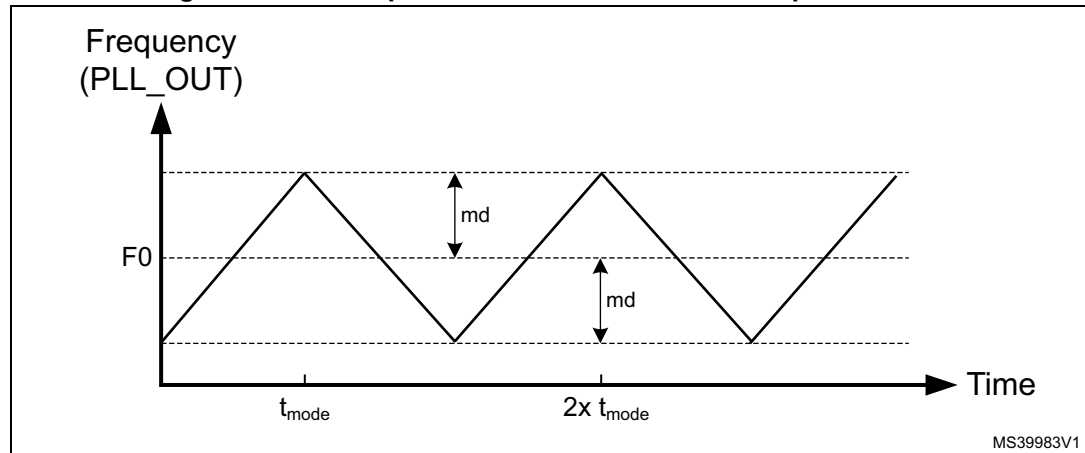
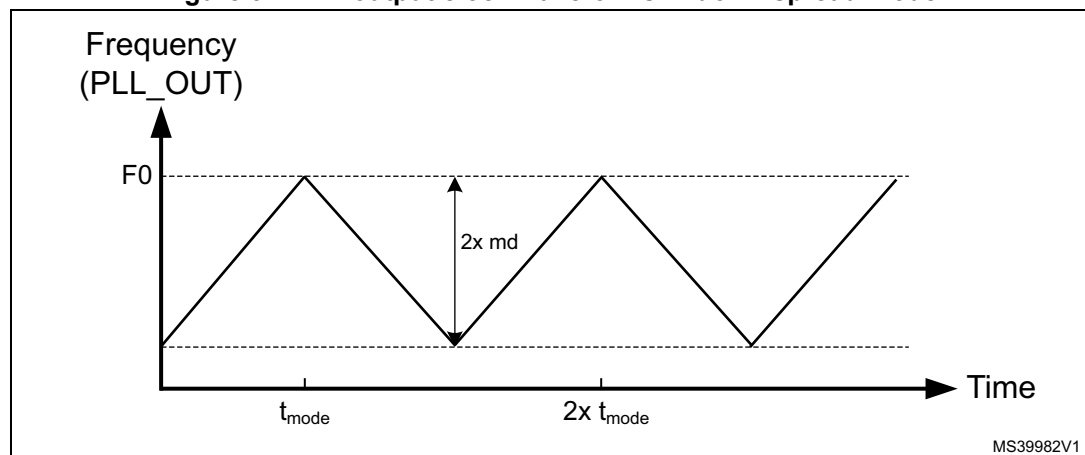


Figure 37. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

6.3.18 TIM timer characteristics

The parameters given in [Table 50](#) and [Table 51](#) are guaranteed by design.

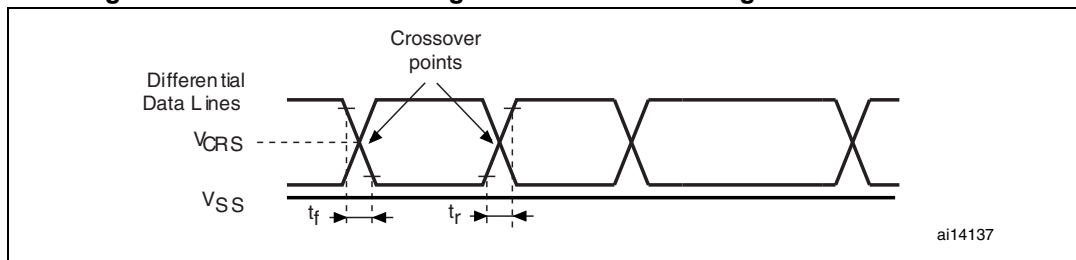
Refer to [Section 6.3.16: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 50. Characteristics of TIMx connected to the APB1 domain⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{\text{res(TIM)}}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{\text{TIMxCLK}} = 60 \text{ MHz}$	1	-	t_{TIMxCLK}
			16.7	-	ns
		AHB/APB1 prescaler = 1, $f_{\text{TIMxCLK}} = 30 \text{ MHz}$	1	-	t_{TIMxCLK}
			33.3	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{\text{TIMxCLK}} = 60 \text{ MHz}$ APB1= 30 MHz	0	$f_{\text{TIMxCLK}}/2$	MHz
			0	30	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{COUNTER}	16-bit counter clock period when internal clock is selected		1	65536	t_{TIMxCLK}
			0.0167	1092	μs
	32-bit counter clock period when internal clock is selected		1	-	t_{TIMxCLK}
			0.0167	71582788	μs
$t_{\text{MAX_COUNT}}$	Maximum possible count		-	65536×65536	t_{TIMxCLK}
			-	71.6	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

Table 58. USB OTG FS electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Table 59 shows the USB HS operating voltage.

Table 59. USB HS DC electrical characteristics

Symbol	Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 60. Clock timing parameters

Parameter ⁽¹⁾		Symbol	Min	Nominal	Max	Unit
Frequency (first transition)	8-bit $\pm 10\%$	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state)	$\pm 500 \text{ ppm}$	F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit $\pm 10\%$	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state)	$\pm 500 \text{ ppm}$	D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	μs

1. Guaranteed by design, not tested in production.

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 66](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 14](#).

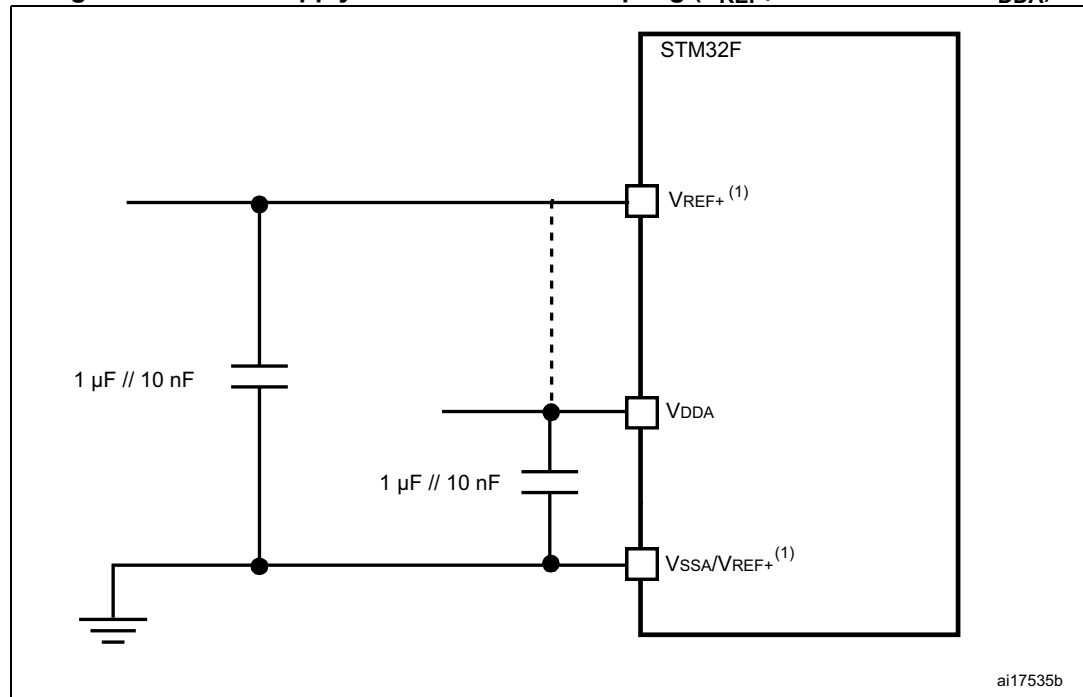
Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8 ⁽¹⁾	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8 ⁽¹⁾⁽²⁾	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	$V_{DDA} = 1.8^{(1)}$ to 2.4 V	0.6	-	15	MHz
		$V_{DDA} = 2.4$ to 3.6 V	0.6	-	30	MHz
$f_{TRIG}^{(3)}$	External trigger frequency	$f_{ADC} = 30$ MHz with 12-bit resolution	-	-	1764	kHz
		-	-	-	17	1/ f_{ADC}
V_{AIN}	Conversion voltage range ⁽⁴⁾	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(3)}$	External input impedance	See Equation 1 for details	-	-	50	k Ω
$R_{ADC}^{(3)(5)}$	Sampling switch resistance	-	1.5	-	6	k Ω
$C_{ADC}^{(3)}$	Internal sample and hold capacitor	-	-	4	-	pF
$t_{lat}^{(3)}$	Injection trigger conversion latency	$f_{ADC} = 30$ MHz	-	-	0.100	μ s
		-	-	-	3 ⁽⁶⁾	1/ f_{ADC}
$t_{latr}^{(3)}$	Regular trigger conversion latency	$f_{ADC} = 30$ MHz	-	-	0.067	μ s
		-	-	-	2 ⁽⁶⁾	1/ f_{ADC}
$t_S^{(3)}$	Sampling time	$f_{ADC} = 30$ MHz	0.100	-	16	μ s
		-	3	-	480	1/ f_{ADC}
$t_{STAB}^{(3)}$	Power-up time	-	-	2	3	μ s
$t_{CONV}^{(3)}$	Total conversion time (including sampling time)	$f_{ADC} = 30$ MHz 12-bit resolution	0.5	-	16.40	μ s
		$f_{ADC} = 30$ MHz 10-bit resolution	0.43	-	16.34	μ s
		$f_{ADC} = 30$ MHz 8-bit resolution	0.37	-	16.27	μ s
		$f_{ADC} = 30$ MHz 6-bit resolution	0.3	-	16.20	μ s
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				1/ f_{ADC}

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 54](#) or [Figure 55](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

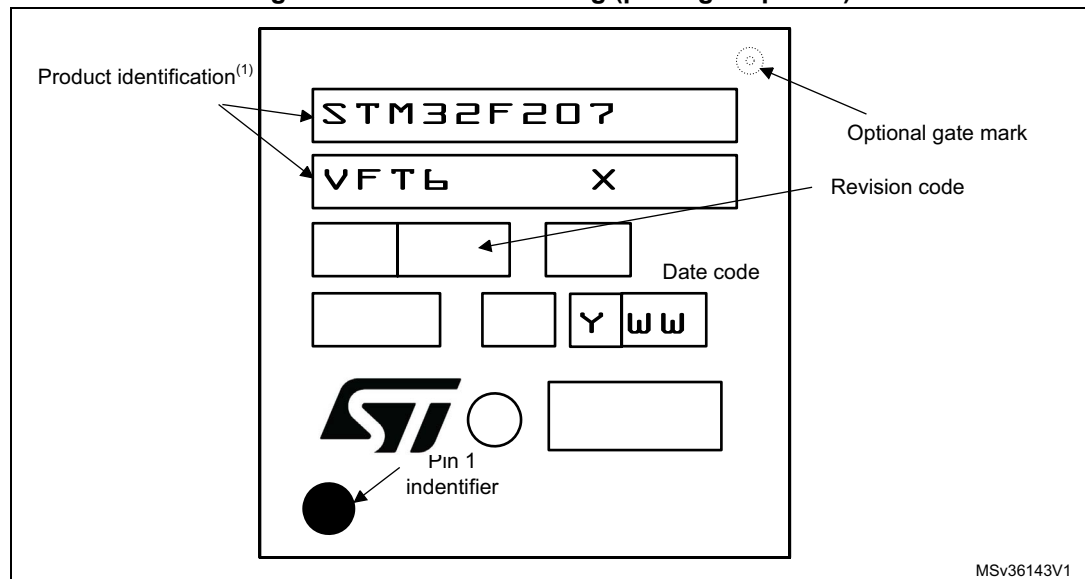
Figure 54. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

Device marking

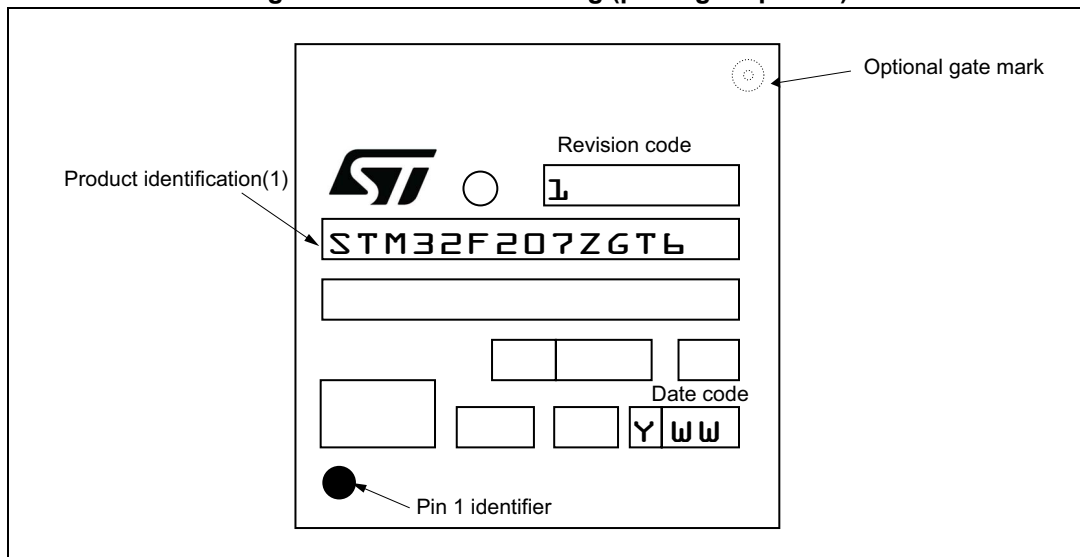
Figure 83. LQFP100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

Figure 86. LQFP144 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 92. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package
mechanical data (continued)**

Symbol	Dimensions					
	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
HD	25.900	-	26.100	1.0197	-	1.0276
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L ⁽²⁾	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.