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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207vgt6tr

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3.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All STM32F20x products embed:

- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

The content of this area is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).

- V_{SSA} , V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 19: Power supply scheme](#) for more details.

3.15 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry.

At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit. On devices in WLCSP64+2 package, the BOR, POR and PDR features can be disabled by setting IRROFF pin to V_{DD} . In this mode an external power supply supervisor is required (see [Section 3.16](#)).

The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.16 Voltage regulator

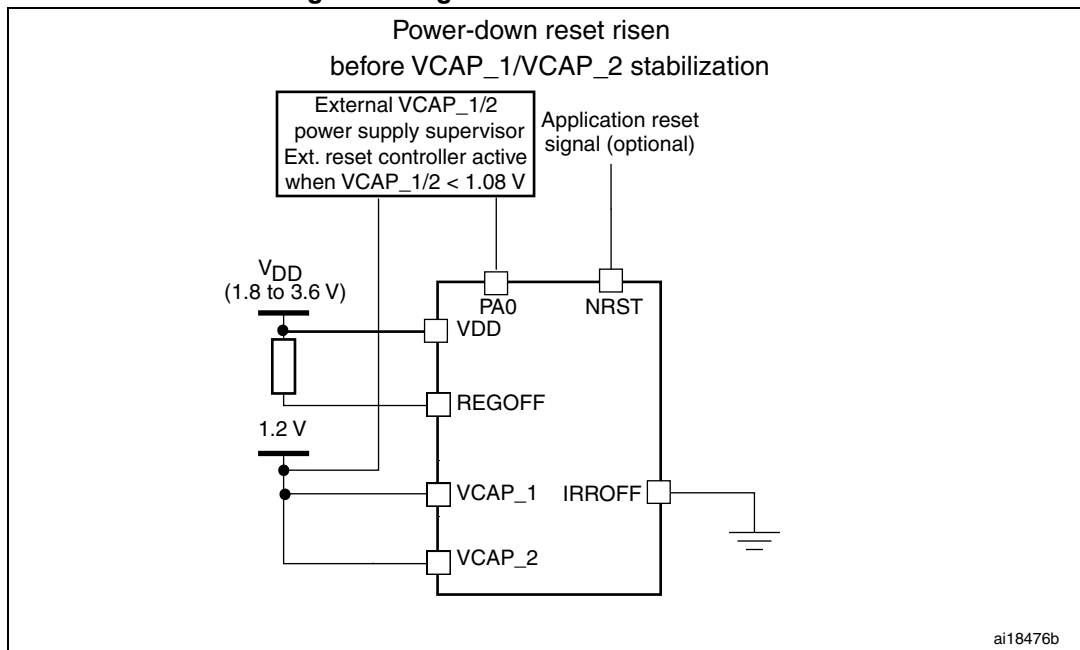
The regulator has five operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low-power regulator (LPR)
 - Power-down
- Regulator OFF
 - Regulator OFF/internal reset ON
 - Regulator OFF/internal reset OFF

3.16.1 Regulator ON

The regulator ON modes are activated by default on LQFP packages. On WLCSP64+2 package, they are activated by connecting both REGOFF and IRROFF pins to V_{SS} , while only REGOFF must be connected to V_{SS} on UFBGA176 package (IRROFF is not available).

V_{DD} minimum value is 1.8 V.

Figure 6. Regulator OFF/internal reset ON

The following conditions must be respected:

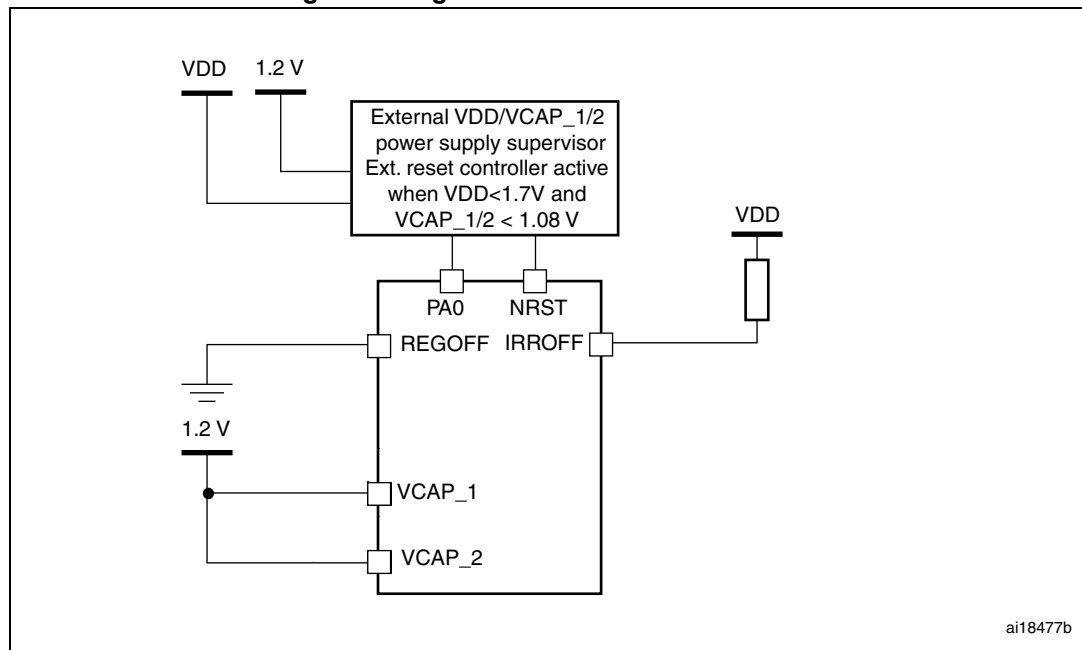
- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see [Figure 8](#)).
- Otherwise, If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is slower than the time for V_{DD} to reach 1.8 V, then PA0 should be asserted low externally (see [Figure 9](#)).
- If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Regulator OFF/internal reset OFF

On WLCSP64+2 package, this mode activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD} . IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP64+2 package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins. In this mode, the integrated power-on reset (POR)/ power-down reset (PDR) circuitry is disabled.

An external power supply supervisor should monitor both the external 1.2 V and the external V_{DD} supply voltage, and should maintain the device in reset mode as long as they remain below a specified threshold. The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V. This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range. A comprehensive set of power-saving modes allows to design low-power applications.

Figure 7. Regulator OFF/internal reset OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains (see [Figure 8](#)).
- PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V, and until V_{DD} reaches 1.7 V.
- NRST should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.7 V (see [Figure 9](#)).

In this mode, when the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry is disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON/internal reset ON	Regulator OFF/internal reset ON	Regulator OFF/internal reset OFF
LQFP64 LQFP100 LQFP144 LQFP176	Yes	No	No
WLCSP 64+2	Yes REGOFF and IRROFF set to V _{SS}	Yes REGOFF set to V _{DD} and IRROFF set to V _{SS}	Yes REGOFF set to V _{SS} and IRROFF set to V _{DD}
UFBGA176	Yes REGOFF set to V _{SS}	Yes REGOFF set to V _{DD}	No

3.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F20x devices includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Its main features are the following:

- Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.
- It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.
- Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μ s to every 36 hours.
- A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The 4-Kbyte backup SRAM is an EEPROM-like area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled to minimize power consumption (see [Section 3.18: Low-power modes](#)). It can be enabled by software.

3.20.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.20.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.21 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

3.22 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F20x devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

3.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

3.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F20x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F20x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	-	84	N12	PH7	I/O	FT	-	I2C3_SCL, ETH_MII_RXD3, EVENTOUT	-
-	-	-	-	85	M12	PH8	I/O	FT	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	86	M13	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, DCMI_D0, EVENTOUT	-
-	-	-	-	87	L13	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	88	L12	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	89	K12	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	90	H12	V _{SS}	S	-	-	-	-
-	-	-	-	91	J12	V _{DD}	S	-	-	-	-
33	J1	51	73	92	P12	PB12	I/O	FT	-	SPI2_NSS, I2S2_WS, I2C2_SMBA, USART3_CK, TIM1_BKIN, CAN2_RX, OTG_HS_ULPI_D5, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_HS_ID, EVENTOUT	-
34	H2	52	74	93	P13	PB13	I/O	FT	-	SPI2_SCK, I2S2_SCK, USART3_CTS, TIM1_CH1N, CAN2_TX, OTG_HS_ULPI_D6, ETH_RMII_TXD1, ETH_MII_TXD1, EVENTOUT	OTG_HS_ VBUS
35	H1	53	75	94	R14	PB14	I/O	FT	-	SPI2_MISO, TIM1_CH2N, TIM12_CH1, OTG_HS_DM USART3_RTS, TIM8_CH2N, EVENTOUT	-
36	G1	54	76	95	R15	PB15	I/O	FT	-	SPI2_MOSI, I2S2_SD, TIM1_CH3N, TIM8_CH3N, TIM12_CH2, OTG_HS_DP, RTC_50Hz, EVENTOUT	-
-	-	55	77	96	P15	PD8	I/O	FT	-	FSMC_D13, USART3_TX, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	-	131	159	C7	V _{DD}	S	-	-	-	-
-	-	-	132	160	B7	PG15	I/O	FT	-	USART6_CTS, DCM1_D13, EVENTOUT	-
55	A4	89	133	161	A10	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/ TRACESWO, SPI3_SCK, I2S3_SCK, TIM2_CH2, SPI1_SCK, EVENTOUT	-
56	B4	90	134	162	A9	PB4	I/O	FT	-	NJTRST, SPI3_MISO, TIM3_CH1, SPI1_MISO, EVENTOUT	-
57	A5	91	135	163	A6	PB5	I/O	FT	-	I2C1_SMBA, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, DCM1_D10, I2S3_SD, EVENTOUT	-
58	B5	92	136	164	B6	PB6	I/O	FT	-	I2C1_SCL,, TIM4_CH1, CAN2_TX, DCM1_D5,USART1_TX, EVENTOUT	-
59	A6	93	137	165	B5	PB7	I/O	FT	-	I2C1_SDA, FSMC_NL ⁽⁶⁾ , DCM1_VSYNC, USART1_RX, TIM4_CH2, EVENTOUT	-
60	B6	94	138	166	D6	BOOT0	I	B	-	-	V _{PP}
61	B7	95	139	167	A5	PB8	I/O	FT	-	TIM4_CH3,SDIO_D4, TIM10_CH1, DCM1_D6, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-
62	A7	96	140	168	B4	PB9	I/O	FT	-	SPI2_NSS, I2S2_WS, TIM4_CH4, TIM11_CH1, SDIO_D5, DCM1_D7, I2C1_SDA, CAN1_TX, EVENTOUT	-
-	-	97	141	169	A4	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, DCM1_D2, EVENTOUT	-

Table 30. HSE 4-26 MHz oscillator characteristics^{(1) (2)}

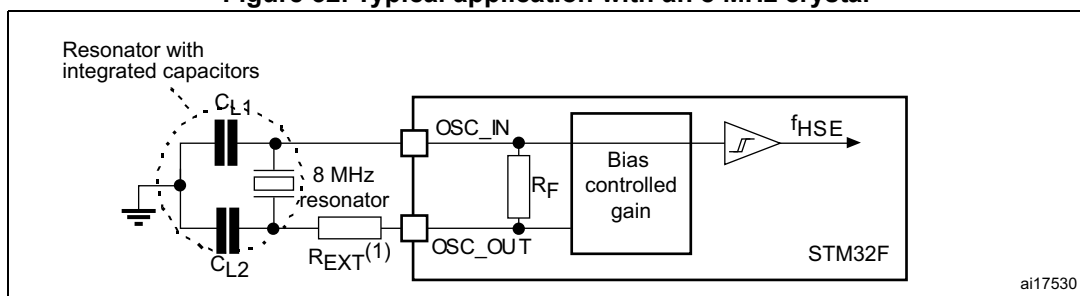
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
I_{DD}	HSE current consumption	$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=5\text{ pF@25 MHz}$	-	449	-	μA
		$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=10\text{ pF@25 MHz}$	-	532	-	
g_m	Oscillator transconductance	Startup	5	-	-	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results, not tested in production.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 32](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 32. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 31](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Jitter ⁽³⁾	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-
			peak to peak	-	±280	-
		Average frequency of 12.288 MHz N=432, R=5 on 1000 samples	-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples	-	400	-	ps
$I_{DD(PLLI2S)}$ ⁽⁴⁾	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$ ⁽⁴⁾	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization results, not tested in production.

Figure 42. SPI timing diagram - slave mode and CPHA = 0

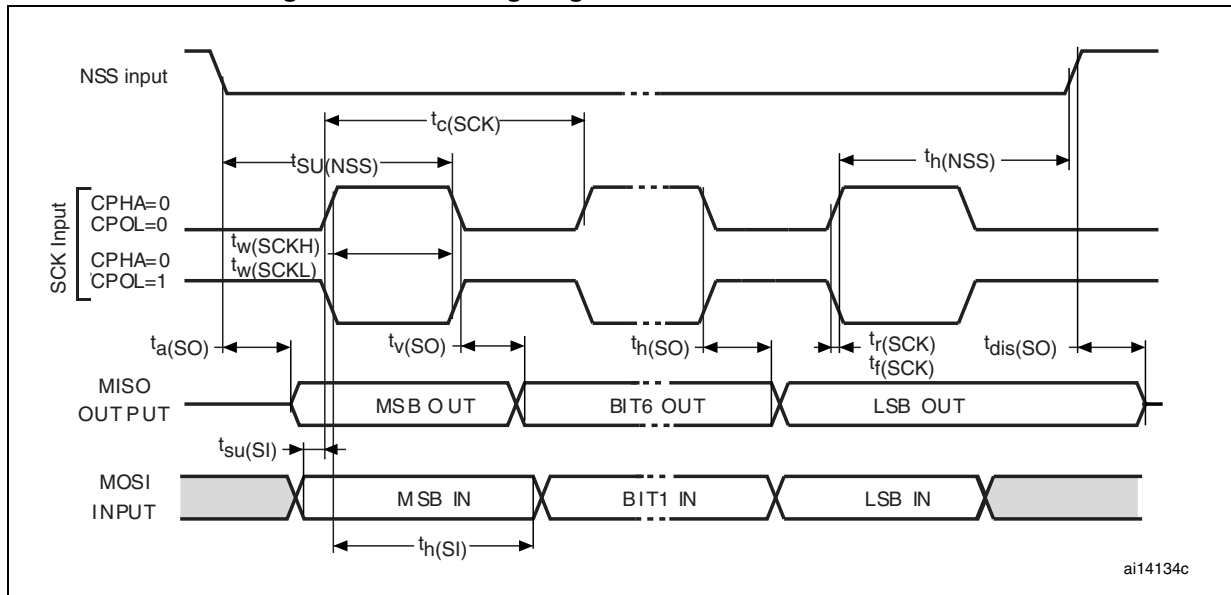


Figure 43. SPI timing diagram - slave mode and CPHA = 1

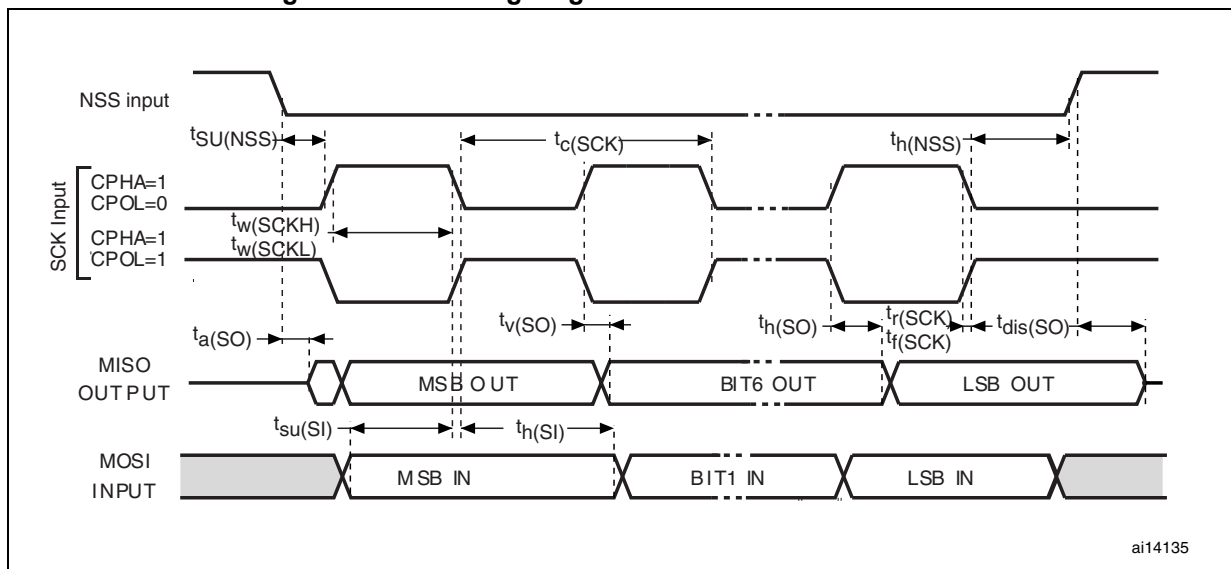


Figure 49. Ethernet SMI timing diagram

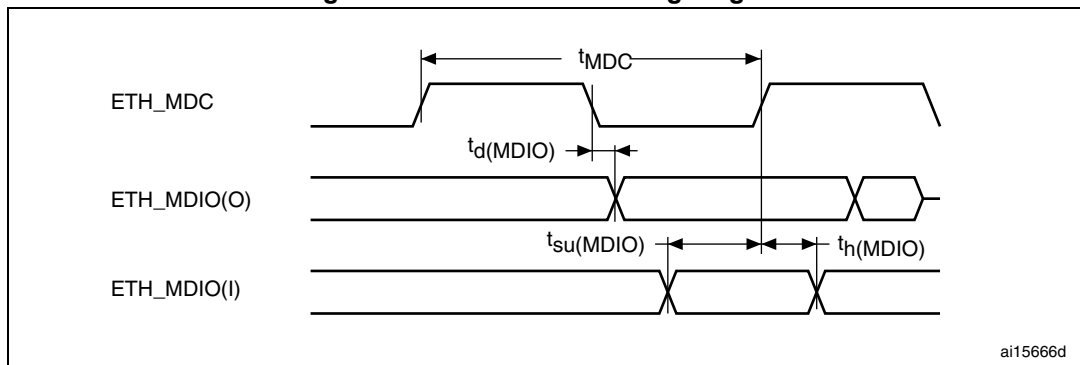


Table 63. Dynamics characteristics: Ethernet MAC signals for SMI

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (2.38 MHz)	411	420	425	ns
$t_{d(MDIO)}$	MDIO write data valid time	6	10	13	ns
$t_{su(MDIO)}$	Read data setup time	12	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

Table 64 gives the list of Ethernet MAC signals for the RMII and Figure 50 shows the corresponding timing diagram.

Figure 50. Ethernet RMII timing diagram

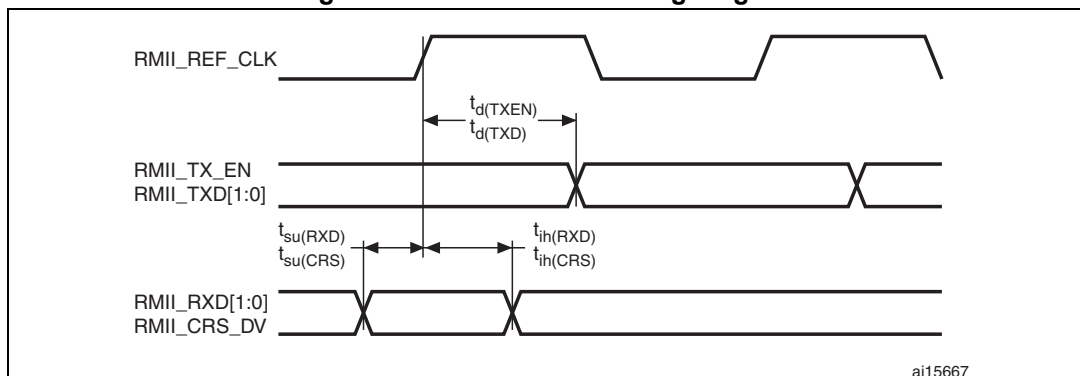


Table 64. Dynamics characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(CRS)}$	Carrier sense set-up time	0	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	9	11	13	
$t_{d(TXD)}$	Transmit data valid delay time	9	11.5	14	

Figure 61. Synchronous multiplexed NOR/PSRAM read timings

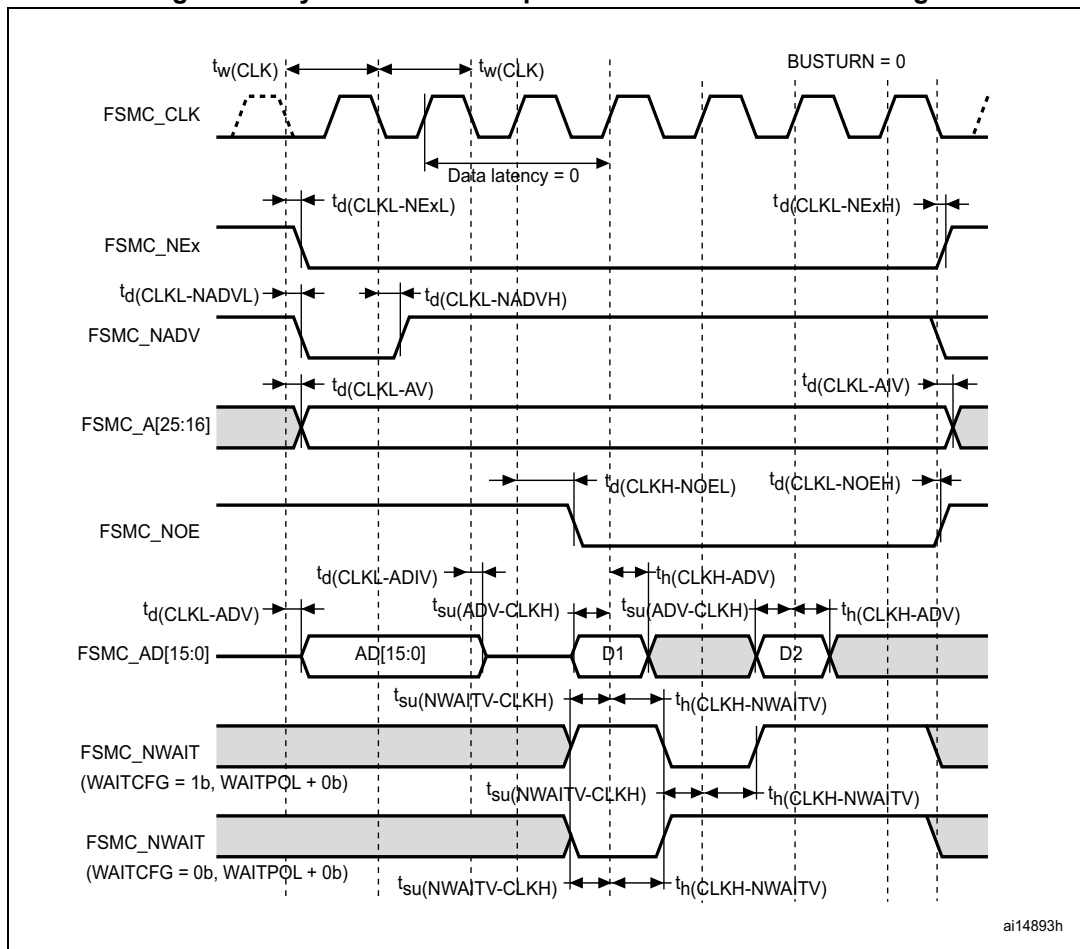


Table 76. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

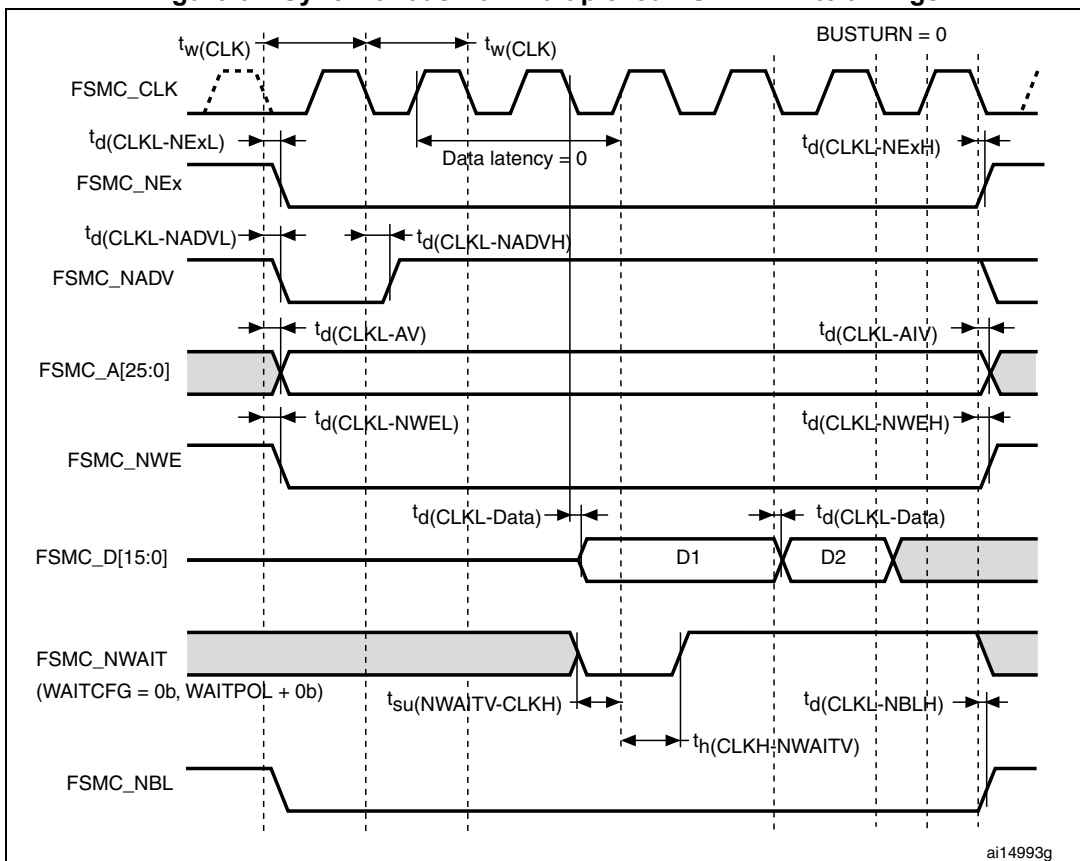
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0...2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1.5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	2.5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16...25)	0	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	3	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾ (continued)

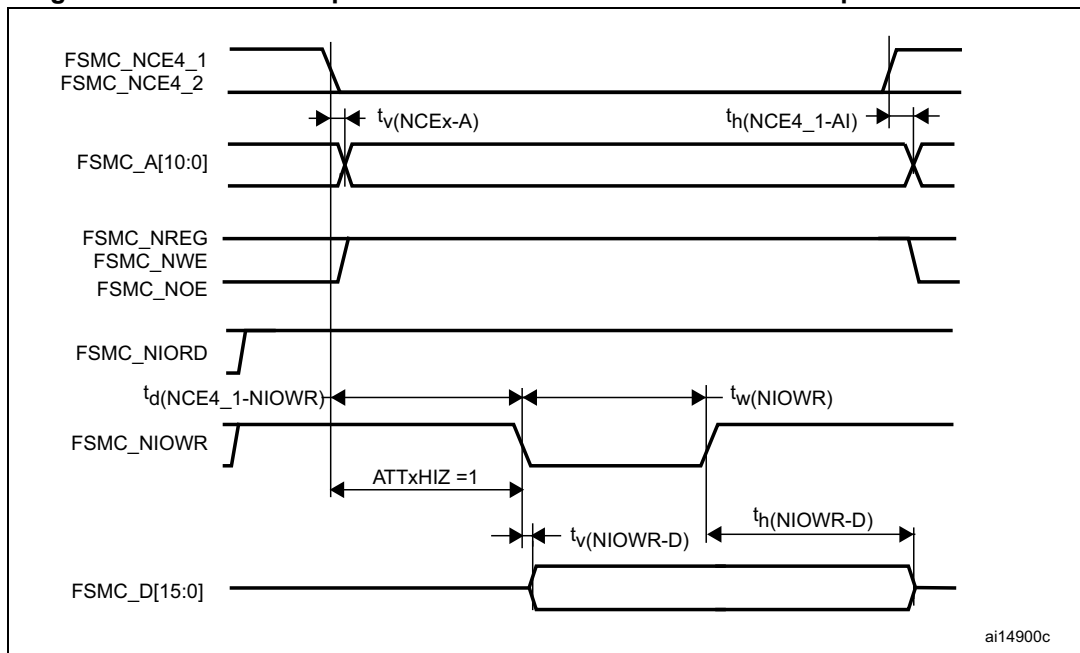
Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16...25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_h(CLKH-DV)$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results, not tested in production.

Figure 64. Synchronous non-multiplexed PSRAM write timings**Table 79. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾**

Symbol	Parameter	Min	Max	Unit
$t_w(CLK)$	FSMC_CLK period	$2T_{HCLK} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0...2)	1	-	ns

Figure 70. PC Card/CompactFlash controller waveforms for I/O space write access**Table 80. Switching characteristics for PC Card/CF read and write cycles in attribute/common space⁽¹⁾⁽²⁾**

Symbol	Parameter	Min	Max	Unit
$t_v(NCEx-A)$	FSMC_Ncex low to FSMC_Ay valid	-	0	ns
$t_h(NCEx-AI)$	FSMC_NCEx high to FSMC_Ax invalid	4	-	ns
$t_d(NREG-NCEx)$	FSMC_NCEx low to FSMC_NREG valid	-	3.5	ns
$t_h(NCEx-NREG)$	FSMC_NCEx high to FSMC_NREG invalid	$T_{HCLK} + 4$	-	ns
$t_d(NCEx-NWE)$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK} + 1$	ns
$t_d(NCEx-NOE)$	FSMC_NCEx low to FSMC_NOE low	-	$5T_{HCLK}$	ns
$t_w(NOE)$	FSMC_NOE low width	$8T_{HCLK} - 0.5$	$8T_{HCLK} + 1$	ns
$t_d(NOE-NCEx)$	FSMC_NOE high to FSMC_NCEx high	$5T_{HCLK} + 2.5$	-	ns
$t_{su}(D-NOE)$	FSMC_D[15:0] valid data before FSMC_NOE high	4	-	ns
$t_h(NOE-D)$	FSMC_NOE high to FSMC_D[15:0] invalid	2	-	ns
$t_w(NWE)$	FSMC_NWE low width	$8T_{HCLK} - 1$	$8T_{HCLK} + 4$	ns
$t_d(NWE-NCEx)$	FSMC_NWE high to FSMC_NCEx high	$5T_{HCLK} + 1.5$	-	ns
$t_d(NCEx-NWE)$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK} + 1$	ns
$t_v(NWE-D)$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_h(NWE-D)$	FSMC_NWE high to FSMC_D[15:0] invalid	$8T_{HCLK}$	-	ns
$t_d(D-NWE)$	FSMC_D[15:0] valid before FSMC_NWE high	$13T_{HCLK}$	-	ns

1. $C_L = 30$ pF.

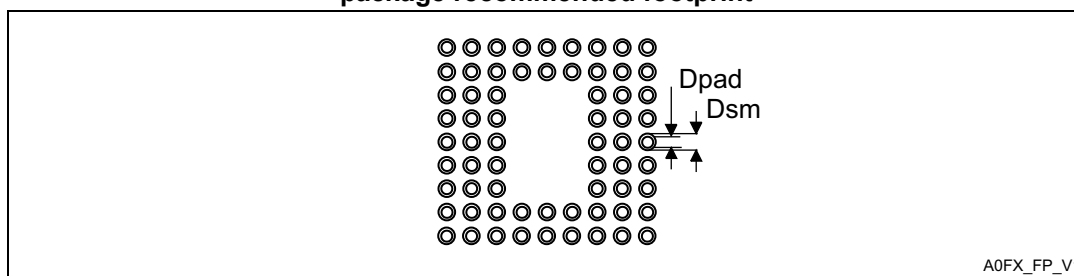
2. Guaranteed by characterization results, not tested in production.

Table 88. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
F	-	0.220	-	-	0.0087	-
G	-	0.386	-	-	0.0152	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 80. WLCSP64+2 - 66-ball, 4.539 x 4.911 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**Table 89. WLCSP64 recommended PCB design rules (0.4 mm pitch)**

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Updated <i>Typical and maximum current consumption</i> conditions, as well as <i>Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)</i> and <i>Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM</i>. Added <i>Figure 23</i>, <i>Figure 24</i>, <i>Figure 25</i>, and <i>Figure 26</i>. Updated <i>Table 22: Typical and maximum current consumption in Sleep mode</i>, and added <i>Figure 27</i> and <i>Figure 28</i>. Updated <i>Table 23: Typical and maximum current consumptions in Stop mode</i>. Added <i>Figure 29: Typical current consumption vs. temperature in Stop mode</i>. Updated <i>Table 24: Typical and maximum current consumptions in Standby mode</i> and <i>Table 25: Typical and maximum current consumptions in VBAT mode</i>. Updated <i>On-chip peripheral current consumption</i> conditions and <i>Table 26: Peripheral current consumption</i>. Updated $t_{WUSTDBY}$ and t_{WUSTOP} and added <i>Note 3</i> in <i>Table 27: Low-power mode wakeup timings</i>. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in <i>Table 28: High-speed external user clock characteristics</i>. Updated C and g_m in <i>Table 30: HSE 4-26 MHz oscillator characteristics</i>. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in <i>Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)</i>. Added <i>Note 1</i> and updated ACC_{HSI}, $IDD_{(HSI)}$, and $t_{su(HSI)}$ in <i>Table 32: HSI oscillator characteristics</i>. Added <i>Figure 34: ACCHSI versus temperature</i>. Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in <i>Table 33: LSI oscillator characteristics</i>. Added <i>Figure 35: ACCLSI versus temperature</i>. <i>Table 34: Main PLL characteristics</i>: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added <i>Note 2</i> for f_{PLL_IN} minimum and maximum values. <i>Table 35: PLLI2S (audio PLL) characteristics</i>: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added <i>Note 2</i> for f_{PLLI2S_IN} minimum and maximum values. Added <i>Note 1</i> in <i>Table 36: SSCG parameters constraint</i>. Updated <i>Table 37: Flash memory characteristics</i>. Modified <i>Table 38: Flash memory programming</i> and added <i>Note 2</i> for t_{prog}. Updated t_{prog} and added <i>Note 1</i> in <i>Table 39: Flash memory programming with VPP</i>. Modified <i>Figure 40: Recommended NRST pin protection</i>. Updated <i>Table 42: EMI characteristics</i> and EMI monitoring conditions in <i>Section : Electromagnetic Interference (EMI)</i>. Added <i>Note 2</i> related to $V_{ESD(HBM)}$ in <i>Table 43: ESD absolute maximum ratings</i>. Updated <i>Table 48: I/O AC characteristics</i>. Added <i>Section 6.3.15: I/O current injection characteristics</i>. Modified maximum frequency values and conditions in <i>Table 48: I/O AC characteristics</i>. Updated $t_{res(TIM)}$ in <i>Table 50: Characteristics of TIMx connected to the APB1 domain</i>. Modified $t_{res(TIM)}$ and f_{EXT} <i>Table 51: Characteristics of TIMx connected to the APB2 domain</i>.