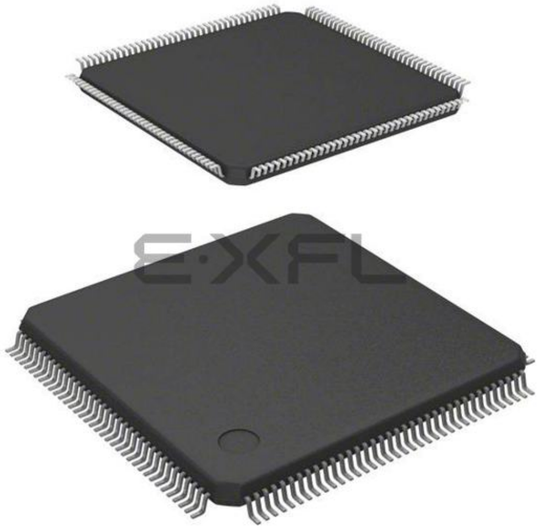

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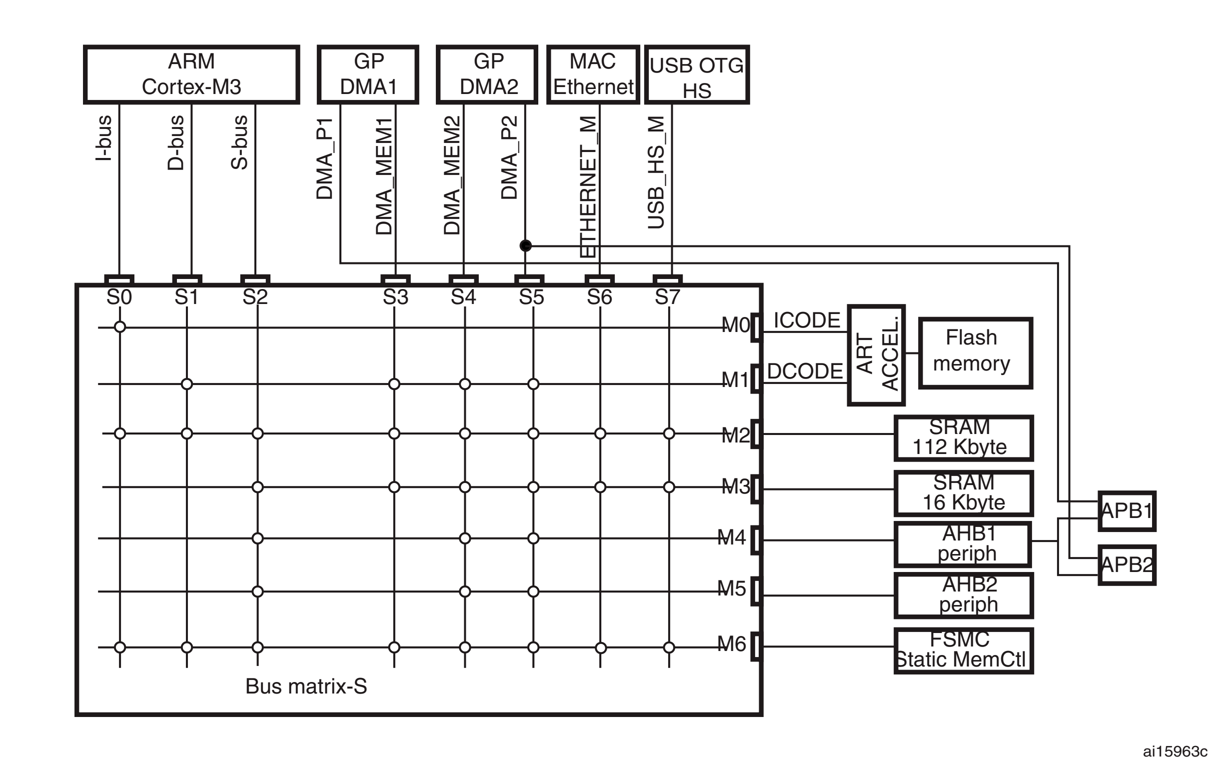
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207zet6tr

Figure 5. Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

3.20 Timers and watchdogs

The STM32F20x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock	Max timer clock
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	60 MHz	120 MHz
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	30 MHz	60 MHz
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	30 MHz	60 MHz
General purpose	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	60 MHz	120 MHz
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	60 MHz	120 MHz
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	30 MHz	60 MHz
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	30 MHz	60 MHz

3.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

3.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

3.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F20x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024× 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.31 Digital camera interface (DCMI)

The camera interface is not available in STM32F205xx devices.

STM32F207xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.32 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

3.33 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

3.34 ADCs (analog-to-digital converters)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers TIM1, TIM2, TIM3, TIM4, TIM5 and TIM8 can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.35 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

Table 8. STM32F20x pin and ball definitions

Pins						Pin name (function after reset)(1)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	1	1	1	A2	PE2	I/O	FT	-	TRACECLK, FSMC_A23, ETH_MII_TXD3, EVENTOUT	-
-	-	2	2	2	A1	PE3	I/O	FT	-	TRACED0,FSMC_A19, EVENTOUT	-
-	-	3	3	3	B1	PE4	I/O	FT	-	TRACED1,FSMC_A20, DCMI_D4, EVENTOUT	-
-	-	4	4	4	B2	PE5	I/O	FT	-	TRACED2, FSMC_A21, TIM9_CH1, DCMI_D6, EVENTOUT	-
-	-	5	5	5	B3	PE6	I/O	FT	-	TRACED3, FSMC_A22, TIM9_CH2, DCMI_D7, EVENTOUT	-
1	A9	6	6	6	C1	V_{BAT}	S		-	-	-
-	-	-	-	7	D2	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_AF2
2	B8	7	7	8	D1	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1
3	B9	8	8	9	E1	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN(4)
4	C9	9	9	10	F1	PC15-OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT(4)
-	-	-	-	11	D3	PI9	I/O	FT	-	CAN1_RX,EVENTOUT	-
-	-	-	-	12	E3	PI10	I/O	FT	-	ETH_MII_RX_ER, EVENTOUT	-
-	-	-	-	13	E4	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	-	-	14	F2	V_{SS}	S		-	-	-
-	-	-	-	15	F3	V_{DD}	S		-	-	-
-	-	-	10	16	E2	PF0	I/O	FT	-	FSMC_A0, I2C2_SDA, EVENTOUT	-
-	-	-	11	17	H3	PF1	I/O	FT	-	FSMC_A1, I2C2_SCL, EVENTOUT	-
-	-	-	12	18	H2	PF2	I/O	FT	-	FSMC_A2, I2C2_SMBA, EVENTOUT	-
-	-	-	13	19	J2	PF3	I/O	FT	(4)	FSMC_A3, EVENTOUT	ADC3_IN9

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
22	H5	31	42	52	P3	PA6	I/O	FT	(4)	SPI1_MISO, TIM8_BKIN, TIM13_CH1, DCMI_PIXCLK, TIM3_CH1, TIM1_BKIN, EVENTOUT	ADC12_IN6
23	J7	32	43	53	R3	PA7	I/O	FT	(4)	SPI1_MOSI, TIM8_CH1N, TIM14_CH1, TIM3_CH2, ETH_MII_RX_DV, TIM1_CH1N, ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
24	H4	33	44	54	N5	PC4	I/O	FT	(4)	ETH_RMII_RXD0, ETH_MII_RXD0, EVENTOUT	ADC12_IN14
25	G3	34	45	55	P5	PC5	I/O	FT	(4)	ETH_RMII_RXD1, ETH_MII_RXD1, EVENTOUT	ADC12_IN15
26	J6	35	46	56	R5	PB0	I/O	FT	(4)	TIM3_CH3, TIM8_CH2N, OTG_HS_ULPI_D1, ETH_MII_RXD2, TIM1_CH2N, EVENTOUT	ADC12_IN8
27	J5	36	47	57	R4	PB1	I/O	FT	(4)	TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, TIM1_CH3N, EVENTOUT	ADC12_IN9
28	J4	37	48	58	M6	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	49	59	R6	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	50	60	P6	PF12	I/O	FT	-	FSMC_A6, EVENTOUT	-
-	-	-	51	61	M8	V_{SS}	S		-	-	-
-	-	-	52	62	N8	V_{DD}	S		-	-	-
-	-	-	53	63	N6	PF13	I/O	FT	-	FSMC_A7, EVENTOUT	-
-	-	-	54	64	R7	PF14	I/O	FT	-	FSMC_A8, EVENTOUT	-
-	-	-	55	65	P7	PF15	I/O	FT	-	FSMC_A9, EVENTOUT	-
-	-	-	56	66	N7	PG0	I/O	FT	-	FSMC_A10, EVENTOUT	-
-	-	-	57	67	M7	PG1	I/O	FT	-	FSMC_A11, EVENTOUT	-

Figure 30. High-speed external clock source AC timing diagram

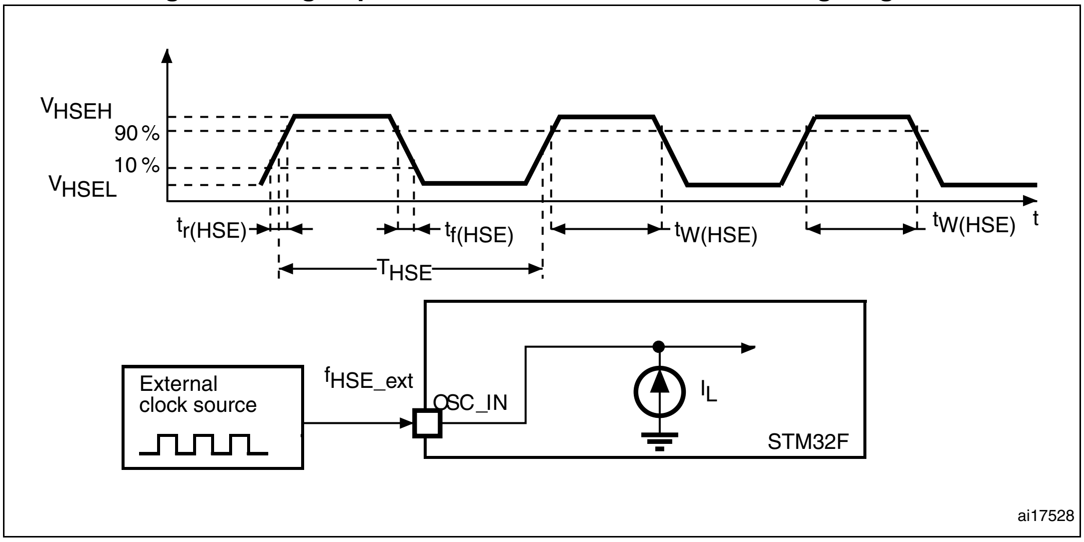
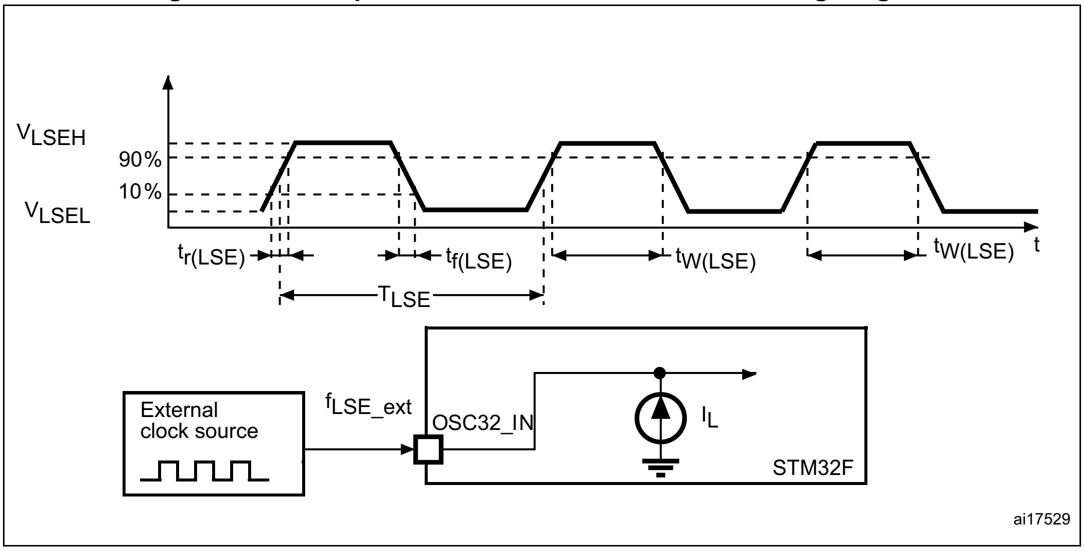


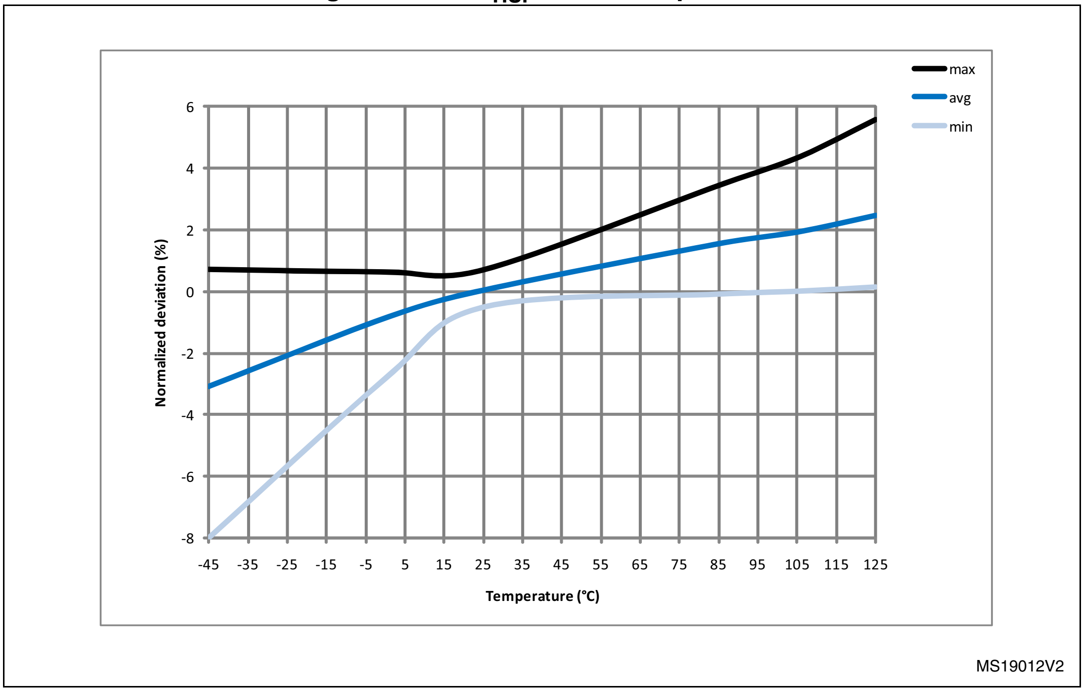
Figure 31. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 30*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Figure 34. ACC_{HSI} versus temperature



Low-speed internal (LSI) RC oscillator

Table 33. LSI oscillator characteristics [(1)]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI} [(2)]	Frequency	17	32	47	kHz
$t_{su(LSI)}$ [(3)]	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$ [(3)]	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 42: EMI characteristics*). It is available only on the main PLL.

Table 36. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%(peak)$$

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*.

Table 45. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	–0	NA	mA
	Injected current on NRST pin	–0	NA	
	Injected current on TTa pins: PA4 and PA5	–0	+5	
	Injected current on all FT pins	–5	NA	

1. NA stands for “not applicable”.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

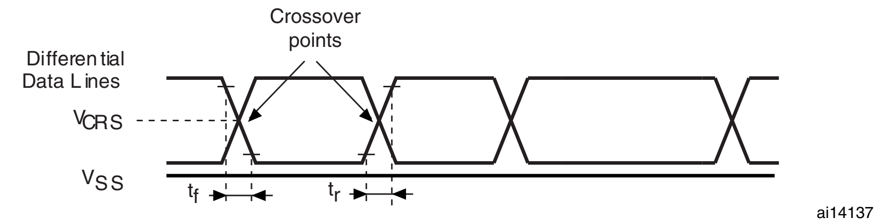


Table 58. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Table 59 shows the USB HS operating voltage.

Table 59. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 60. Clock timing parameters

Parameter(1)		Symbol	Min	Nominal	Max	Unit
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design, not tested in production.

Figure 48. ULPI timing diagram

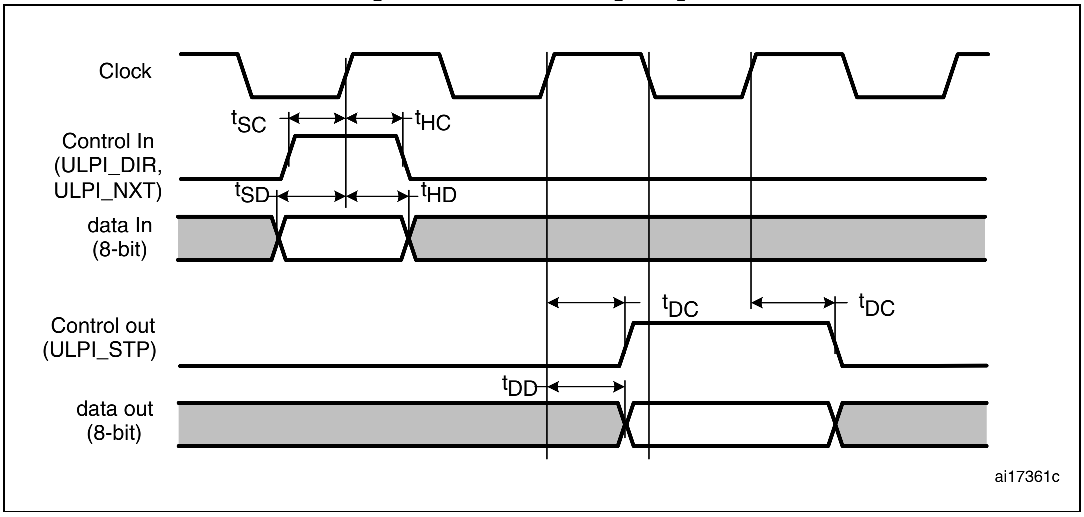


Table 61. ULPI timing

Symbol	Parameter	Value(1)		Unit
		Min.	Max.	
t_{SC}	Control in (ULPI_DIR) setup time	-	2.0	ns
	Control in (ULPI_NXT) setup time	-	1.5	
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0	-	
t_{SD}	Data in setup time	-	2.0	
t_{HD}	Data in hold time	0	-	
t_{DC}	Control out (ULPI_STP) setup time and hold time	-	9.2	
t_{DD}	Data out available from clock rising edge	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Ethernet characteristics

Table 62 shows the Ethernet operating voltage.

Table 62. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

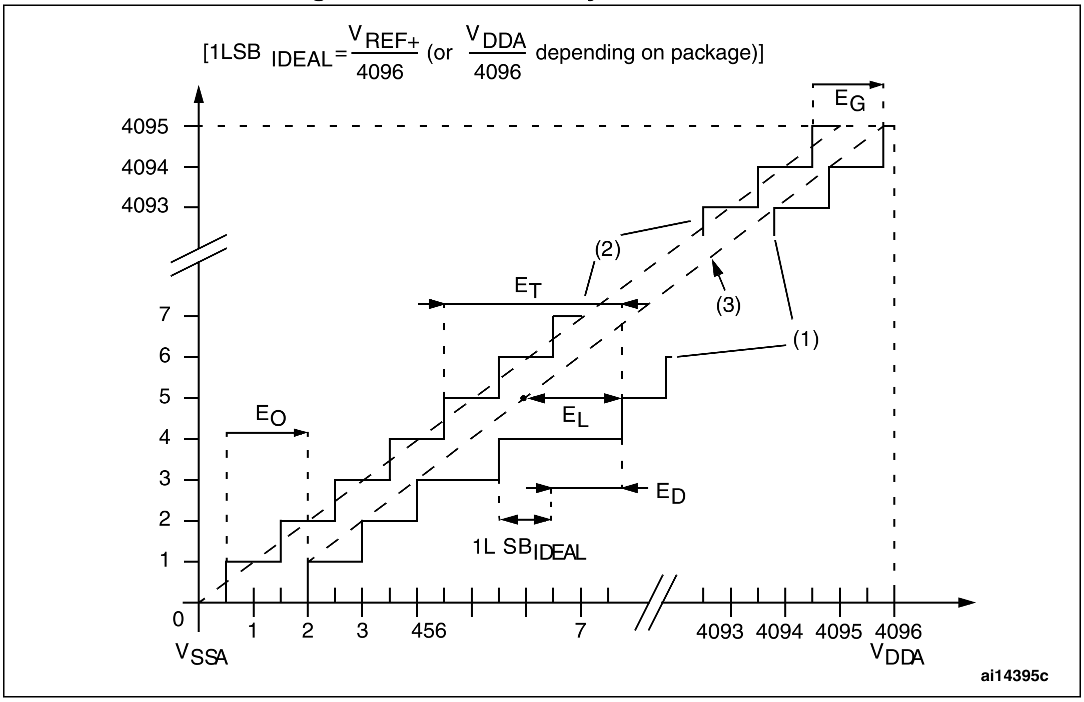
1. All the voltages are measured from the local ground potential.

Table 63 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 49* shows the corresponding timing diagram.

being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

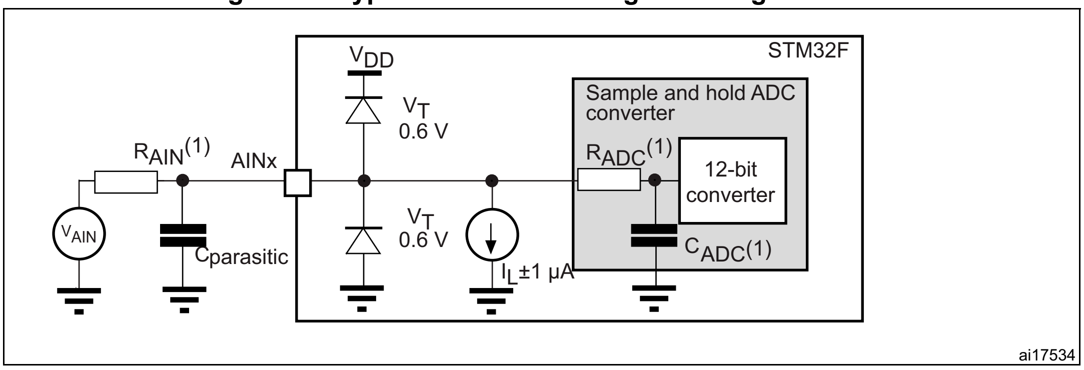
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 52. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
EO = Offset Error: deviation between the first actual transition and the first ideal one.
EG = Gain Error: deviation between the last ideal transition and the last actual one.
ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 53. Typical connection diagram using the ADC

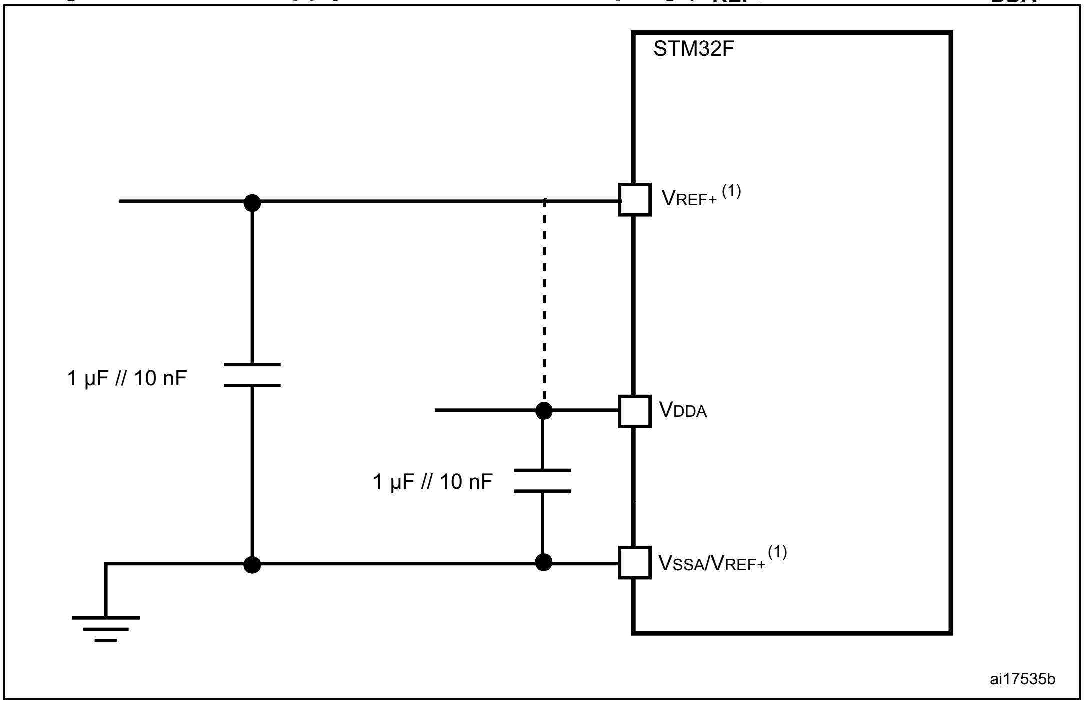


1. Refer to *Table 66* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 54* or *Figure 55*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 54. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	4	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	3	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	8	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 64. Synchronous non-multiplexed PSRAM write timings

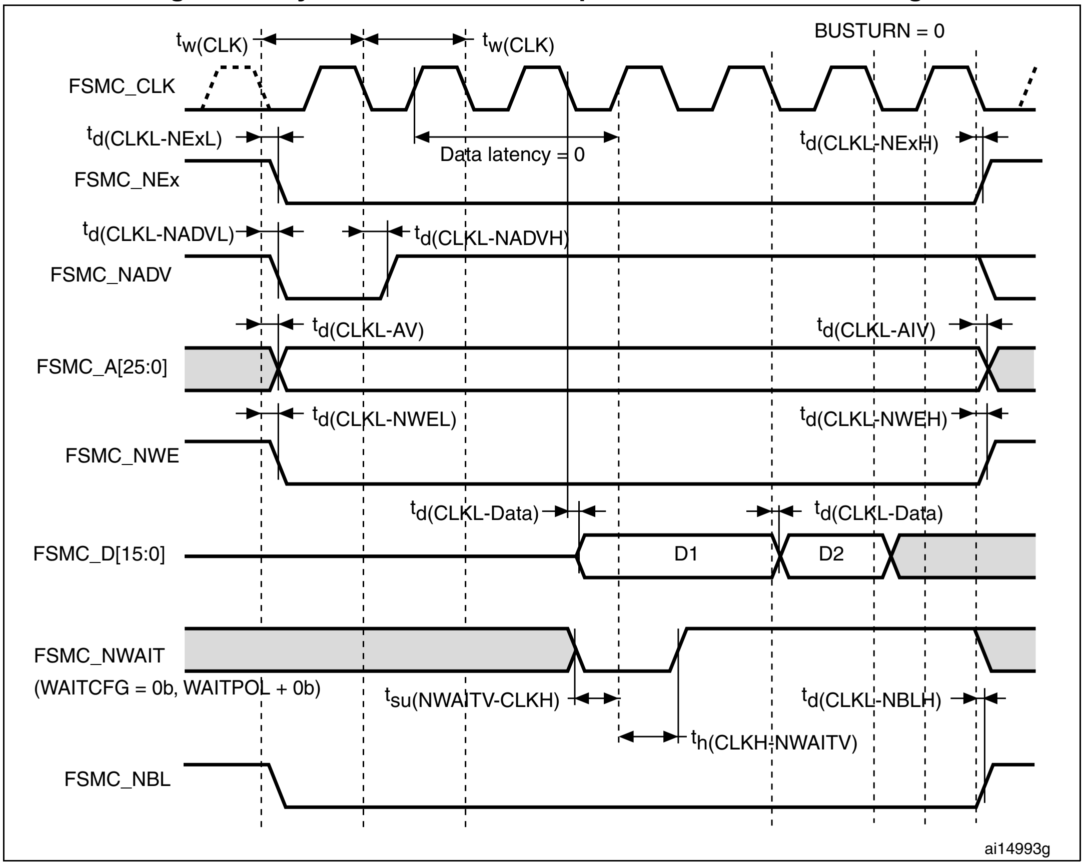


Table 79. Synchronous non-multiplexed PSRAM write timings(1)(2)

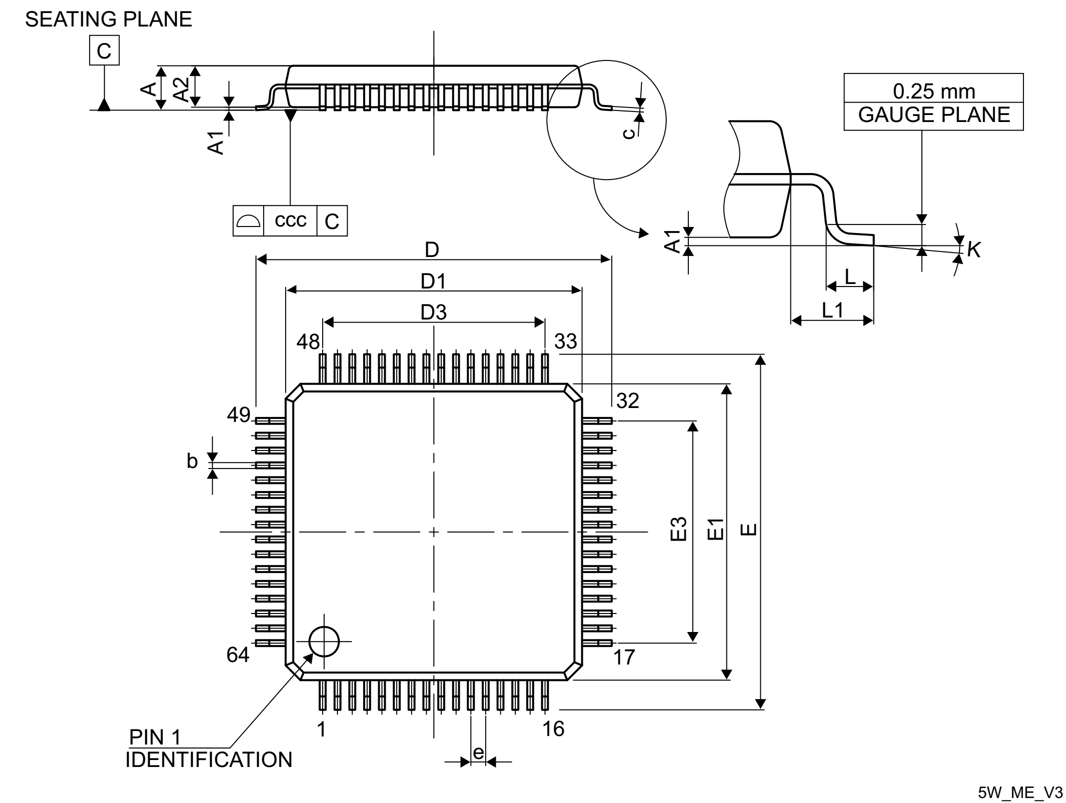
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$- 1	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J\ max = T_A\ max + (P_D\ max \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O}\ max = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 95. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch	51	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Updated *Typical and maximum current consumption* conditions, as well as *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure 23*, *Figure 24*, *Figure 25*, and *Figure 26*. Updated *Table 22: Typical and maximum current consumption in Sleep mode*, and added *Figure 27* and *Figure 28*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Added *Figure 29: Typical current consumption vs. temperature in Stop mode*. Updated *Table 24: Typical and maximum current consumptions in Standby mode* and *Table 25: Typical and maximum current consumptions in VBAT mode*. Updated *On-chip peripheral current consumption* conditions and *Table 26: Peripheral current consumption*. Updated $t_{WUSTDBY}$ and t_{WUSTOP}, and added *Note 3* in *Table 27: Low-power mode wakeup timings*. Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in *Table 28: High-speed external user clock characteristics*. Updated C and g_m in *Table 30: HSE 4-26 MHz oscillator characteristics*. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in *Table 31: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added *Note 1* and updated ACC_{HSI}, $IDD_{(HSI)}$, and $t_{su(HSI)}$ in *Table 32: HSI oscillator characteristics*. Added *Figure 34: ACCHSI versus temperature*. Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in *Table 33: LSI oscillator characteristics*. Added *Figure 35: ACCLSI versus temperature* *Table 34: Main PLL characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added *Note 2* for f_{PLL_IN} minimum and maximum values. *Table 35: PLLI2S (audio PLL) characteristics*: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added *Note 2* for f_{PLLI2S_IN} minimum and maximum values. Added *Note 1* in *Table 36: SSCG parameters constraint*. Updated *Table 37: Flash memory characteristics*. Modified *Table 38: Flash memory programming* and added *Note 2* for t_{prog}. Updated t_{prog} and added *Note 1* in *Table 39: Flash memory programming with VPP*. Modified *Figure 40: Recommended NRST pin protection*. Updated *Table 42: EMI characteristics* and EMI monitoring conditions in *Section : Electromagnetic Interference (EMI)*. Added *Note 2* related to $V_{ESD(HBM)}$in *Table 43: ESD absolute maximum ratings*. Updated *Table 48: I/O AC characteristics*. Added *Section 6.3.15: I/O current injection characteristics*. Modified maximum frequency values and conditions in *Table 48: I/O AC characteristics*. Updated $t_{res(TIM)}$ in *Table 50: Characteristics of TIMx connected to the APB1 domain*. Modified $t_{res(TIM)}$ and f_{EXT} *Table 51: Characteristics of TIMx connected to the APB2 domain*.

Table 97. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	11 (continued)	Removed Appendix A Application block diagrams. Updated *Figure 77: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 87: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 80: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 83: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*.
27-Oct-2014	12	Updated V_{BAT} voltage range in *Figure 19: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 14: General operating conditions*. Removed note 1 in *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Table 45: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 69: Temperature sensor characteristics*. Updated *Figure 79: WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline* and *Table 88: WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data*. Added *Figure 83: LQFP100 marking (package top view)* and *Figure 86: LQFP144 marking (package top view)*.
2-Feb-2016	13	Updated *Section 1: Introduction*. Updated *Table 32: HSI oscillator characteristics* and its footnotes. Updated *Figure 36: PLL output clock waveforms in center spread mode*, *Figure 37: PLL output clock waveforms in down spread mode*, *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.