



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I ² C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207zgt6

Table 2. STM32F205xx features and peripheral counts (continued)

Peripherals	STM32F205Rx				STM32F205Vx		STM32F205Zx
Operating temperatures	Ambient temperatures: −40 to +85 °C /−40 to +105 °C						
	Junction temperature: −40 to + 125 °C						
Package	LQFP64	LQFP64 WLCSP64 +2	LQFP6 4	LQFP64 WLCSP6 4+2	LQFP100		LQFP144

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD} , the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).

Table 3. STM32F207xx features and peripheral counts

Peripherals		STM32F207Vx				STM32F207Zx				STM32F207Ix			
Flash memory in Kbytes		256	512	768	1024	256	512	768	1024	256	512	768	1024
SRAM in Kbytes	System (SRAM1+SRAM2)	128 (112+16)											
	Backup	4											
FSMC memory controller		Yes ⁽¹⁾											
Ethernet		Yes											
Timers	General-purpose	10											
	Advanced-control	2											
	Basic	2											
	IWDG	Yes											
	WWDG	Yes											
RTC		Yes											
Random number generator		Yes											

Table 6. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	IrDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	1.87	7.5	APB2 (max. 60 MHz)
USART2	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
USART3	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
UART4	X	-	X	-	X	-	1.87	3.75	APB1 (max. 30 MHz)
UART5	X	-	X	-	X	-	3.75	3.75	APB1 (max. 30 MHz)
USART6	X	X	X	X	X	X	3.75	7.5	APB2 (max. 60 MHz)

3.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.24 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

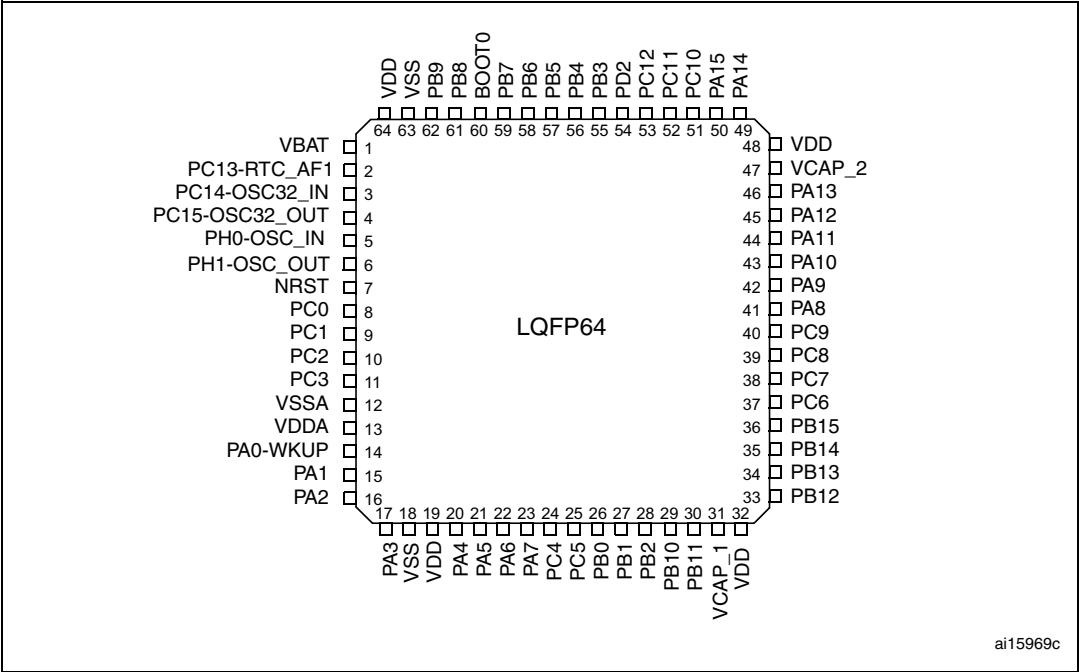
All I2Sx interfaces can be served by the DMA controller.

3.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

4 Pinouts and pin description

Figure 10. STM32F20x LQFP64 pinout



1. The above figure shows the package top view.

Figure 11. STM32F20x WLCSP64+2 ballout

	1	2	3	4	5	6	7	8	9
A	PA14	PA15	PC12	PB3	PB5	PB7	PB9	VDD	V _{BAT}
B	VSS	PA13	PC10	PB4	PB6	BOOT0	PB8	PC13	PC14
C	PA12	VCAP_2	PC11				PD2	IRROFF	PC15
D	PC9	PA11	PA10				PC2	VSS	VDD
E	VDD	PA8	PA9				PA0	NRST	PH0-OSC_IN
F	VSS	PC7	PC8				VREF+	PC1	PH1-OSC_OUT
G	PB15	PC6	PC5				PA3	PC3	PC0
H	PB14	PB13	PB10	PC4	PA6	PA5	REGOFF	PA1	VSS_5
J	PB12	PB11	VCAP_1	PB2	PB1	PB0	PA7	PA4	PA2

1. The above figure shows the package top view.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
38	F2	64	97	116	G15	PC7	I/O	FT	-	I2S3_MCK, TIM8_CH2, SDIO_D7, USART6_RX, DCMI_D1, TIM3_CH2, EVENTOUT	-
39	F3	65	98	117	G14	PC8	I/O	FT	-	TIM8_CH3, SDIO_D0, TIM3_CH3, USART6_CK, DCMI_D2, EVENTOUT	-
40	D1	66	99	118	F14	PC9	I/O	FT	-	I2S2_CKIN, I2S3_CKIN, MCO2, TIM8_CH4, SDIO_D1, I2C3_SDA, DCMI_D3, TIM3_CH4, EVENTOUT	-
41	E2	67	100	119	F15	PA8	I/O	FT	-	MCO1, USART1_CK, TIM1_CH1, I2C3_SCL, OTG_FS_SOF, EVENTOUT	-
42	E3	68	101	120	E15	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, I2C3_SMBA, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
43	D3	69	102	121	D15	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, OTG_FS_ID, DCMI_D1, EVENTOUT	-
44	D2	70	103	122	C15	PA11	I/O	FT	-	USART1_CTS, CAN1_RX, TIM1_CH4, OTG_FS_DM, EVENTOUT	-
45	C1	71	104	123	B15	PA12	I/O	FT	-	USART1_RTS, CAN1_TX, TIM1_ETR, OTG_FS_DP, EVENTOUT	-
46	B2	72	105	124	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
47	C2	73	106	125	F13	V _{CAP_2}	S	-	-	-	-
-	B1	74	107	126	F12	V _{SS}	S	-	-	-	-
48	A8	75	108	127	G13	V _{DD}	S	-	-	-	-
-	-	-	-	128	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	129	E13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
54	C7	83	116	144	D12	PD2	I/O	FT	-	TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	-	84	117	145	D11	PD3	I/O	FT	-	FSMC_CLK, USART2_CTS, EVENTOUT	-
-	-	85	118	146	D10	PD4	I/O	FT	-	FSMC_NOE, USART2_RTS, EVENTOUT	-
-	-	86	119	147	C11	PD5	I/O	FT	-	FSMC_NWE, USART2_TX, EVENTOUT	-
-	-	-	120	148	D8	V _{SS}	S	-	-	-	-
-	-	-	121	149	C8	V _{DD}	S	-	-	-	-
-	-	87	122	150	B11	PD6	I/O	FT	-	FSMC_NWAIT, USART2_RX, EVENTOUT	-
-	-	88	123	151	A11	PD7	I/O	FT	-	USART2_CK, FSMC_NE1, FSMC_NCE2, EVENTOUT	-
-	-	-	124	152	C10	PG9	I/O	FT	-	USART6_RX, FSMC_NE2, FSMC_NCE3, EVENTOUT	-
-	-	-	125	153	B10	PG10	I/O	FT	-	FSMC_NCE4_1, FSMC_NE3, EVENTOUT	-
-	-	-	126	154	B9	PG11	I/O	FT	-	FSMC_NCE4_2, ETH_MII_TX_EN, ETH_RMII_TX_EN, EVENTOUT	-
-	-	-	127	155	B8	PG12	I/O	FT	-	FSMC_NE4, USART6_RTS, EVENTOUT	-
-	-	-	128	156	A8	PG13	I/O	FT	-	FSMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-
-	-	-	129	157	A7	PG14	I/O	FT	-	FSMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, EVENTOUT	-
-	-	-	130	158	D7	V _{SS}	S	-	-	-	-

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	1.8 ⁽¹⁾	3.6	V
V_{DDA} ⁽²⁾	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD} ⁽³⁾	1.8 ⁽¹⁾	3.6	
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	
V_{IN}	Input voltage on RST and FT pins	$2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-0.3	5.5	
		$1.7\text{ V} \leq V_{DD} \leq 2\text{ V}$	-0.3	5.2	
	Input voltage on TTa pins	-	-0.3	$V_{DD}+0.3$	
	Input voltage on BOOT0 pin	-	0	9	
V_{CAP1}	Internal core voltage to be supplied externally in REGOFF mode	-	1.1	1.3	
V_{CAP2}					
P_D	Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 ⁽⁴⁾	LQFP64	-	444	mW
		WLCSP64+2	-	392	
		LQFP100	-	434	
		LQFP144	-	500	
		LQFP176	-	526	
		UFBGA176	-	513	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low-power dissipation ⁽⁵⁾	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low-power dissipation ⁽⁵⁾	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD} , the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see [Section 3.16](#)).
2. When the ADC is used, refer to [Table 66: ADC characteristics](#).
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} .
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} .

6.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 19](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 19. Embedded reset and power control block characteristics

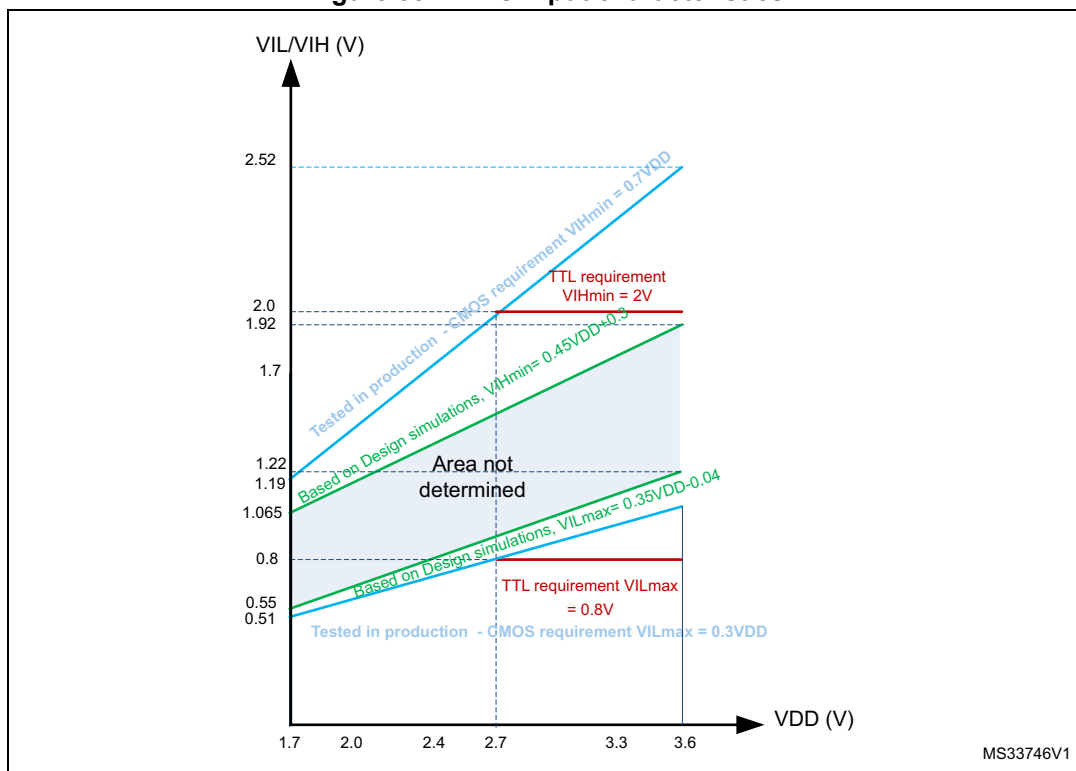
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}^{(1)}$	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f _{HCLK}	Typ	Max ⁽¹⁾		Unit
				T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled ⁽³⁾	120 MHz	61	81	93	mA
			90 MHz	48	68	80	
			60 MHz	33	53	65	
			30 MHz	18	38	50	
			25 MHz	14	34	46	
			16 MHz ⁽⁴⁾	10	30	42	
			8 MHz	6	26	38	
			4 MHz	4	24	36	
			2 MHz	3	23	35	
		External clock ⁽²⁾ , all peripherals disabled	120 MHz	33	54	66	
			90 MHz	27	47	59	
			60 MHz	19	39	51	
			30 MHz	11	31	43	
			25 MHz	8	28	41	
			16 MHz ⁽⁴⁾	6	26	38	
			8 MHz	4	24	36	
			4 MHz	3	23	35	
			2 MHz	2	23	34	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.

Figure 38. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 12](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 12](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 47](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#). All I/Os are CMOS and TTL compliant.

Table 47. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS ports $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	
$V_{OL}^{(2)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL ports $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
$V_{OL}^{(2)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-1.3$	-	
$V_{OL}^{(2)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	

- PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
- The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
- The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
- Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 39](#) and [Table 48](#), respectively.

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 48. I/O AC characteristics⁽¹⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(I/O)out}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} > 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} > 1.8 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}$, $V_{DD} > 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}$, $V_{DD} > 1.8 \text{ V}$	-	-	4	
	$t_{f(I/O)out}/$ $t_{r(I/O)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}$, $V_{DD} = 1.8 \text{ V}$ to 3.6 V	-	-	100	ns

I²S - SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 54](#) for SPI or in [Table 55](#) for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 14](#).

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 54. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	SPI1 master/slave mode	-	30	MHz
		SPI2/SPI3 master/slave mode	-	15	
$t_{r(SCL)}$ $t_{f(SCL)}$	SPI clock rise and fall time	Capacitive load: $C = 30$ pF, $f_{PCLK} = 30$ MHz	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLH)}^{(1)}$ $t_{w(SCLL)}^{(1)}$	SCK high and low time	Master mode, $f_{PCLK} = 30$ MHz, presc = 2	$t_{PCLK}-3$	$t_{PCLK}+3$	
$t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}^{(1)}$ $t_{h(SI)}^{(1)}$	Data input hold time	Master mode	5	-	
		Slave mode	4	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, $f_{PCLK} = 30$ MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}^{(1)(3)}$	Data output disable time	Slave mode	2	10	
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}^{(1)}$ $t_{h(MO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	15	-	
		Master mode (after enable edge)	2	-	

1. Guaranteed by characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

[Table 65](#) gives the list of Ethernet MAC signals for MII and [Figure 50](#) shows the corresponding timing diagram.

Figure 51. Ethernet MII timing diagram

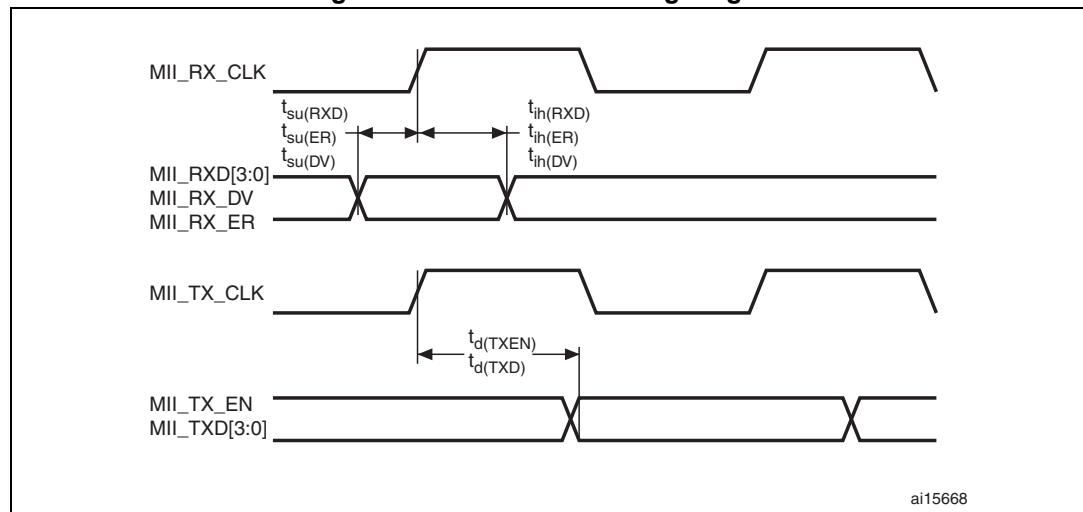


Table 65. Dynamics characteristics: Ethernet MAC signals for MII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	7.5	-	-	ns
$t_{oh}(RXD)$	Receive data hold time	1	-	-	ns
$t_{su}(DV)$	Data valid setup time	4	-	-	ns
$t_{oh}(DV)$	Data valid hold time	0	-	-	ns
$t_{su}(ER)$	Error setup time	3.5	-	-	ns
$t_{oh}(ER)$	Error hold time	0	-	-	ns
$t_d(TXEN)$	Transmit enable valid delay time	-	11	14	ns
$t_d(TXD)$	Transmit data valid delay time	-	11	14	ns

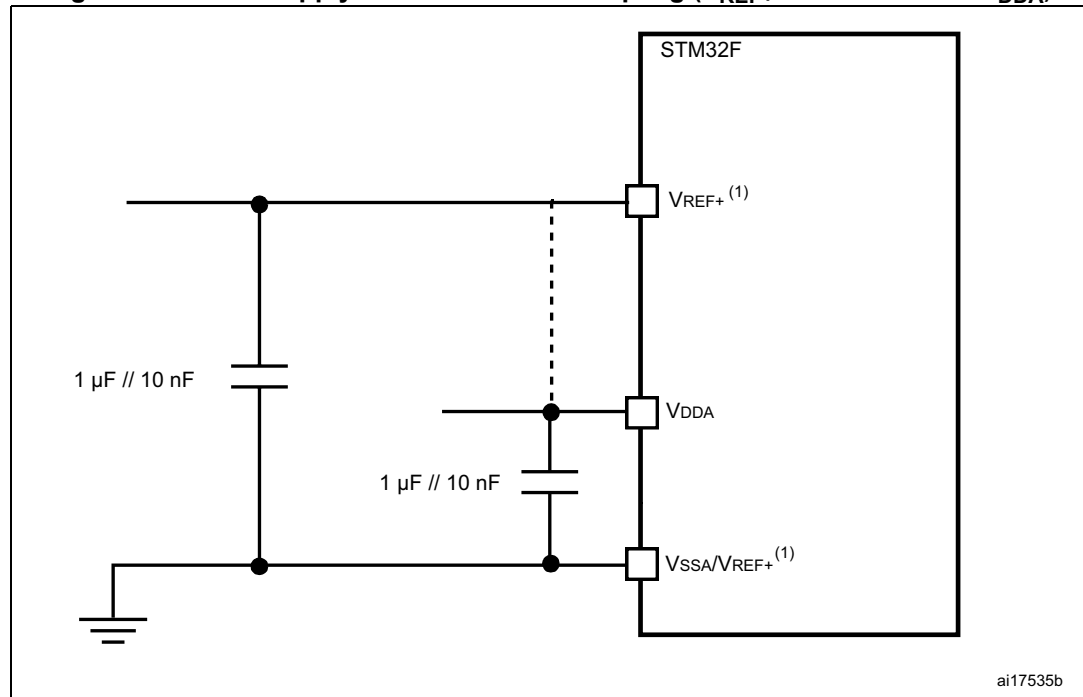
CAN (controller area network) interface

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANTX and CANRX).

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 54](#) or [Figure 55](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 54. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



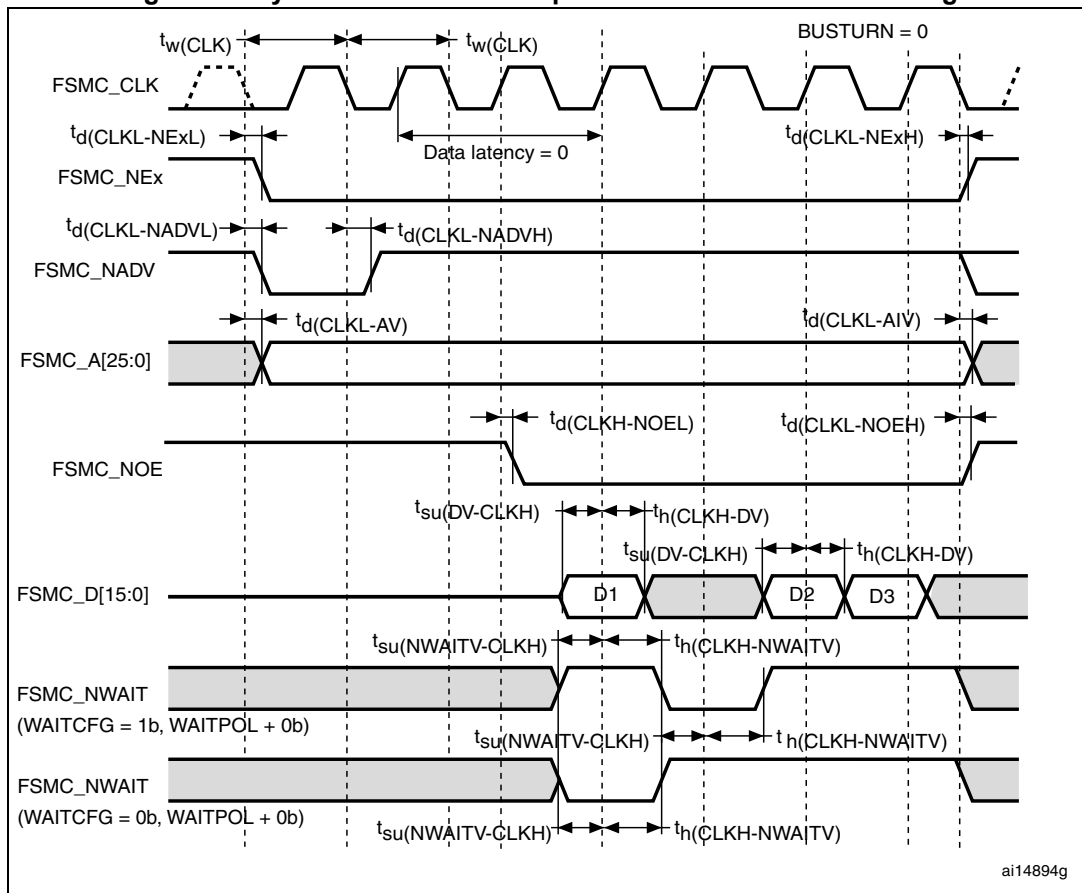
1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

Table 77. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	2	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0.5	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results, not tested in production.

Figure 63. Synchronous non-multiplexed NOR/PSRAM read timings**Table 78. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾**

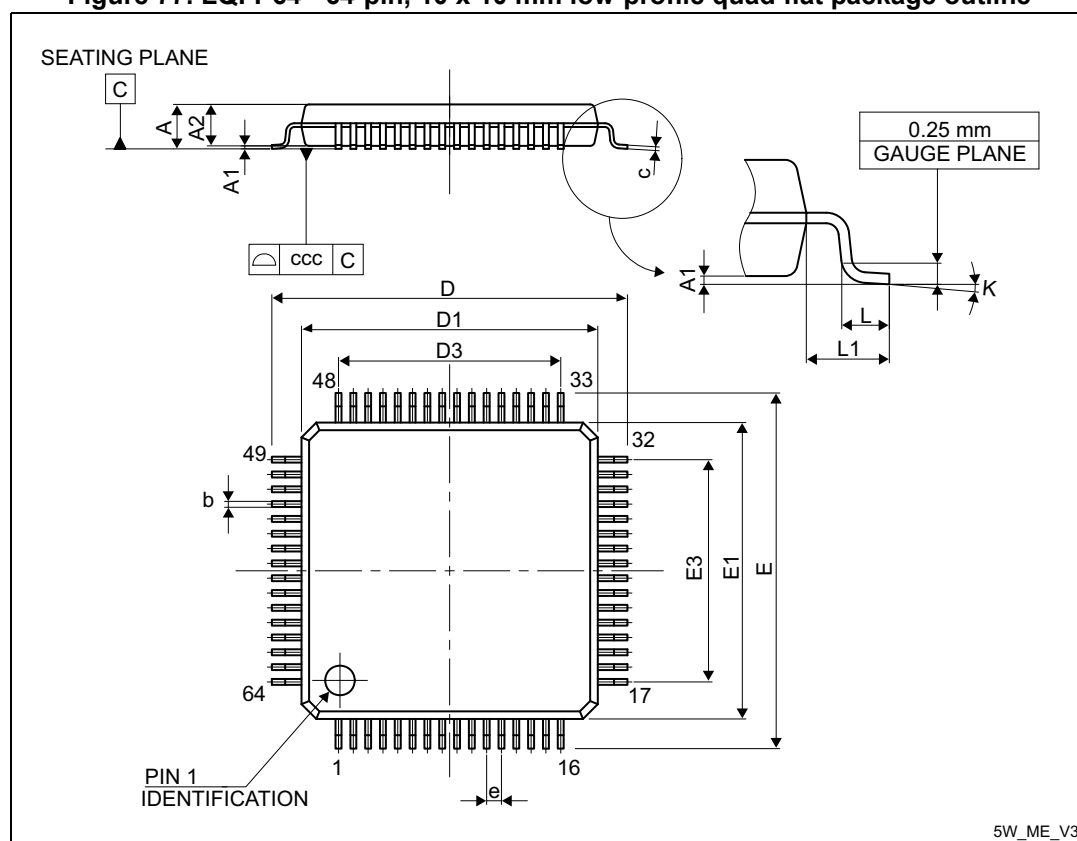
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0...2)	1	-	ns
$t_{d(CLKL-NADV)}$	FSMC_CLK low to FSMC_NADV low	-	2.5	ns

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

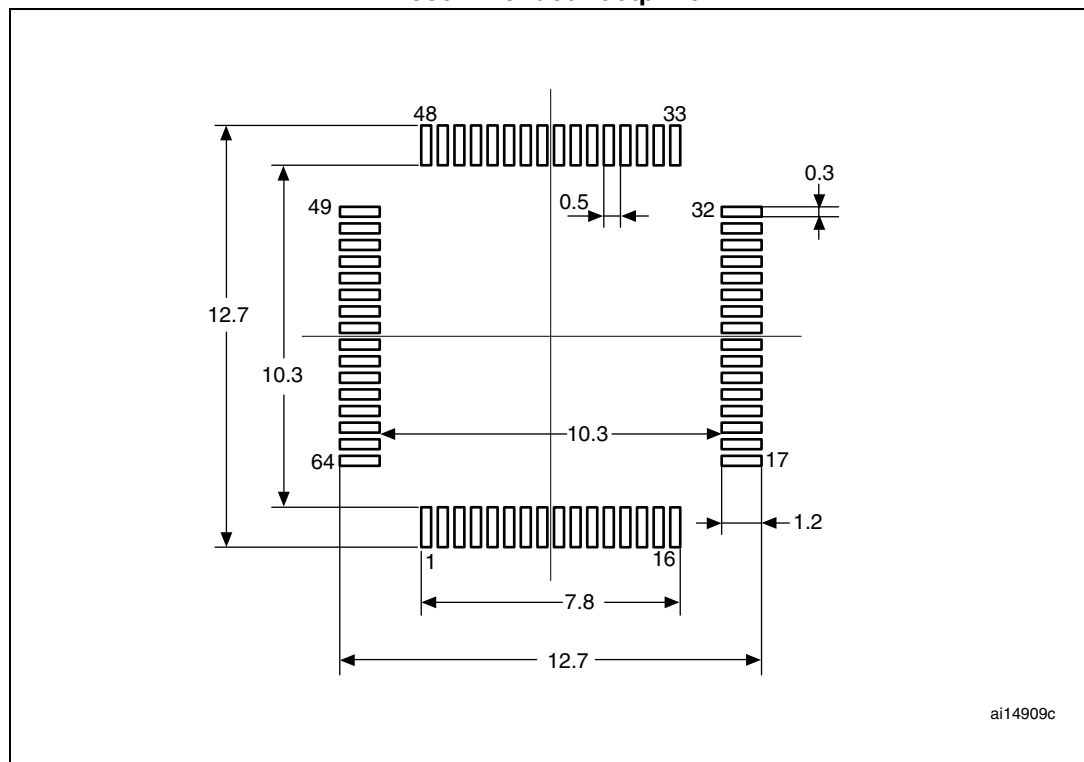
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 87. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

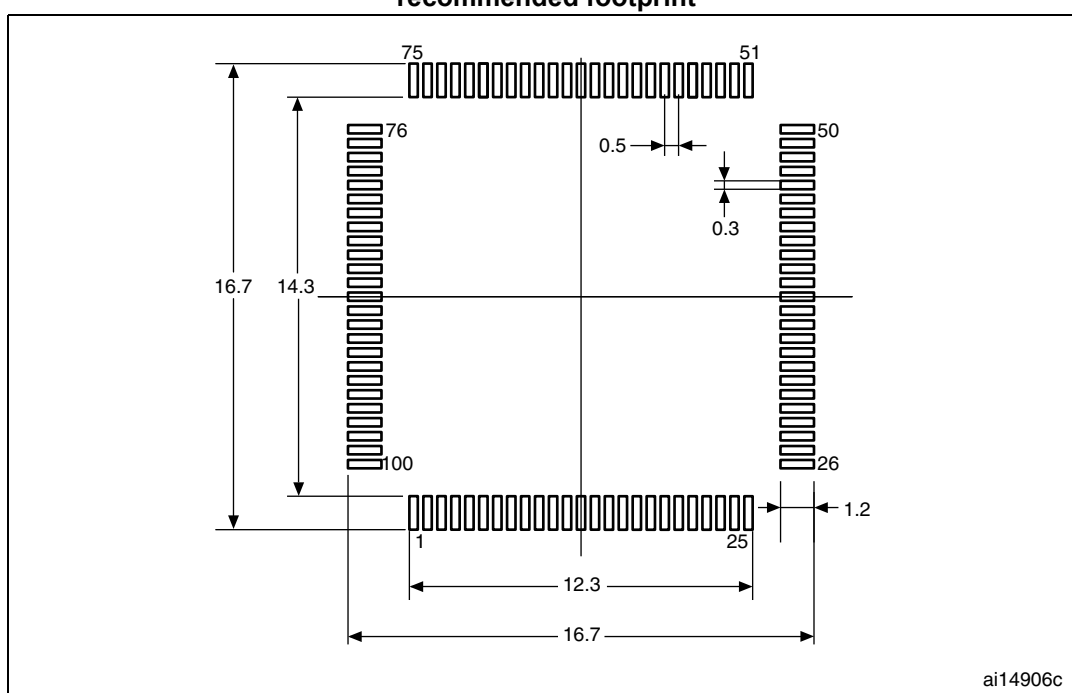
Figure 78. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

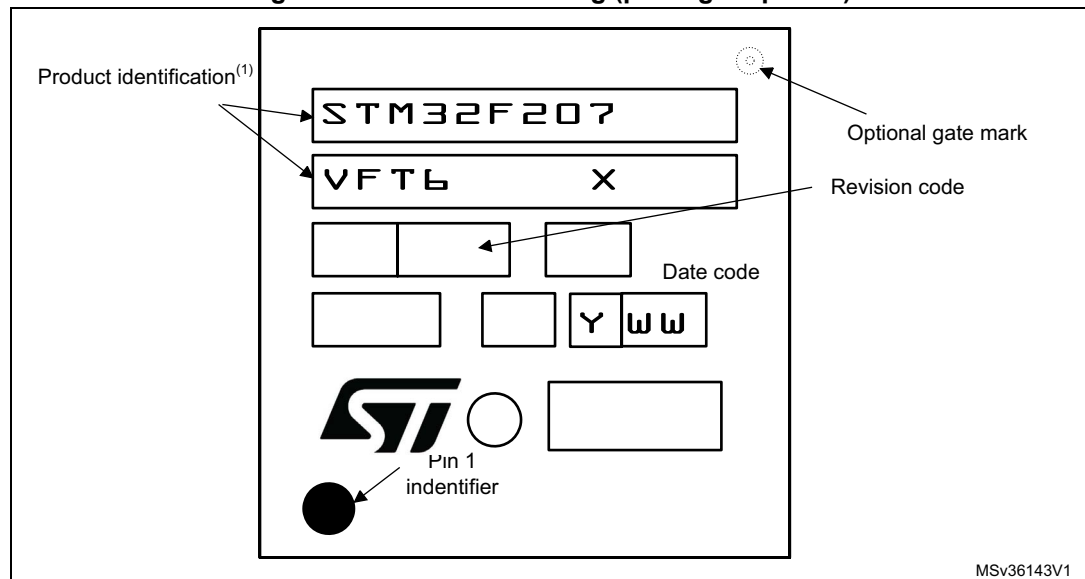
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



Device marking

Figure 83. LQFP100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 91. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 97. Document revision history (continued)

Date	Revision	Changes
22-Apr-2011	6 (continued)	Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in Table 52: I2C characteristics and in Figure 41: I2C bus AC waveforms and measurement circuit. Added Table 57: USB OTG FS DC electrical characteristics and updated Table 58: USB OTG FS electrical characteristics. Updated V_{DD} minimum value in Table 62: Ethernet DC electrical characteristics. Updated Table 66: ADC characteristics and R_{AIN} equation. Updated R_{AIN} equation. Updated Table 68: DAC characteristics. Updated t_{START} in Table 69: Temperature sensor characteristics. Updated R typical value in Table 70: VBAT monitoring characteristics. Updated Table 71: Embedded internal reference voltage. Modified FSMC_NOE waveform in Figure 57: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in Figure 61: Synchronous multiplexed NOR/PSRAM read timings, Figure 62: Synchronous multiplexed PSRAM write timings, Figure 63: Synchronous non-multiplexed NOR/PSRAM read timings, and Figure 64: Synchronous non-multiplexed PSRAM write timings. Changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in Table 76, Table 77, Table 78, and Table 79. Updated note 2 in Table 72, Table 73, Table 74, Table 75, Table 76, Table 77, Table 78, and Table 79. Modified $t_{h(NIOWR-D)}$ in Figure 70: PC Card/CompactFlash controller waveforms for I/O space write access. Modified FSMC_NCE signal in Figure 71: NAND controller waveforms for read access, Figure 72: NAND controller waveforms for write access, Figure 73: NAND controller waveforms for common memory read access, and Figure 74: NAND controller waveforms for common memory write access. Specified Full speed (FS) mode for Figure 89: USB OTG HS peripheral-only connection in FS mode and Figure 90: USB OTG HS host-only connection in FS mode.