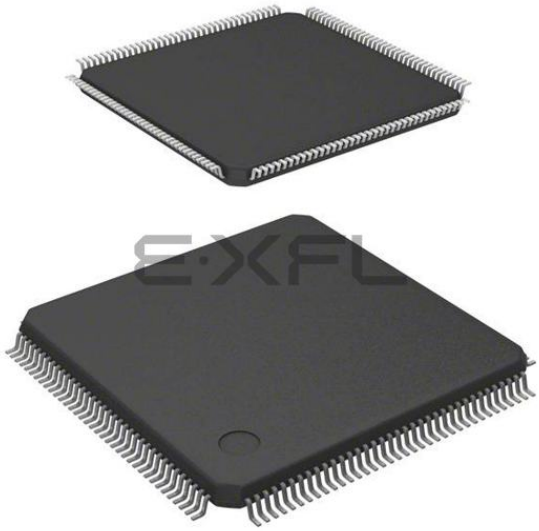

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	132K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f207zgt6j

Contents

Table 2. STM32F205xx features and peripheral counts (continued)

Peripherals	STM32F205Rx				STM32F205Vx	STM32F205Zx
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C					
	Junction temperature: –40 to + 125 °C					
Package	LQFP64	LQFP64 WLCSP64 +2	LQFP64	LQFP64 WLCSP64+2	LQFP100	LQFP144

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).

Table 3. STM32F207xx features and peripheral counts

Peripherals		STM32F207Vx				STM32F207Zx				STM32F207Ix			
Flash memory in Kbytes		256	512	768	1024	256	512	768	1024	256	512	768	1024
SRAM in Kbytes	System (SRAM1+SRAM2)	128 (112+16)											
	Backup	4											
FSMC memory controller		Yes(1)											
Ethernet		Yes											
Timers	General-purpose	10											
	Advanced-control	2											
	Basic	2											
	IWDG	Yes											
	WWDG	Yes											
RTC		Yes											
Random number generator		Yes											

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode
- LPR is used in Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost).

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Figure 19: Power supply scheme* and *Table 16: VCAP1/VCAP2 operating conditions*.

All packages have the regulator ON feature.

3.16.2 Regulator OFF

This feature is available only on packages featuring the REGOFF pin. The regulator is disabled by holding REGOFF high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 19: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used at power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection at reset or pre-reset is required.

Regulator OFF/internal reset ON

On WLCSP64+2 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS}. On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available). In this mode, V_{DD}/V_{DDA} minimum value is 1.8 V.

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

Table 6. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	1.87	7.5	APB2 (max. 60 MHz)
USART2	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
USART3	X	X	X	X	X	X	1.87	3.75	APB1 (max. 30 MHz)
UART4	X	-	X	-	X	-	1.87	3.75	APB1 (max. 30 MHz)
UART5	X	-	X	-	X	-	3.75	3.75	APB1 (max. 30 MHz)
USART6	X	X	X	X	X	X	3.75	7.5	APB2 (max. 60 MHz)

3.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.24 Inter-integrated sound (I^2S)

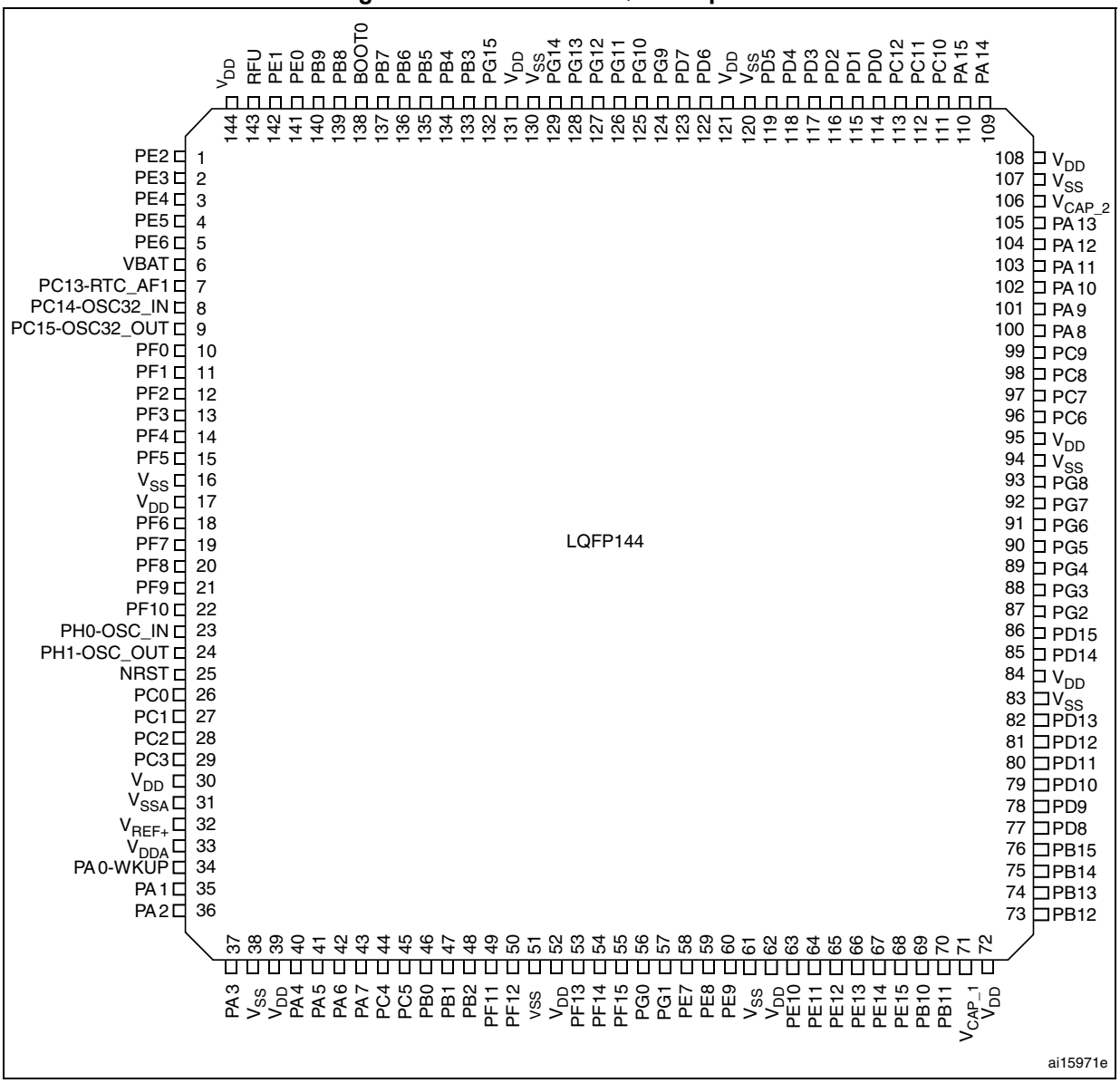
Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx interfaces can be served by the DMA controller.

3.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

Figure 13. STM32F20x LQFP144 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.
2. The above figure shows the package top view.

Table 8. STM32F20x pin and ball definitions (continued)

Pins						Pin name (function after reset)[1]	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP64	WLCSP64+2	LQFP100	LQFP144	LQFP176	UFBGA176						
-	-	98	142	170	A3	PE1	I/O	FT	-	FSMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	D5	V_{SS}	S	-	-	-	-
63	D8	-	-	-	-	V_{SS}	S	-	-	-	-
-	-	99	143	171	C6	RFU	-	-	(7)	-	-
64	D9	100	144	172	C5	V_{DD}	S	-	-	-	-
-	-	-	-	173	D4	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5, EVENTOUT	-
-	-	-	-	174	C4	PI5	I/O	FT	-	TIM8_CH1, DCMI_VSYNC, EVENTOUT	-
-	-	-	-	175	C3	PI6	I/O	FT	-	TIM8_CH2, DCMI_D6, EVENTOUT	-
-	-	-	-	176	C2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	C8	-	-	-	-	IRROFF	I/O	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F20x and STM32F21x reference manual, available from the STMicroelectronics website: www.st.com.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA176 package and if the REGOFF pin is set to V_{DD} (Regulator OFF), then PA0 is used as an internal Reset (active low).
6. FSMC_NL pin is also named FSMC_NADV on memory devices.
7. RFU means “reserved for future use”. This pin can be tied to V_{DD},V_{SS} or left unconnected.

Table 9. FSMC pin definition

Pins	FSMC				LQFP100
	CF	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	A23	A23	-	Yes
PE3	-	A19	A19	-	Yes
PE4	-	A20	A20	-	Yes

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency (f_{CPUmax}= 120 MHz)(1)	I/O operation	FSMC_CLK frequency for synchronous accesses	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(2)	Conversion time up to 1 Msps	16 MHz with no Flash memory wait state	7(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1 Msps	18 MHz with no Flash memory wait state	6(3)	– Degraded speed performance – No I/O compensation	Up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2 Msps	24 MHz with no Flash memory wait state	4(3)	– Degraded speed performance – I/O compensation works	Up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2 Msps	30 MHz with no Flash memory wait state	3(3)	– Full-speed operation – I/O compensation works	– Up to 60 MHz when V_{DD} = 3.0 to 3.6 V – Up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency (see *Figure 21*).
2. On devices in WLCSP64+2 package, if IRROFF is set to V_{DD}, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor (see *Section 3.16*).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Figure 27. Typical current consumption vs. temperature in Sleep mode, peripherals ON

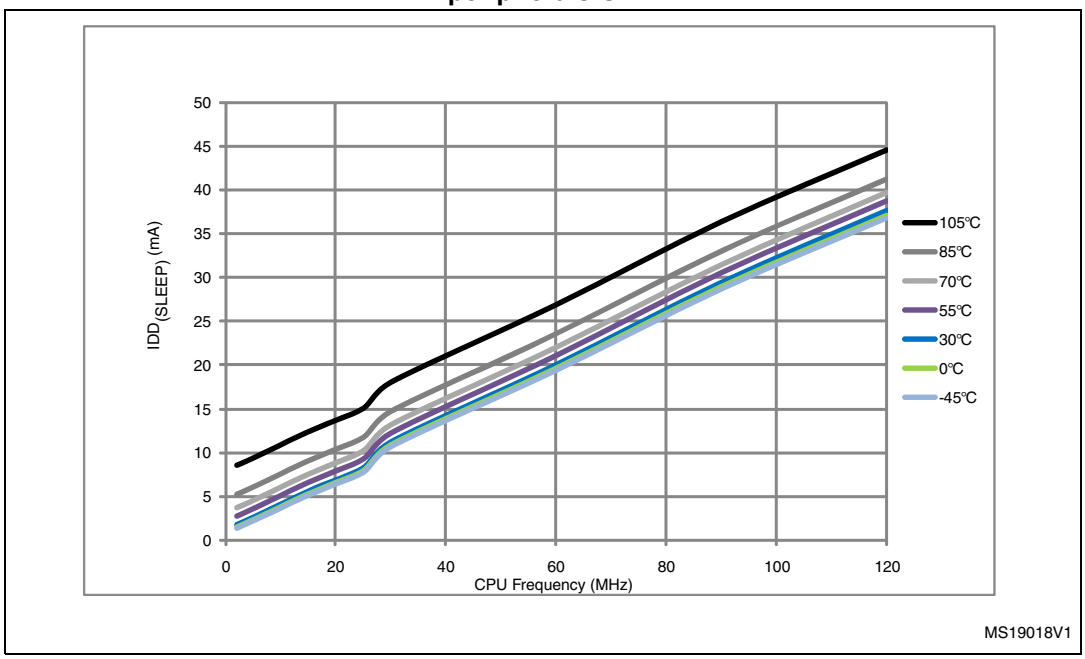


Figure 28. Typical current consumption vs. temperature in Sleep mode, peripherals OFF

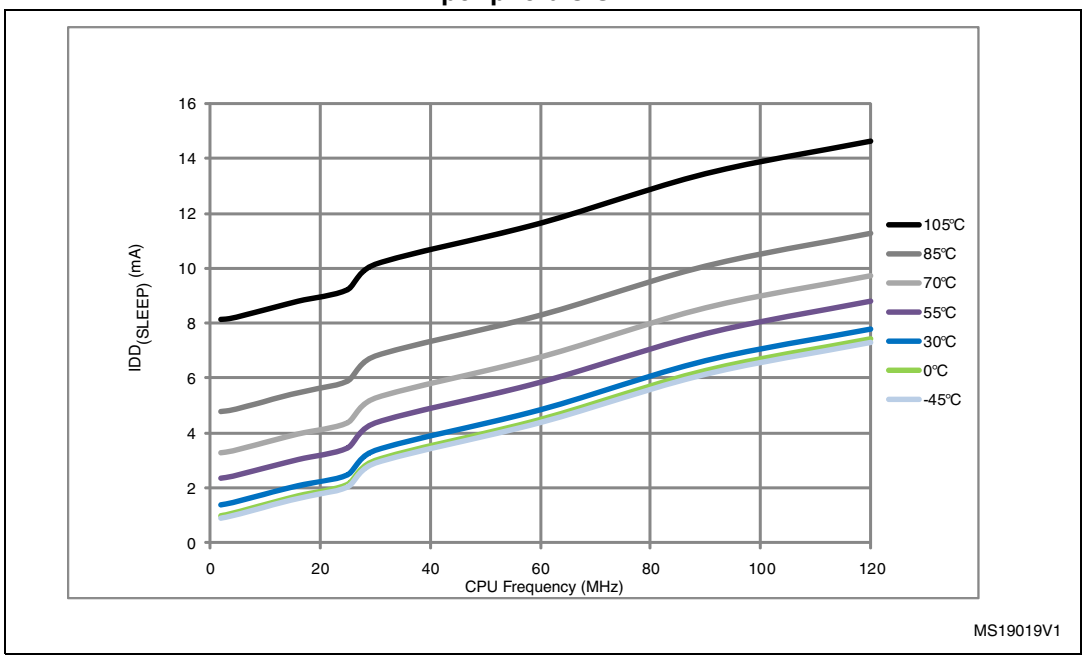
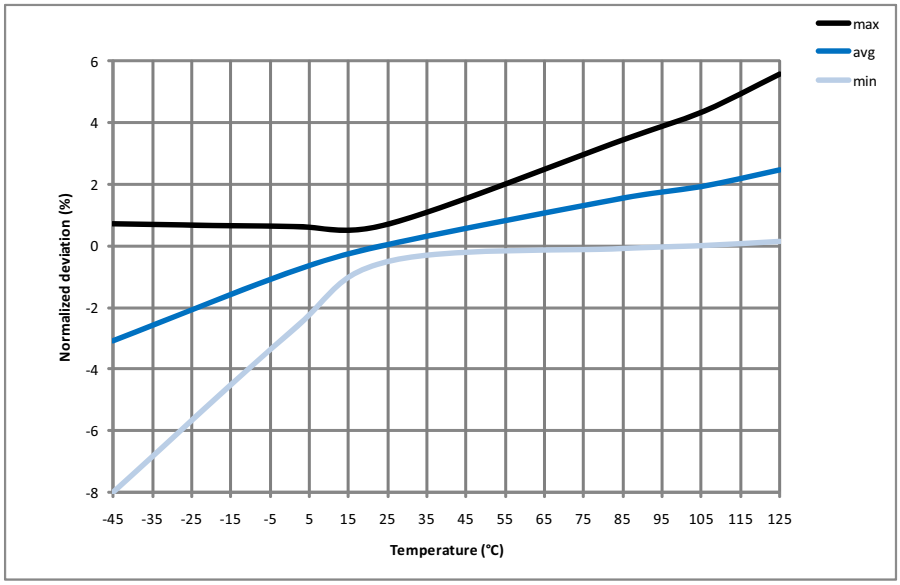


Figure 34. ACC_{HSI} versus temperature



Low-speed internal (LSI) RC oscillator

Table 33. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

Table 55. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master, 16-bit data, audio frequency = 48 kHz, main clock disabled	1.23	1.24	MHz
		Slave	0	$64F_S$ (1)	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF	-	(2)	ns
$t_{v(WS)}$ (3)	WS valid time	Master	0.3	-	
$t_{h(WS)}$ (3)	WS hold time	Master	0	-	
$t_{su(WS)}$ (3)	WS setup time	Slave	3	-	
$t_{h(WS)}$ (3)	WS hold time	Slave	0	-	
$t_{w(CKH)}$ (3) $t_{w(CKL)}$ (3)	CK high and low time	Master f_{PCLK}= 30 MHz	396	-	
$t_{su(SD\_MR)}$ (3) $t_{su(SD\_SR)}$ (3)	Data input setup time	Master receiver Slave receiver	45 0	-	
$t_{h(SD\_MR)}$ (3)(4) $t_{h(SD\_SR)}$ (3)(4)	Data input hold time	Master receiver: f_{PCLK}= 30 MHz, Slave receiver: f_{PCLK}= 30 MHz	13 0	-	
$t_{v(SD\_ST)}$ (3)(4)	Data output valid time	Slave transmitter (after enable edge)	-	30	
$t_{h(SD\_ST)}$ (3)	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_MT)}$ (3)(4)	Data output valid time	Master transmitter (after enable edge)	-	6	
$t_{h(SD\_MT)}$ (3)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. F_S is the sampling frequency. Refer to the I2S section of the STM32F20xxx/21xxx reference manual for more details. f_{CK} values reflect only the digital peripheral behavior which leads to a minimum of (I2SDIV/(2*I2SDIV+ODD), a maximum of (I2SDIV+ODD)/(2*I2SDIV+ODD) and F_S maximum values for each mode/condition.
2. Refer to *Table 48: I/O AC characteristics*.
3. Guaranteed by design, not tested in production.
4. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PLCLK} =125 ns.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 56. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 57. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

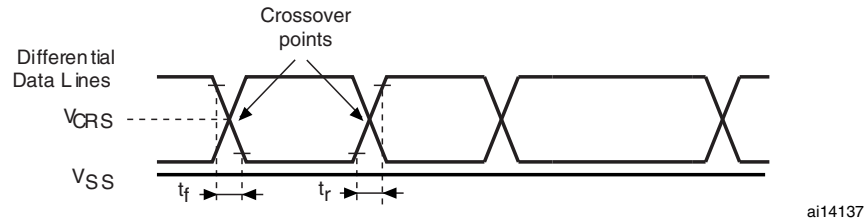


Table 58. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Table 59 shows the USB HS operating voltage.

Table 59. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

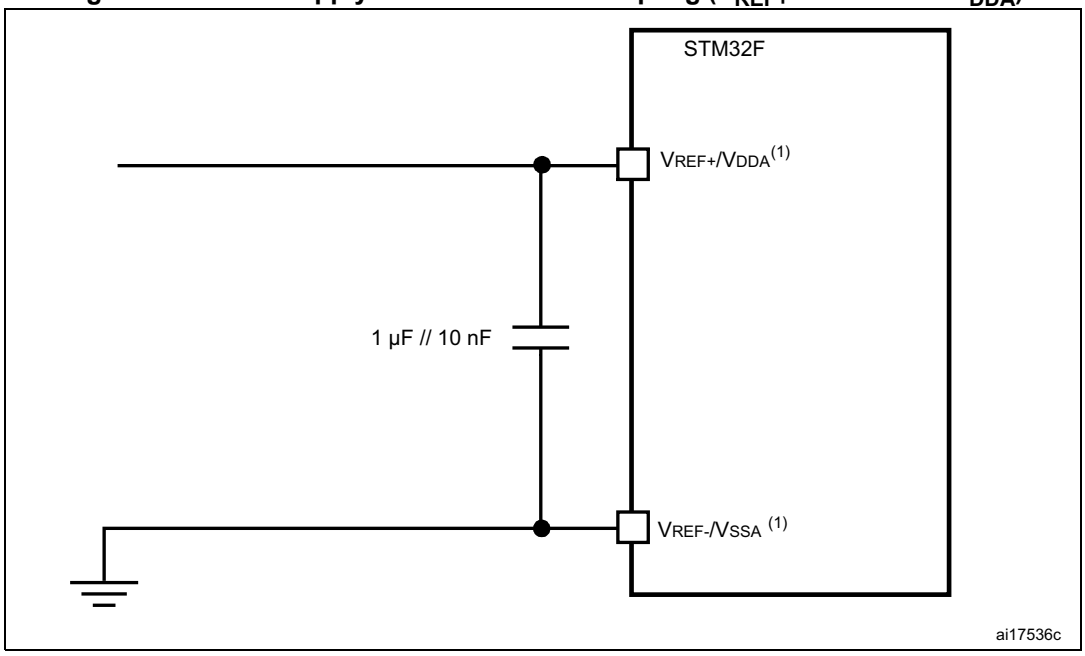
1. All the voltages are measured from the local ground potential.

Table 60. Clock timing parameters

Parameter(1)		Symbol	Min	Nominal	Max	Unit
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design, not tested in production.

Figure 55. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 DAC electrical characteristics

Table 68. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.8(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	

Table 77. Synchronous multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	2	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0.5	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 63. Synchronous non-multiplexed NOR/PSRAM read timings

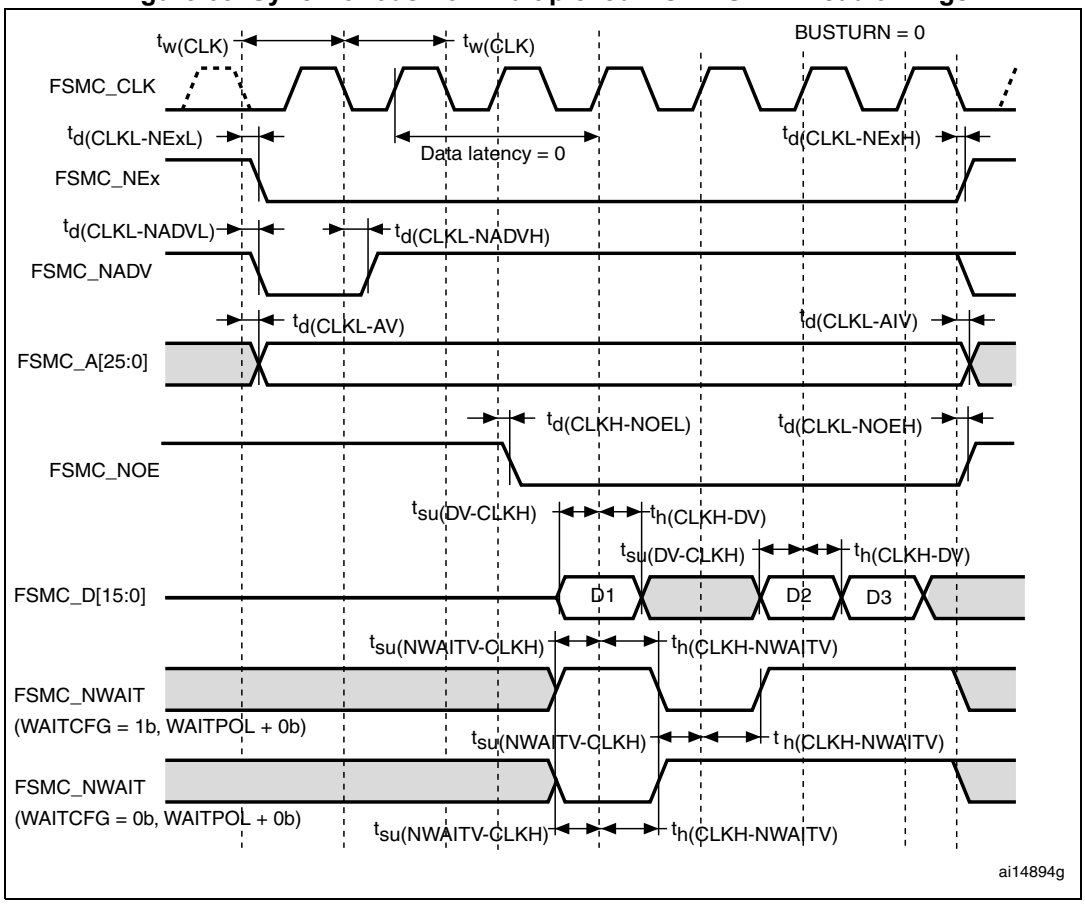


Table 78. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2.5	ns

Table 81. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK}$ - 0.5	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}$- 1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}$- 3	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}$+ 1.5	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}$+ 1	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}$– 0.5	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}$+ 1	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 71 through *Figure 74* represent synchronous waveforms, together with *Table 82* and *Table 83* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 93. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

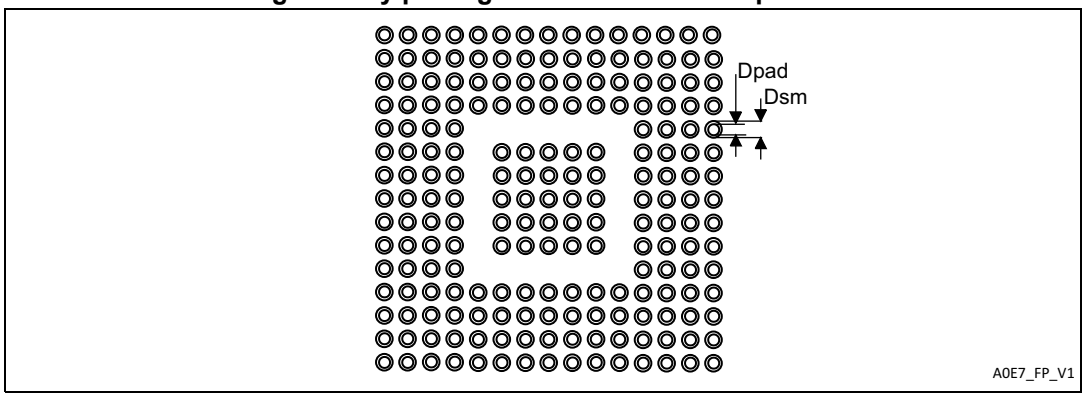


Table 94. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Table 97. Document revision history (continued)

Date	Revision	Changes
25-Nov-2010	5	Update I/Os in *Section : Features*. Added WLCSP64+2 package. Added note 1 related to LQFP176 on cover page. Added trademark for ART accelerator. Updated *Section 3.2: Adaptive real-time memory accelerator (ART Accelerator™)*. Updated *Figure 5: Multi-AHB matrix*. Added case of BOR inactivation using IRROFF on WLCSP devices in *Section 3.15: Power supply supervisor*. Reworked *Section 3.16: Voltage regulator* to clarify regulator off modes. Renamed PDROFF, IRROFF in the whole document. Added *Section 3.19: VBAT operation*. Updated LIN and IrDA features for UART4/5 in *Table 6: USART feature comparison*. *Table 8: STM32F20x pin and ball definitions*: Modified V_{DD_3} pin, and added note related to the FSMC_NL pin; renamed BYPASS-REG REGOFF, and add IRROFF pin; renamed USART4/5 UART4/5. USART4 pins renamed UART4. Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use. Updated maximum HSE crystal frequency to 26 MHz. *Section 6.2: Absolute maximum ratings*: Updated V_{IN} minimum and maximum values and note related to five-volt tolerant inputs in *Table 11: Voltage characteristics*. Updated $I_{INJ(PIN)}$ maximum values and related notes in *Table 12: Current characteristics*. Updated V_{DDA} minimum value in *Table 14: General operating conditions*. Added Note 2 and updated Maximum CPU frequency in *Table 15: Limitations depending on the operating power supply range*, and added *Figure 21: Number of wait states versus fCPU and VDD range*. Added brownout level 1, 2, and 3 thresholds in *Table 19: Embedded reset and power control block characteristics*. Changed f_{OSC_IN} maximum value in *Table 30: HSE 4-26 MHz oscillator characteristics*. Changed f_{PLL_IN} maximum value in *Table 34: Main PLL characteristics*, and updated jitter parameters in *Table 35: PLLI2S (audio PLL) characteristics*. *Section 6.3.16: I/O port characteristics*: updated V_{IH} and V_{IL} in *Table 48: I/O AC characteristics*. Added *Note 1* below *Table 47: Output voltage characteristics*. Updated R_{PD} and R_{PU} parameter description in *Table 57: USB OTG FS DC electrical characteristics*. Updated V_{REF+} minimum value in *Table 66: ADC characteristics*. Updated *Table 71: Embedded internal reference voltage*. Removed Ethernet and USB2 for 64-pin devices in *Table 101: Main applications versus package for STM32F2xxx microcontrollers*. Added *A.2: USB OTG full speed (FS) interface solutions*, removed “OTG FS connection with external PHY” figure, updated *Figure 87*, *Figure 88*, and *Figure 90* to add STULPI01B.

Table 97. Document revision history (continued)

Date	Revision	Changes
04-Nov-2013	11 (continued)	Removed Appendix A Application block diagrams. Updated *Figure 77: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 87: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 80: LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 83: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline*, *Figure 86: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline*. Updated *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline* and *Figure 88: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline*.
27-Oct-2014	12	Updated V_{BAT} voltage range in *Figure 19: Power supply scheme*. Added caution note in *Section 6.1.6: Power supply scheme*. Updated V_{IN} in *Table 14: General operating conditions*. Removed note 1 in *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Table 45: I/O current injection susceptibility*, *Section 6.3.16: I/O port characteristics* and *Section 6.3.17: NRST pin characteristics*. Removed note 3 in *Table 69: Temperature sensor characteristics*. Updated *Figure 79: WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline* and *Table 88: WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data*. Added *Figure 83: LQFP100 marking (package top view)* and *Figure 86: LQFP144 marking (package top view)*.
2-Feb-2016	13	Updated *Section 1: Introduction*. Updated *Table 32: HSI oscillator characteristics* and its footnotes. Updated *Figure 36: PLL output clock waveforms in center spread mode*, *Figure 37: PLL output clock waveforms in down spread mode*, *Figure 54: Power supply and reference decoupling (VREF+ not connected to VDDA)* and *Figure 55: Power supply and reference decoupling (VREF+ connected to VDDA)*. Updated *Section 7: Package information* and its subsections.