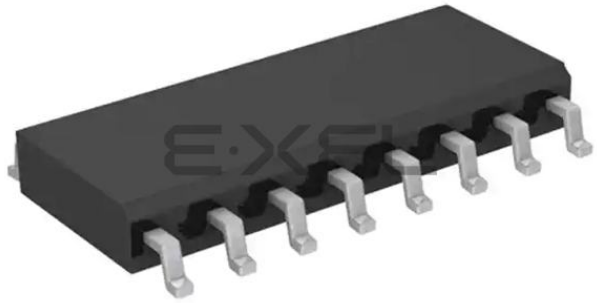
Nuvoton Technology Corporation - N79E8432ASG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e8432asg

Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Symbol	Definition	Address	MSB							LSB	Reset Value[1]
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P3M2	Port 3 output mode 2	97H	-	-	-	-	-	ENCLK	P3M2.1	P3M2.0	00000000B
P3M1	Port 3 output mode 1	96H	P3S	-	P1S	P0S	T1OE	T0OE	P3M1.1	P3M1.0	00000000B
DIVM	CPU Clock Divide Register	95H	DIVM[7:0]								0000 0000B
CAPCON2	Input capture control 2	94H	-	-	ENF1	ENF0	-	-	-	-	0000 0000B
CAPCON1	Input capture control 1	93H	-	-			CAP1LS1[2:0]		CAP1LS1[2:0]		0000 0000B
CAPCON0	Input capture control 0	92H	-	-	CAPEN1	CAPEN0	-	-	CAPF1	CAPF0	0000 0000B
P1	Port 1	90H	(97) P17	(96) P16	-	(94) P14	(93) P13	(92) P12	(91) P11	(90) P10	1111 1111B
CKCON	Clock control	8EH	-	-	-	T1M	T0M	-	-	-	0000 0000B
TH1	Timer high 1	8DH	TH1[7:0]								0000 0000B
TH0	Timer high 0	8CH	TH0[7:0]								0000 0000B
TL1	Timer low 1	8BH	TL1[7:0]								0000 0000B
TL0	Timer low 0	8AH	TL0[7:0]								0000 0000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power control	87H	SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL	Power-on 0001 0000B Other reset 000u 0000B
DPH	Data pointer high	83H	DPH[7:0]								0000 0000B
DPL	Data pointer low	82H	DPL[7:0]								0000 0000B
SP	Stack pointer	81H	SP[7:0]								0000 0111B
P0	Port 0	80H	(87) P07	(86) P06	(85) P05	(84) P04	(83) P03	(82) P02	(81) P01	(80) P00	1111 1111B

Note: Bits marked in "-" should be kept in their own initial states. User should never change their values.

Note:

[1.] ( ) item means the bit address in bit-addressable SFRs.

[2.] BODEN, BOV and BORST are initialized by CONFIG2 at power-on reset, and keep unchanged at any other resets. If BODEN=1, BOF will be automatically set by hardware at power-on reset, and keeps unchanged at any other resets.

[3.] Initialized by power-on reset. WDTEN=/CWDTEN; BS=/CBS;

[4.] With TA-Protection. (Time Access Protection)

[5.] Notation “C” means the bit is defined by CONFIG-bits; “U” means the bit is unchanged after any reset except power-on reset.

[6.] Reset value symbol description. 0: logic 0, 1: logic 1, U: unchanged, X:, C: initial by CONFIG.

8 General 80C51 System Control

A or ACC – Accumulator (Bit-addressable)

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: E0H Reset value: 0000 0000B

Bit	Name	Description
7:0	ACC[7:0]	**Accumulator.** The A or ACC register is the standard 8051 accumulator for arithmetic operation.

B – B Register (Bit-addressable)

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F0H Reset value: 0000 0000B

Bit	Name	Description
7:0	B[7:0]	**B Register** The B register is the other accumulator of the standard 8051. It is used mainly for MUL and DIV operations.

SP – Stack Pointer

7	6	5	4	3	2	1	0
SP[7:0]							
R/W							

Address: 81H Reset value: 0000 0111B

Bit	Name	Description
7:0	SP[7:0]	**Stack Pointer** The Stack Pointer stores the scratch-pad RAM address where the stack begins. It is incremented before data is stored during PUSH or CALL instructions. Note that the default value of SP is 07H. It causes the stack to begin at location 08H.

10 Timers/Counters

The N79E845/844/8432 has three 16-bit programmable timers/counters.

10.1 Timers/Counters 0 and 1

Timer/Counter 0 and 1 in the N79E845/844/8432 is two 16-bit Timers/Counters. Each of them has two 8-bit registers that form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8-bit register, and TL0, the lower 8-bit register. Similar Timer/Counter 1 has two 8-bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

They have additional timer 0 or timer 1 overflow toggle output enable feature as compare to conventional timers/counters. This timer overflow toggle output can be configured to automatically toggle T0 or T1 pin output whenever a timer overflow occurs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the clock system or 1/4 of the clock system. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine-cycle at C4. If the sampled value is high in one machine-cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine-cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine-cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

The N79E845/844/8432 can operate like the standard 8051/52 family, counting at the rate of 1/12 of the clock speed, or in turbo mode, counting at the rate of 1/4 clock speed. The speed is controlled by the T0M and T1M bits in CKCON, and the default value is zero, which uses the standard 8051/52 speed.

CKCON – Clock Control

7	6	5	4	3	2	1	0
-	-	-	T1M	T0M	-	-	-
-	-	-	R/W	R/W	-	-	-

12.6 Framing Error Detection

Framing error detection is provided for asynchronous modes. (Mode 1, 2 and 3.) The framing error occurs when a valid stop bit is not detected due to the bus noise or contention. The UART can detect a framing error and notify the software.

The framing error bit, FE, is located in SCON.7. This bit normally serves as SM0. While the framing error detection enable bit SMOD0 (PCON.6) is set 1, it serves as FE flag. Actually SM0 and FE locate in different registers.

The FE bit will be set 1 via hardware while a framing error occurs. It should be cleared via software. Note that SMOD0 should be 1 while reading or writing to FE. If FE is set, any of the following frames received without any error will not clear the FE flag. The clearing has to be done via software.

12.7 Multiprocessor Communication

The communication feature of the N79E845/844/8432 enables a Master device send a multiple frame serial message to a Slave device in a multi-slave configuration. It does this without interrupting other slave devices that may be on the same serial line. UART mode 2 or 3 mode can use this feature only. After 9 data bits are received. The 9^{th} bit value is written to RB8 (SCON.2). The user can enable this function by setting SM2 (SCON.5) as logic 1 so that when the stop bit is received, the serial interrupt will be generated only if RB8 is 1. When the SM2 bit is 1, serial data frames that are received with the 9^{th} bit as 0 do not generate an interrupt. In this case, the 9^{th} bit simply separates the address from the serial data.

When the Master device wants to transmit a block of data to one of several slaves on a serial line, it first sends out an address byte to identify the target slave. Note that in this case, an address byte differs from a data byte: In an address byte, the 9^{th} bit is 1 and in a data byte, it is 0. The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its SM2 bit and prepares to receive incoming data bytes. The SM2 bits of slaves that were not addressed remain set, and they continue operating normally while ignoring the incoming data bytes.

Follow the steps below to configure multiprocessor communications:

1. Set all devices (Masters and Slaves) to UART mode 2 or 3.

2. Write the SM2 bit of all the Slave devices to 1.

3. The Master device's transmission protocol is:

   – First byte: the address, identifying the target slave device, (9^{th} bit = 1).

   – Next bytes: data, (9^{th} bit = 0).

13 Serial Peripheral Interface (SPI)

13.1 Features

The N79E845/844/8432 exists a Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between MCUs or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to F_{SYS}/16 for Master mode and F_{SYS}/4 for Slave mode, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

13.2 Functional Description

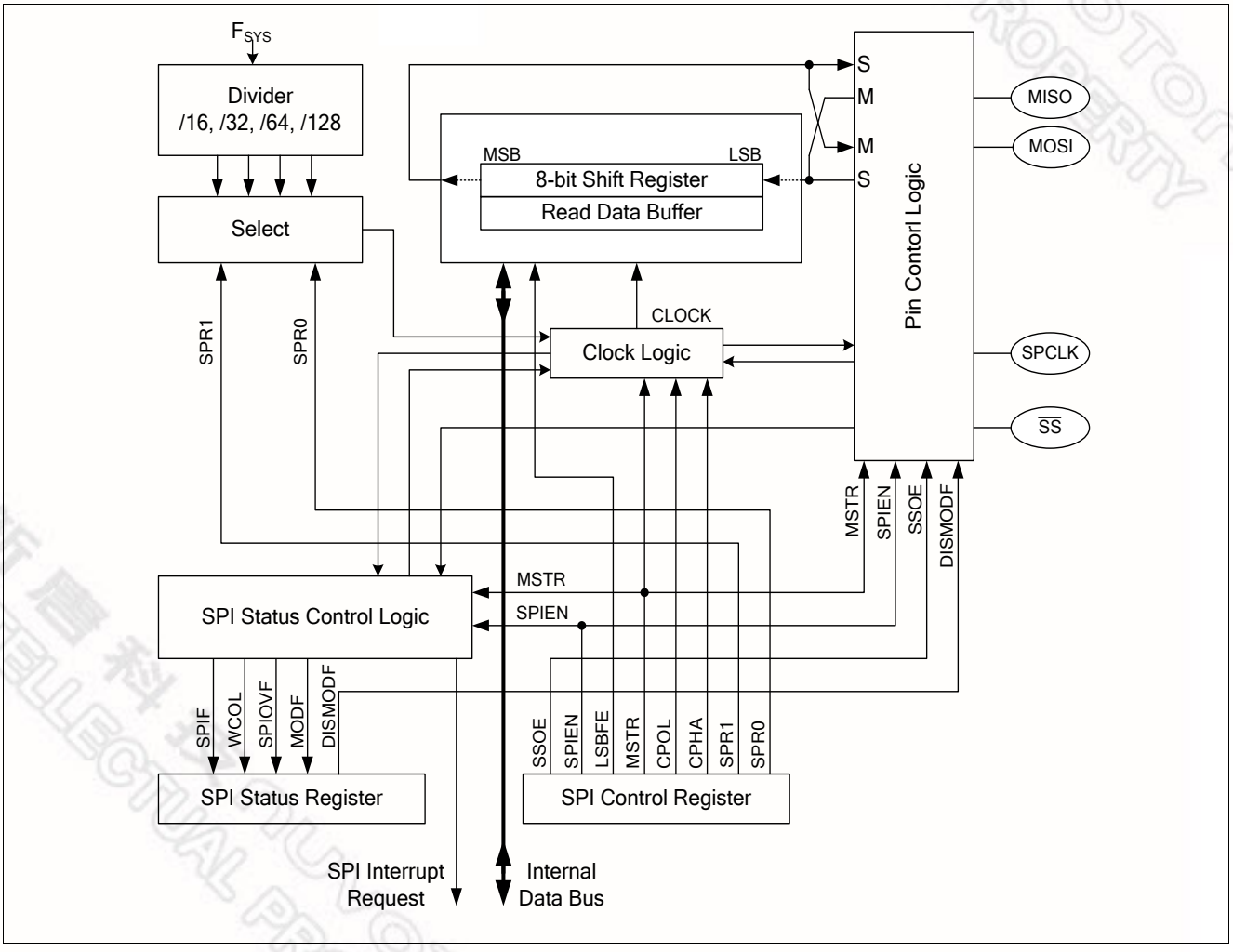


Figure 13–1 SPI Block Diagram

Figure 13–1 shows SPI block diagram and provides an overview of SPI architecture in this device. The main blocks of SPI are the SPI control register logic, SPI status logic, clock rate control logic, and pin control logic. For a serial data transfer

After the SLA+W byte has been transmitted and an acknowledge (ACK) has been returned by the addressed slave device, the SI flag is set again and I2STA is read as 18H. The appropriate action to be taken follows the user defined communication protocol by sending data continuously. After all data is transmitted, the master can send a STOP condition by setting STO (I2CON.4) and then clearing SI to terminate the transmission. A repeated START condition can be also generated without sending STOP condition to immediately initial another transmission.

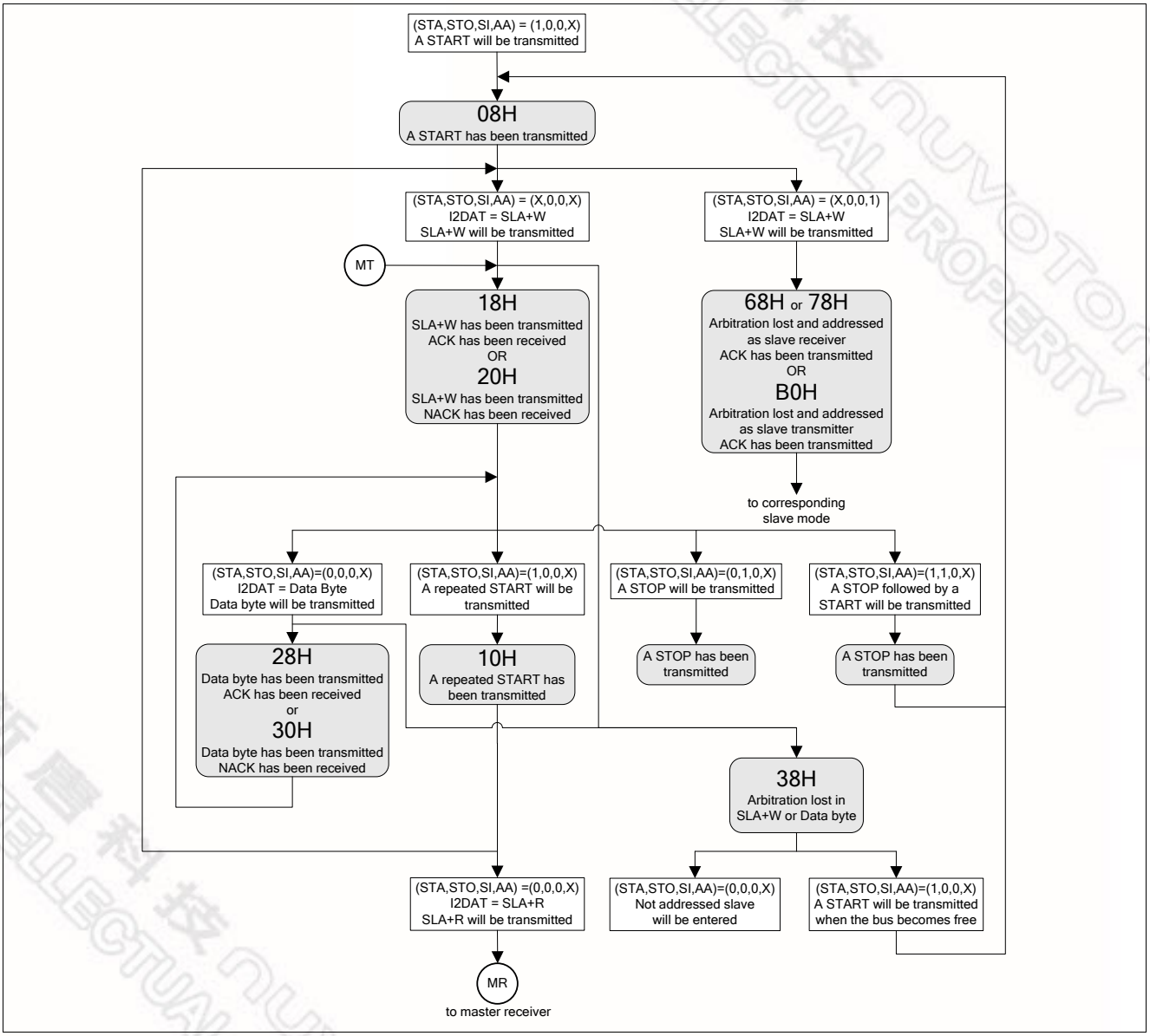


Figure 16–7 Flow and Status of Master Transmitter Mode

16.4.2 Master Receiver Mode

In the master receiver mode, several bytes of data are received from a slave transmitter. The transaction is initialized just as the master transmitter mode. Following the START condition, I2DAT should be loaded with the target slave address

After the initialization above, the I²C wait until it is addressed by its own address with the data direction bit "write" (SLA+W) or by General Call addressing. The slave receiver mode may also be entered if arbitration is lost.

After the slave is addressed by SLA+W, it should clear its SI flag to receive the data from the master transmitter. If the AA bit is 0 during a transaction, the slave will return a non-acknowledge after the next received data byte. The slave will be become not addressed and isolate with the master. It cannot receive any byte of data with I2DAT remaining the previous byte of data which is just received.

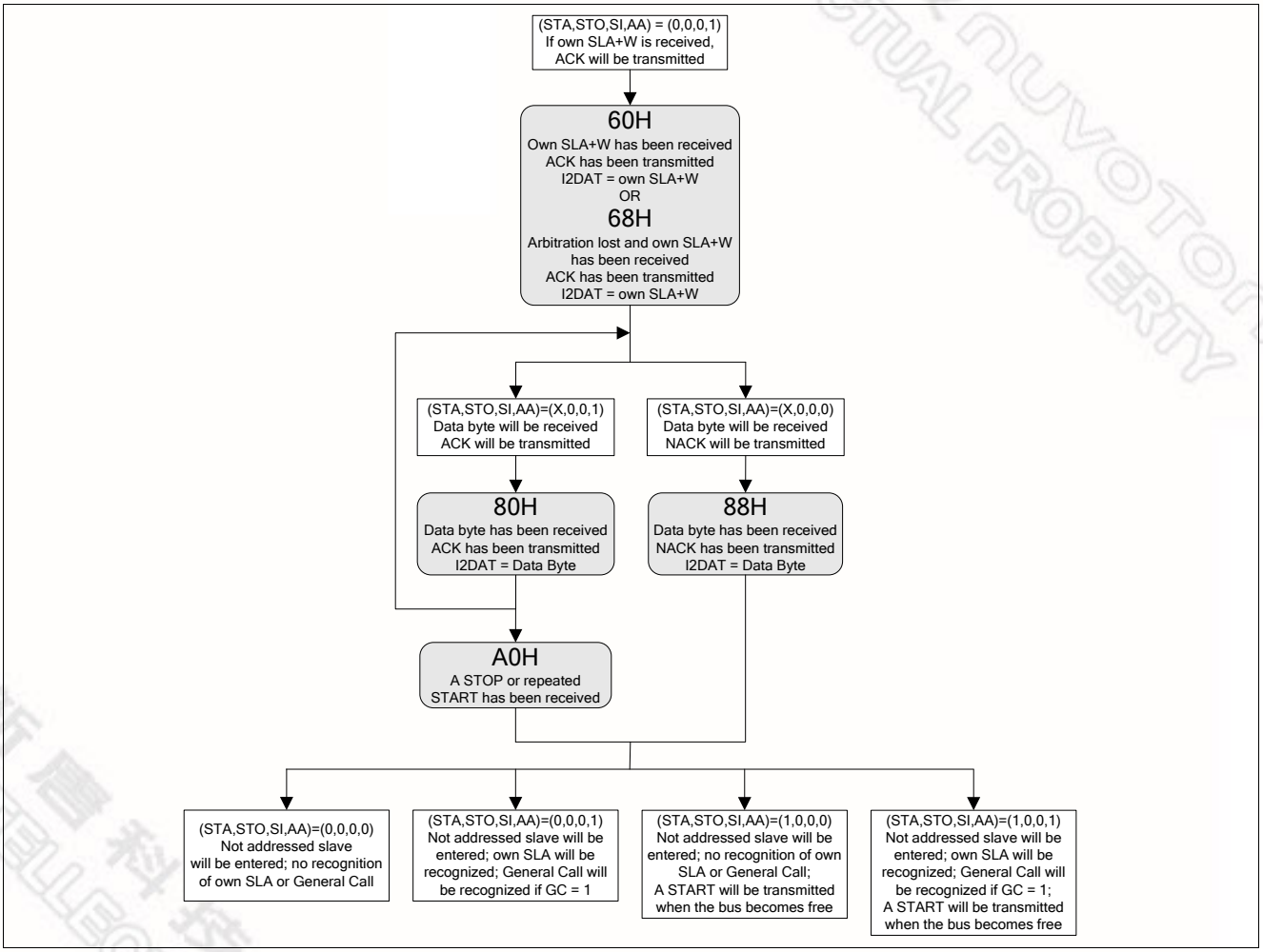


Figure 16–9 Flow and Status of Slave Receiver Mode

16.4.4 Slave Transmitter Mode

In Slave Transmitter mode, several bytes of data are transmitted to a master receiver. After I2ADDR and I2CON values are given, the I²C wait until it is addressed by its own address with the data direction bit "read" (SLA+R). The slave transmitter mode may also be entered if arbitration is lost.

After the slave is addressed by SLA+W, it should clear its SI flag to transmit the data to the master transmitter. Normally the master receiver will return an acknowledge after every byte of data is transmitted by the slave. If the acknowledge is not received, it will transmit all "1" data if it continues the transaction. It becomes a not addressed slave. If the AA flag is cleared during a transaction, the slave transmit the last byte of data. The next transmitting data will be all "1" and the slave becomes not addressed.

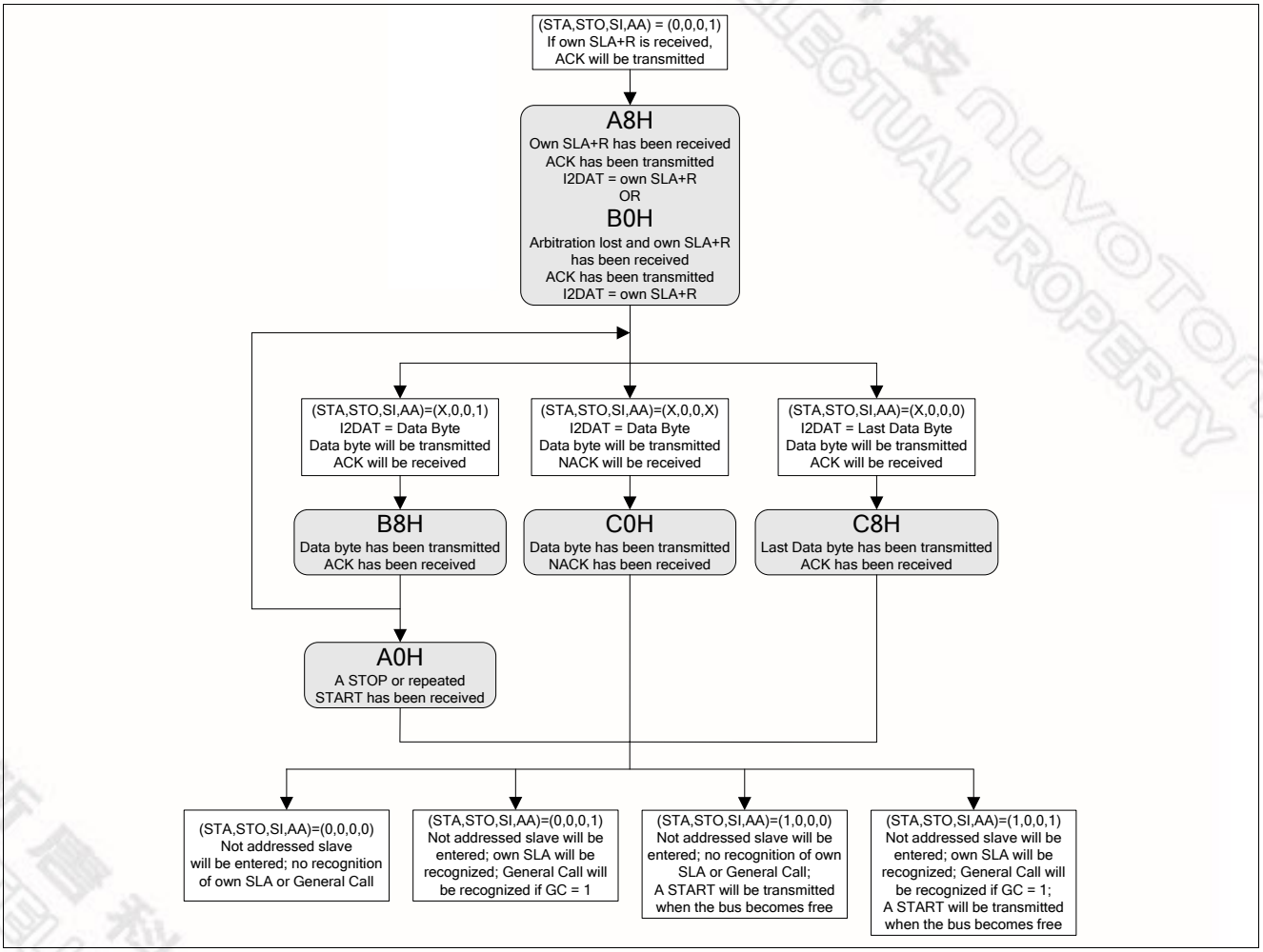


Figure 16–10 Flow and Status of Slave Transmitter Mode

16.4.5 General Call

The General Call is a special condition of slave receiver mode by sending all "0" data in slave address with data direction bit. The slave addressed by a General Call has different status codes in I2STA with normal slave receiver mode. The General Call may be also produced if arbitration is lost.

Bit	Name	Description
1	DIV	**I²C time-out Counter Clock Divider** 0 = The divider of I²C time-out counter is 1/1 of F_{SYS}. 1 = The divider of I²C time-out counter is 1/4 of F_{SYS}.
0	I2TOF	**I²C Time-out Counter Overflow Flag** I2TOF flag is set by hardware if 14-bit I²C time-out counter overflows. I2TOF flag is cleared by software.

16.7 I²C Interrupts

There are two I²C flags, SI and I2TOF. Both of them can generate an I²C event interrupt requests. If I²C interrupt mask is enabled via setting EI2C (EIE.0) and EA is 1, CPU will executes the I²C interrupt service routine once any of the two flags is set. The user needs to check flags to determine what event caused the interrupt. Both of I²C flags are cleared by software.

Table 19-1 Vector Locations for Interrupt Sources

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Timer 2 Overflow/Match	002Bh
I^2C Interrupt	0033h	KBI Interrupt	003Bh
BOD Interrupt	0043h	SPI Interrupt	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
Capture	0063h		
PWM brake Interrupt	0073h		

The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Table 19-2 Four-level Interrupt Priority

Priority bits		Interrupt Priority Level
IPXH	IPX	
0	0	Level 0 (Lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user should watch out for the status of the stack is restored to whatever after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

The N79E845/844/8432 uses a four-priority level interrupt structure. This allows great flexibility in controlling the handling of the N79E845/844/8432 many interrupt sources. The N79E845/844/8432 supports up to 14 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE or EIE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP, IPH, EIP, and EIPH registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but

not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

The following table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power-down mode.

R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Address: E8H Reset value: 0000 0000B

Bit	Name	Description
7	ET2	0 = Disable Timer 2 Interrupt. 1 = Enable Timer 2 Interrupt.
6	ESPI	SPI interrupt enable: 0 = Disable SPI Interrupt. 1 = Enable SPI Interrupt.
5	EPWM	0 = Disable PWM Interrupt when external brake pin was braked. 1 = Enable PWM Interrupt when external brake pin was braked.
4	EWDI	0 = Disable Watchdog Timer Interrupt. 1 = Enable Watchdog Timer Interrupt.
3	-	Reserved
2	ECPTF	0 = Disable capture interrupts. 1 = Enable capture interrupts.
1	EKB	0 = Disable Keypad Interrupt. 1 = Enable Keypad Interrupt.
0	EI2C	0 = Disable I^2C Interrupt. 1 = Enable I^2C Interrupt.

IP – Interrupt Priority-0 Register

7	6	5	4	3	2	1	0
PCAP	PADC	PBOD	PS	PT1	PX1	PT0	PX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: B8H Reset value: 0000 0000B

Bit	Name	Description
7	PCAP	1 = Set interrupt high priority of Capture 0/1/2 as highest priority level.
6	PADC	1 = Set interrupt priority of ADC as higher priority level.
5	PBOD	1 = Set interrupt priority of BOD Detector as higher priority level.
4	PS	1 = Set interrupt priority of Serial port 0 as higher priority level.
3	PT1	1 = Set interrupt priority of Timer 1 as higher priority level.

22 Clock System

The N79E845/844/8432 provides three options of the clock system source that is configured by F_{OSC} (CONFIG3.1~0). It switches the clock system from crystal/resonator, on-chip RC oscillator, or external clock from XTAL1 pin. The N79E845/844/8432 is embedded with an on-chip RC oscillator of 22.1184 MHz/11.0592 MHz selected by CONFIG setting, factory trimmed to ± 1% under the condition of room temperature and V_{DD}=5V. If the external clock source is from the crystal, the frequency supports from 4 MHz to 24 MHz.

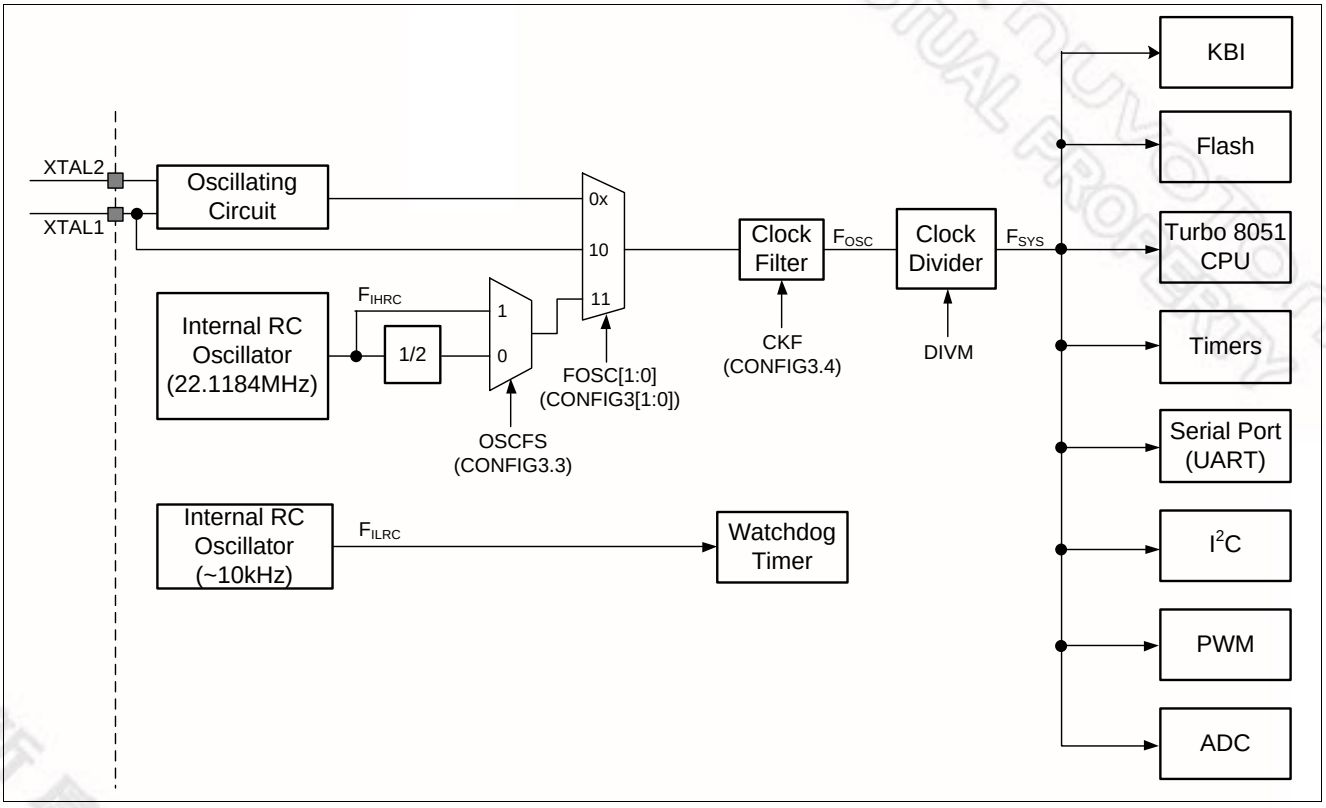


Figure 22–1 Clock System Block Diagram

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	-	-	CKF	OSCFS	-	FOSC1	FOSC0
R/W	-	-	R/W	R/W	-	R/W	R/W

Uprogrammed value: 1111 1111B

Bit	Name	Description
4	CKF	**Clock Filter Enable** 1 = Enable clock filter. It increases noise immunity and EMC capacity. 0 = Disable clock filter.
3	OSCFS	**Internal RC Oscillator Frequency Selection** 1 = Select 22.1184 MHz as the clock system if internal RC oscillator mode is used. It bypasses the divided-by-2 path of internal oscillator to select 22.1184 MHz output as the clock system source. 0 = Select 11.0592 MHz as the clock system if internal RC oscillator mode is used. The internal RC divided-by-2 path is selected. The internal oscillator is equivalent to 11.0592 MHz output used as the clock system.
2	-	**Reserved**
1:0	FOSC1 FOSC0	**Oscillator Select Bit** For chip clock source selection, refer to the following table.

(FOSC1, FOSC0)	Chip Clock Source
(1, 1)	Internal RC oscillator
(1, 0)	Reserved
(0, 1) (0, 0)	External crystal, 4 MHz ~ 24 MHz

DIVM – Clock Divider Register

7	6	5	4	3	2	1	0
DIVM[7:0]							
R/W							

Address: 95H

Reset value: 0000 0000B

Bit	Name	Description
7:0	DIVM[7:0]	**Clock Dvider** The clock system frequency F_{SYS} follows the equation below according to DIVM value. $F_{SYS} = F_{OSC}$, while DIVM = 00H. $F_{SYS} = \frac{1}{2(DIVM+1)} \times F_{OSC}$, while DIVM = 01H ~ FFH.

Bit	Name	Description
6	CBOV	**CONFIG BOD Voltage Selection** This bit select one of two BOD voltage level. CONFIG-bits CBOV / SFR BOV / BOD voltage 1 / 0 / Enable BOD= 2.7V 0 / 1 / Enable BOD= 3.8V
5	-	**Reserved**
4	CBORST	**CONFIG BOD Reset Enable** This bit decides if a BOD reset is caused after a BOD event. 1 = Enable BOD reset when V_{DD} drops below V_{BOD} or V_{DD} rises above V_{BOD}. 0 = Disable BOD reset when V_{DD} drops below V_{BOD}. Chip will assert BOF when V_{DD} drops below V_{BOD} or V_{DD} rises above V_{BOD}.

PMCR – Power Monitoring Control (TA Protected)

7	6	5	4	3	2	1	0
BODEN	BOV	-	BORST	BOF	-	-	-
R/W	R/W	-	R/W	R/W	-	-	-

Address: A3H Reset value: see Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Bit	Name	Description
7	BODEN	**BOD-detect Function Control** BODEN is initialized by inverted CBODEN (CONFIG2, bit-7) at any resets. 1 = Enable BOD detection. 0 = Disable BOD detection.
6	BOV	**BOD Voltage Select Bits** BOD are initialized at reset with the value of bits CBOV in CONFIG3-bits BOD Voltage Select bits: **CONFIG-bits CBOV** / **SFR BOV** / **BOD Voltage** 1 / 0 / Enable BOD= 2.7V 0 / 1 / Enable BOD= 3.8V
5	-	**Reserved**

CHPCON – Chip Control (TA Protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	-	-	-	BS	ISPEN
W	R/W	R/W	-	-	-	R/W	R/W

Address: 9FH Reset value: see Table 7–2 N79E845/844/8432 SFR Description and Reset Values

Bit	Name	Description
7	SWRST	**Software Reset** Setting this bit as logic 1 will cause a software reset. It will automatically be cleared via hardware after reset in finished.

The software demo code is listed below.

```
CLR EA                  ;If any interrupt is enabled, disable temporarily
MOV TA,#0AAh            ;TA protection.
MOV TA,#55h             ;
ANL CHPCON,#0FDh        ;BS = 0, reset to APROM.
MOV TA,#0AAh
MOV TA,#55h
ORL CHPCON,#80h         ;Software reset
```

24.6 Boot Selection

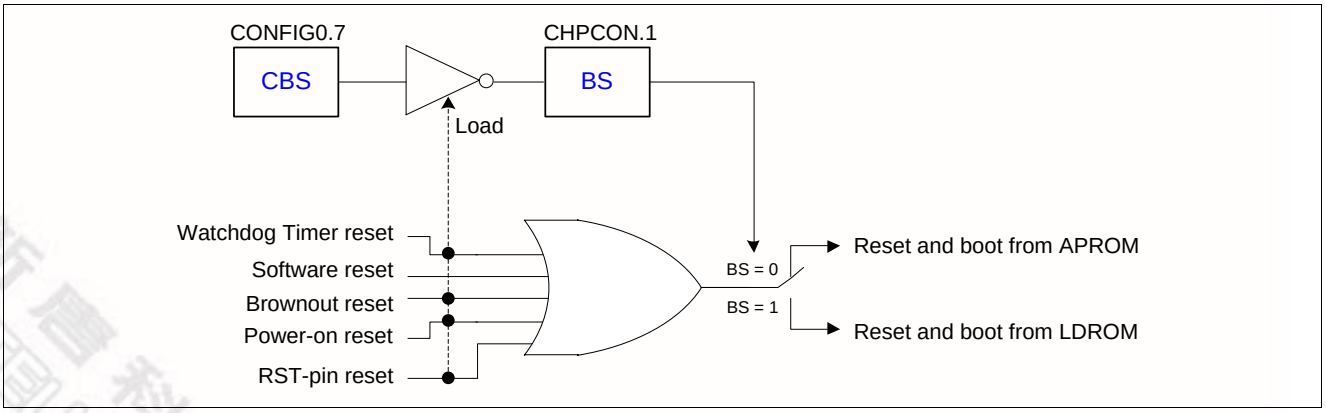


Figure 24–1 Boot Selection Diagram

The N79E845/844/8432 provides user a flexible boot selection for variant application. The SFR bit BS in CHPCON.1 determines CPU booting from APROM or LDROM after any source of reset. If reset occurs and BS is 0, CPU will reboot from APPROM. Else, the CPU will reboot from LDROM.

25 CONFIG Bits (CONFIG)

The N79E845/844/8432 has several hardware configuration bytes, called CONFIG bits, which are used to configure the hardware options such as the security bits, clock system source, and so on, which hardware options can be re-configured through the Programmer/Writer or ISP modes. The N79E845/844/8432 has four CONFIG bits those are CONFIG0~3. Several functions which are defined by certain CONFIG bits are also available to be re-configured by certain SFR bits. Therefore, there is a need to LOAD such CONFIG bits into respective SFR bits. Such loading will occurs after resets. (Software reset will reload all CONFIG bits except CBS bit in CONFIG0.7) These SFR bits can be continuously controlled via user's software. Other resets will remain the values in these SFR bits unchanged.

Note: CONFIG bits marked as "-" should always keep unprogrammed.

25.1 CONFIG0

7	6	5	4	3	2	1	0
CBS	-	-	-	-	-	LOCK	DFEN
R/W	-	-	-	-	-	R/W	R/W

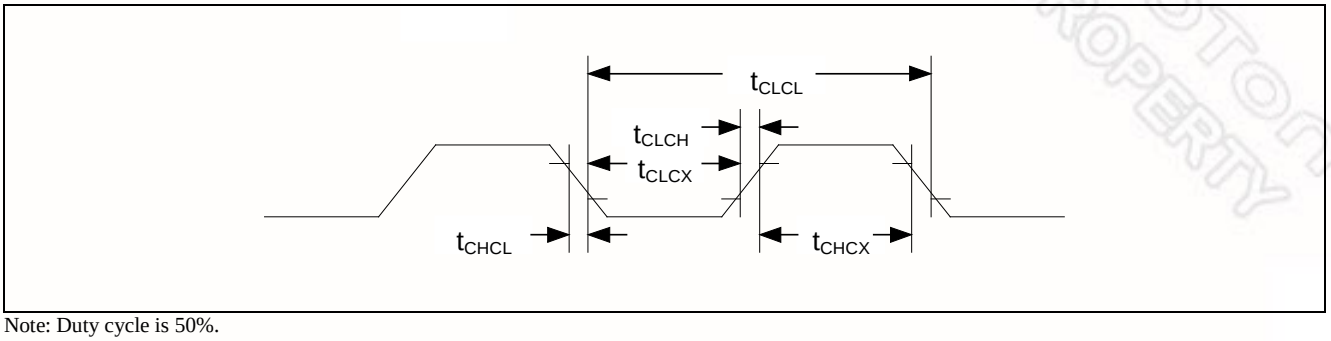
Unprogrammed value: 1111 1111B

Bit	Name	Description
7	CBS	**CONFIG Boot Selection** This bit defines from which block MCU boots after all resets except software reset. 1 = MCU will boot from APROM after all resets except software reset. 0 = MCU will boot from LDROM after all resets except software reset.
6:2	-	**Reserved**
1	LOCK	**Chip Lock Enable** 1 = Chip is unlocked. All of APROM, LDROM, and Data Flash are not locked. Their contents can be read out through a parallel Programmer/Writer. 0 = Chip is locked. APROM, LDROM, and Data Flash are locked. Their contents read through parallel Programmer/Writer will become FFH. Note that CONFIG bytes are always unlocked and can be read. Hence, once the chip is locked, the CONFIG bytes cannot be erased or programmed individually. The only way to disable chip lock is to use the whole chip erase mode. However, all data within APROM, LDROM, Data Flash, and other CONFIG bits will be erased when this procedure is executed. If the chip is locked, it does not alter the ISP function.

28.3.2 4 ~ 24 MHz XTAL Specifications

Parameter	Condition	MIN.	TYP.	MAX.	Unit
Input clock frequency	External crystal	4		24	MHz

Parameter	Symbol	MIN.	TYP.	MAX.	Units	Notes
External crystal Frequency	$1/t_{CLCL}$	4		24	MHz	
Clock High Time	t_{CHCX}	20.8	-	-	nS	
Clock Low Time	t_{CLCX}	20.8	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	



Note: Duty cycle is 50%.

28.3.3 Internal RC Oscillator Specifications – 22.1184 MHz/11.0592 MHz

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Center Frequency			22.1184/11.0592		MHz
Internal Oscillator Frequency	+25^{0}C at V_{DD} = 5V	-1		+1	%
	+25^{0}C at V_{DD} = 2.7~5.5V	-3		+3	%
	-10^{0}C~+70^{0}C at V_{DD} = 2.7~5.5V	-5		+5	%
	-40^{0}C~+85^{0}C at V_{DD} = 2.7~5.5V	-8		+8	%

31 Document Revision History

Revision	Date	Description
A1.0	-	Initial preliminary release
A2.0	2011/10/05	Revised typos
A2.1	2011/11/03	Removed the PDIP20 package Revised Table 12-3 Revised Figure 15-2
A2.2	2011/11/23	Revised Figure 29-1 Revised Chapter 22.1
A2.3	2012/02/16	Revised the following operation voltage: "V_{DD} = 2.4V to 5.5V at FOSC = 4~12MHz or Internal RC 11.0592MHz" Revised CONFIG3[1:0]=10B as a reserved item Revised operating and IDLE currents in Table 28–2 Revised Figure 24–1
A2.4	2012/05/11	Revised typos Revised BOD27/38 of Table 28–2 Revised P16/P17 of Table 5–1 Revised Figure 6-1 Removed the "N79E843A" part number Revised Chapter 21.2 Revised Chapter 27
A2.5	2012/06/26	Revised Chapter 2
A2.6	2014/04/23	Revised 20.2 ISP Command Table Revised ADC Demo Code Revised SOP16 package Removed SOP20 package

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