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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320К х 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f745igk6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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	Figure 41.	ADC accuracy characteristics



2 Functional overview

2.1 ARM[®] Cortex[®]-M7 with FPU

The ARM[®] Cortex[®]-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and a low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex[®]-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (4 Kbytes of I-cache and 4 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up the software development by using metalanguage development tools, while avoiding saturation.

Figure 2 shows the general block diagram of the STM32F745xx and STM32F746xx devices.

Note: Cortex[®]-M7 with FPU core is binary compatible with the Cortex[®]-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.



2.21 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

 V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT} , external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

2.22 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 6 compares the features of the advanced-control, general-purpose and basic timers.



SAI1 and SAI2 can be served by the DMA controller

2.27 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIFRX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

2.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S and SAI applications. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S/SAI flow with an external PLL (or Codec output).



The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Support of the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.35 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.36 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.37 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.



		F	Pin N	umber	ſ	-							
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
53	H10	K3	75	R14	94	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	G10	J3	76	R15	95	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	K9	L2	77	P15	96	108	L15	PD8	I/O	FT	-	USART3_TX, SPDIFRX_IN11, FMC_D13, EVENTOUT	-
56	J9	M1	78	P14	97	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	H9	H4	79	N15	98	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	G9	K2	80	N14	99	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	K10	H6	81	N13	100	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	J10	H5	82	M15	101	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-



		F	Pin Nu	umber	ſ								
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	G2	93	H14	112	135	H14	PG8	I/O	FT	-	SPI6_NSS, SPDIFRX_IN2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT	-
-	-	D2	94	G12	113	136	G10	VSS	S	-	-	-	-
-	F6	G1	95	H13	114	137	G11	VDDUSB	S	-	-	-	-
63	F10	F2	96	H15	115	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	E10	F3	97	G15	116	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	F9	E4	98	G14	117	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	E9	E3	99	F14	118	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, DCMI_D3, EVENTOUT	-
67	D9	F1	100	F15	119	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
68	C9	E2	101	E15	120	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VB US

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)



4 Memory mapping

The memory map is shown in *Figure 19*.



Figure 19. Memory map



				Тур		Ma	x ⁽²⁾	
Symbol	Parameter	Conditions ⁽¹⁾	1	۲ _A =25 °C	2	T _A =85 °C	T _A =105 °C	Unit
			V _{BAT} = 1.7 V	V _{BAT} = 2.4 V	V _{BAT} = 3.3 V	V _{BAT} =	= 3.6 V	
		Backup SRAM OFF, RTC and LSE OFF	0.03	0.03	0.04	0.2	0.4	
		Backup SRAM ON, RTC and LSE OFF	0.74	0.75	0.78	3.0	7.0	
	Supply current in V _{BAT} mode	Backup SRAM OFF, RTC ON and LSE in low drive mode	0.40	0.52	0.72	2.8	6.5	
			Backup SRAM OFF, RTC ON and LSE in medium low drive mode	0.40	0.52	0.72	2.8	6.5
I _{DD_VBAT}		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	0.54	0.64	0.85	3.3	7.6	μA
		Backup SRAM OFF, RTC ON and LSE in high drive mode	0.62	0.73	0.94	3.6	8.4	
		Backup SRAM ON, RTC ON and LSE in low drive mode	1.06	1.18	1.41	5.4	12.7	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	1.16	1.28	1.51	5.8	13.6	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	1.18	1.3	1.54	5.9	13.8	
		Backup SRAM ON, RTC ON and LSE in High drive mode	1.36	1.48	1.73	6.7	15.5	

Table 33. Typical and maximum current consumptions in V_{BAT} mode

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_{L} of 6 pF for typical values.

2. Guaranteed by characterization results.



pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

 I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load V_{DD} is the MCU supply voltage

 f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: C = C_{INT} + C_{EXT}

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Тур V _{DD} = 3.3 V	Тур V _{DD} = 1.8 V	Unit
			2	0.1	0.1	
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
		$C_{EXT} = 0 pF$	60	3.1	1.6	
		U - UINT · US · UEXT	84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
	I/O switching			108	5.6	-
IDDIO	Current		2	0.2	0.1	ША
			8	0.6	0.3	-
			25	1.8	1.1	
		С _{ЕХТ} = 10 рF	50	3.1	2.3	
		$C = C_{INT} + C_S + C_{EXT}$	60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	
			108	18.11	-	

Table 34. Switching output I/O current consumption⁽¹⁾



5.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 56: I/O static characteristics*).

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
R _{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	kΩ
V _{F(NRST)} ⁽²⁾	NRST Input filtered pulse	-	-	-	100	ns
V _{NF(NRST)} ⁽²⁾	NRST Input not filtered pulse	V _{DD} > 2.7 V	300	-	-	ns
T _{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μs

Table 59. NRST pin characteristics

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2. Guaranteed by design.





1. The reset network protects the device against parasitic resets.

 The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 59. Otherwise the reset is not taken into account by the device.



Symbol	Parameter	Min	Max	Unit
t _{w(CLK)}	FMC_CLK period	2T _{HCLK} -0.5	-	
t _{d(CLKL-NExL)}	FMC_CLK low to FMC_NEx low (x=02)	-	2	
t _{d(CLKH_NExH)}	FMC_CLK high to FMC_NEx high (x= 02)	T _{HCLK} +0.5	-	
t _{d(CLKL-NADVL)}	FMC_CLK low to FMC_NADV low	-	1.5	
t _{d(CLKL-NADVH)}	FMC_CLK low to FMC_NADV high	0	-	
t _{d(CLKL-AV)}	FMC_CLK low to FMC_Ax valid (x=1625)	-	2	
t _{d(CLKH-AIV)}	FMC_CLK high to FMC_Ax invalid (x=1625)	T _{HCLK}	-	
t _{d(CLKL-NOEL)}	L) FMC_CLK low to FMC_NOE low -		2	ns
t _{d(CLKH-NOEH)}	FMC_CLK high to FMC_NOE high	T _{HCLK} -0.5	-	
t _{d(CLKL-ADV)}	FMC_CLK low to FMC_AD[15:0] valid	-	3	
t _{d(CLKL-ADIV)}	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
t _{su(ADV-CLKH)}	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
t _{h(CLKH-ADV)}	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
t _{su(NWAIT-CLKH)}	FMC_NWAIT valid before FMC_CLK high	2	-	
t _{h(CLKH-NWAIT)}	FMC_NWAIT valid after FMC_CLK high	3.5	-	

Table 96. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

1. Guaranteed by characterization results.



Symbol	Parameter	Min	Max	Unit					
t _(CLK)	FMC_CLK period	2T _{HCLK} -1	-						
t _{d(CLKL-NExL)}	FMC_CLK low to FMC_NEx low (x=02)	-	2.5						
t _(CLKH-NExH)	FMC_CLK high to FMC_NEx high (x= 02)	T _{HCLK} +0.5	-						
t _{d(CLKL-NADVL)}	FMC_CLK low to FMC_NADV low	-	1.5						
t _{d(CLKL-NADVH)}	FMC_CLK low to FMC_NADV high	0	-						
t _{d(CLKL-AV)}	FMC_CLK low to FMC_Ax valid (x=1625)	-	2.5						
t _{d(CLKH-AIV)}	FMC_CLK high to FMC_Ax invalid (x=1625)	0	-	200					
t _{d(CLKL-NWEL)}	FMC_CLK low to FMC_NWE low	-	1.5	115					
t _{d(CLKH-NWEH)}	FMC_CLK high to FMC_NWE high	T _{HCLK} +1	-						
t _{d(CLKL-Data)}	FMC_D[15:0] valid data after FMC_CLK low	-	3						
t _{d(CLKL-NBLL)}	FMC_CLK low to FMC_NBL low	1.5	-						
t _{d(CLKH-NBLH)}	FMC_CLK high to FMC_NBL high	T _{HCLK} +0.5	-						
t _{su(NWAIT-CLKH)}	FMC_NWAIT valid before FMC_CLK high	2	-						
t _{h(CLKH-NWAIT)}	FMC_NWAIT valid after FMC_CLK high	3.5	-						

Table 99. Synchronous non-multiplexed PSRAM write timings⁽¹⁾

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 66 through *Figure 69* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the $T_{\mbox{HCLK}}$ is the HCLK clock period.



SDRAM waveforms and timings

 CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the $T_{\mbox{HCLK}}$ is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V \leq V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).



Figure 70. SDRAM read access waveforms (CL = 1)





Figure 71. SDRAM write access waveforms

Table 104. SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Мах	Unit
t _{w(SDCLK)}	FMC_SDCLK period	2T _{HCLK} -0.5	2T _{HCLK} +0.5	
t _{d(SDCLKL_Data})	Data output valid time	-	2	
^t h(SDCLKL _Data)	Data output hold time	0.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	4	
t _{d(SDCLKL_SDNWE)}	SDNWE valid time	-	0.5	
t _{h(SDCLKL_SDNWE)}	SDNWE hold time	0	-	20
t _{d(SDCLKL_SDNE)}	Chip select valid time	-	0.5	115
t _{h(SDCLKLSDNE)}	Chip select hold time	0	-	
td(SDCLKL_SDNRAS)	SDNRAS valid time	-	0.5	
th(SDCLKL_SDNRAS)	SDNRAS hold time	0	-	
td(SDCLKL_SDNCAS)	SDNCAS valid time	-	0.5	
t _{d(SDCLKL_SDNCAS)}	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.







1. Dimensions are expressed in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.



Figure 81. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example

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Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.





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Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.



Figure 96. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package top view example

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Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.





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