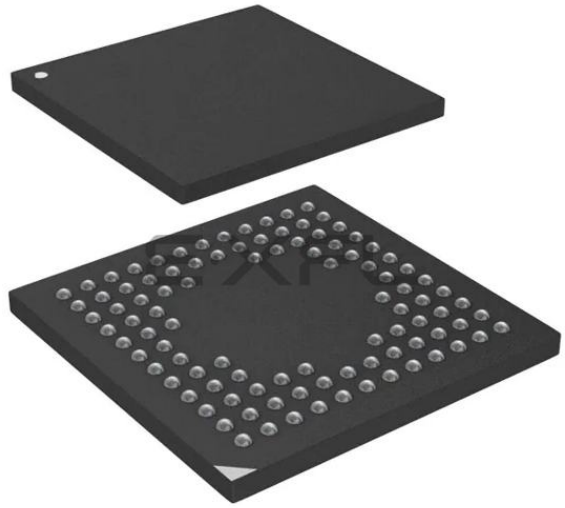

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f745veh6

2.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.30 SD/SDIO/MMC card host interface (SDMMC)

An SDMMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory card specification version 2.0.

The SDMMC card specification version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Support of 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.38 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 108 MHz.

2.39 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

2.40 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

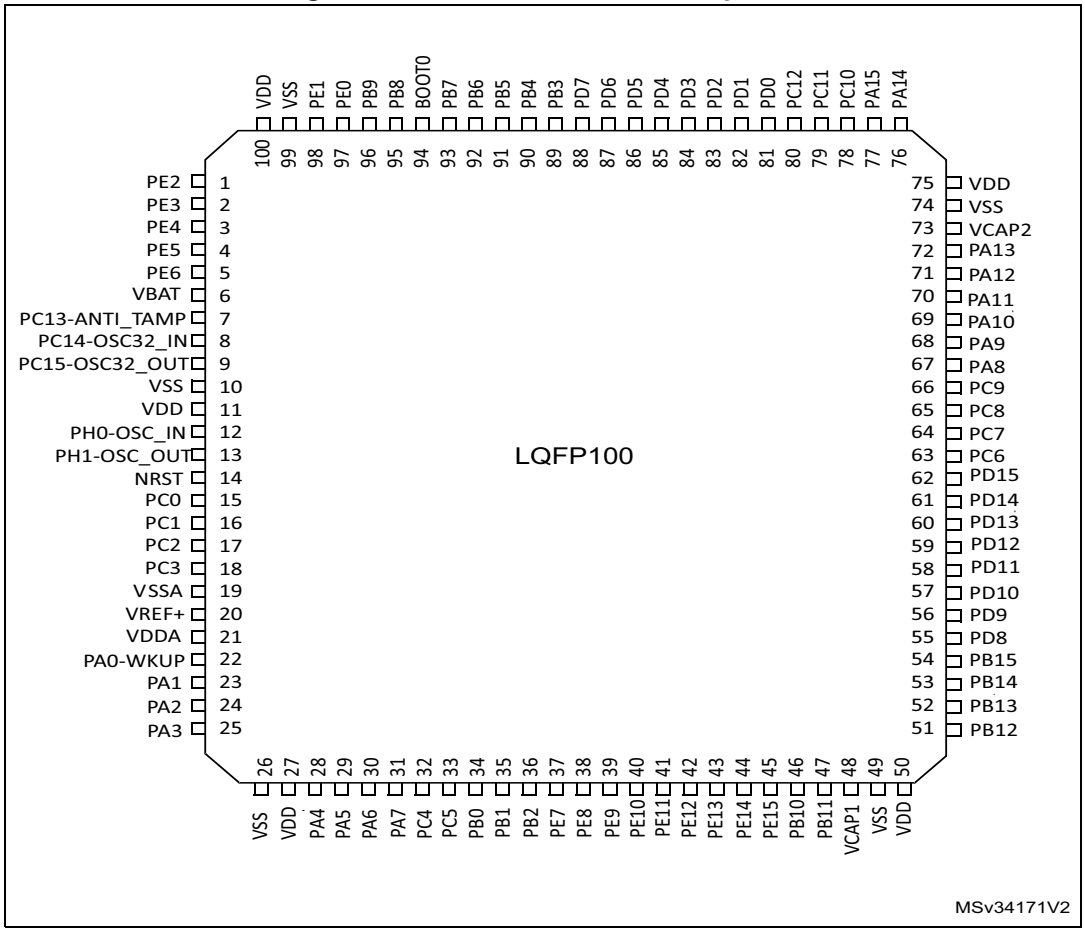
As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.41 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

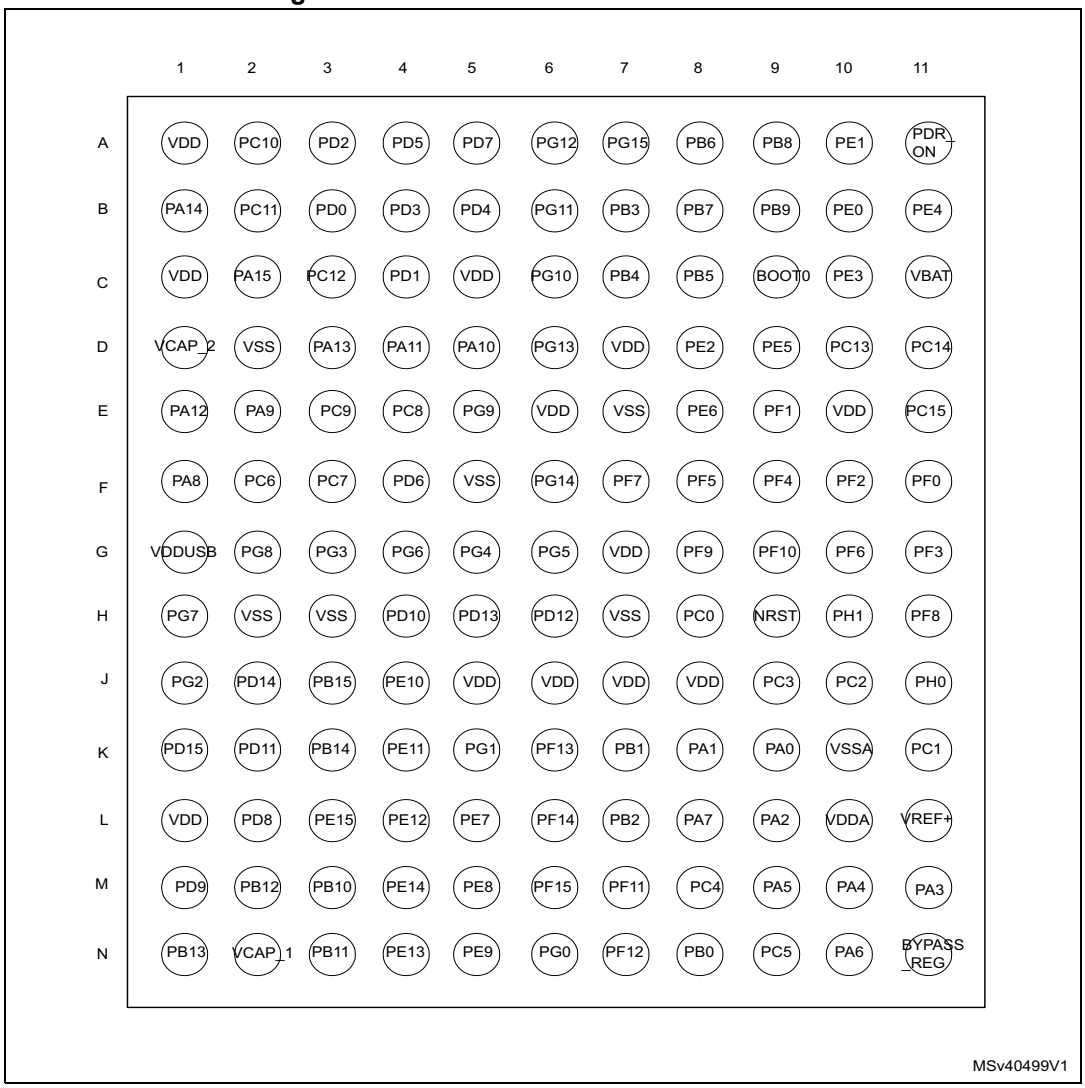
3 Pinouts and pin description

Figure 11. STM32F74xVx LQFP100 pinout



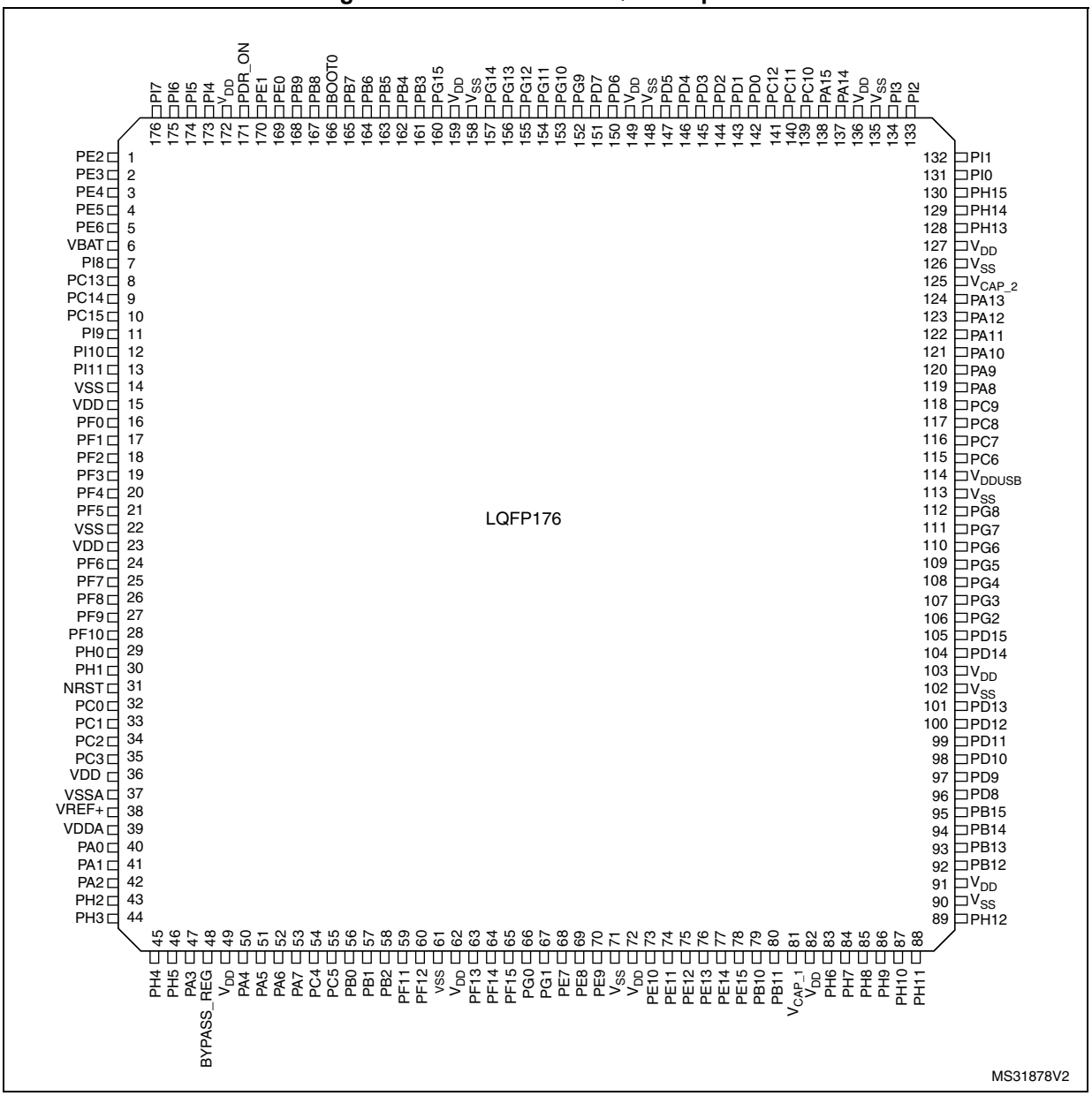
2. The above figure shows the package top view.

Figure 13. STM32F74xZx WLCSP143 ballout



1. The above figure shows the package top view.

Figure 15. STM32F74xIx LQFP176 pinout



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F745xx and STM32F746xx pin and ball definition

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
1	A3	D8	1	A2	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	B3	C10	2	A1	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
3	C3	B11	3	B1	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	-	-	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	-	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	-	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	-	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	-	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	-	A7	132	B7	160	191	B7	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	A7	B7	133	A10	161	192	A10	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, EVENTOUT	-
90	A6	C7	134	A9	162	193	A9	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, EVENTOUT	-
91	C5	C8	135	A6	163	194	A8	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT	-
92	B5	A8	136	B6	164	195	B6	PB6	I/O	FT	-	TIM4_CH1, HDMI-CEC, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, FMC_SDNE1, DCMI_D5, EVENTOUT	-
93	A5	B8	137	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
94	D5	C9	138	D6	166	197	E6	BOOT	I	B	-	-	VPP

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4001 6C00- 0x4001 FFFF	Reserved
APB2	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDMMC
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 44. PLLI2S characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)	-	0.95(2)	1	2.10	MHz
$f_{PLLSAIP\_OUT}$	PLLSAI multiplier output clock for 48 MHz	-	-	48	75	
$f_{PLLSAIQ\_OUT}$	PLLSAI multiplier output clock for SAI	-	-	-	216	
$f_{PLLSAIR\_OUT}$	PLLSAI multiplier output clock for LCD-TFT	-	-	-	216	
f_{VCO_OUT}	PLLSAI VCO output	-	100	-	432	
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Figure 47. SPI timing diagram - slave mode and CPHA = 1

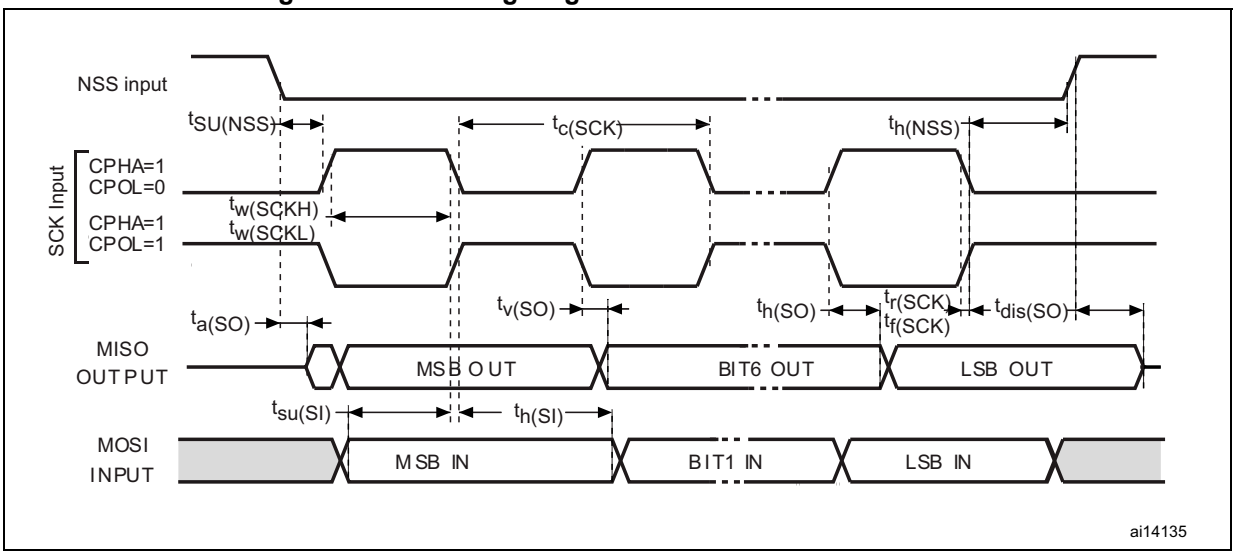
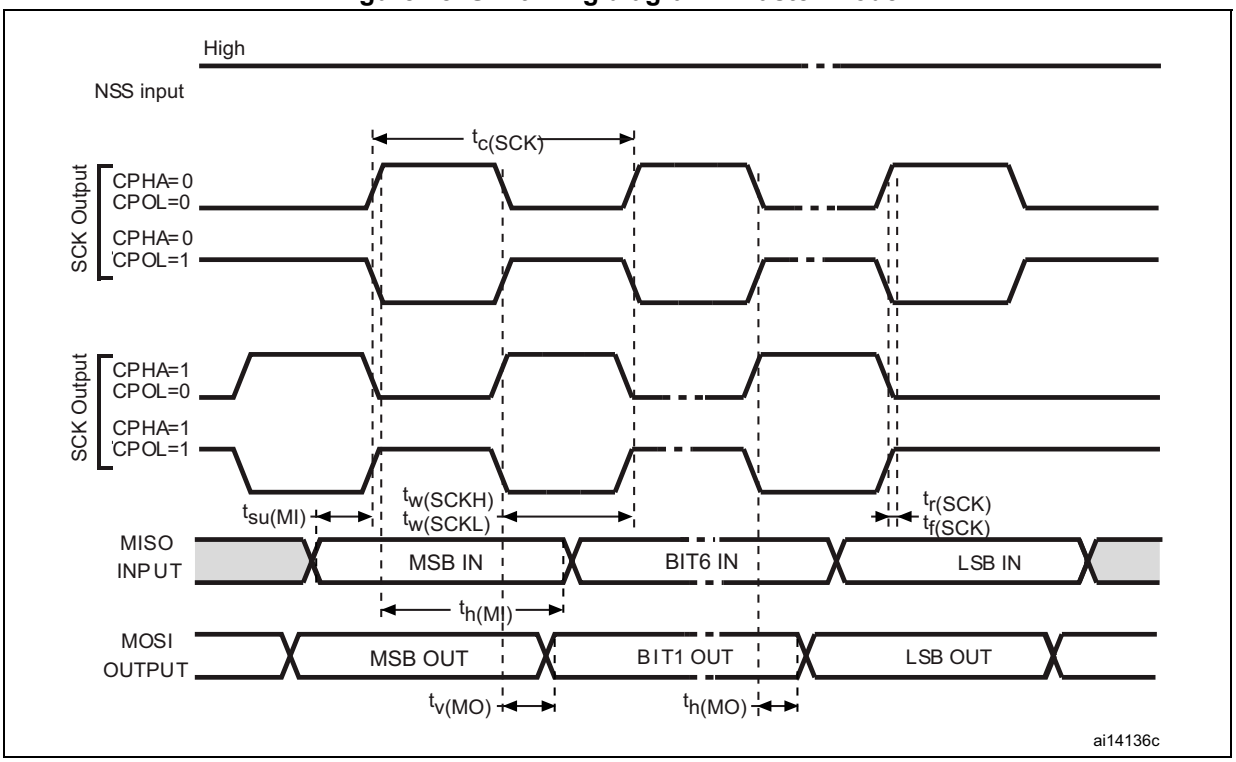


Figure 48. SPI timing diagram - master mode



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 77* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 79. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

Table 80. USB OTG full speed DC electrical characteristics

Symbol		Parameter	Conditions	Min. (1)	Typ.	Max. (1)	Unit
Input levels	V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

1. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+1.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}-0.5$	$7T_{HCLK}+0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 62 through *Figure 65* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

– For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).

– For 1.71 V≤V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Table 99. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK}-1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK}+0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK}+1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK}+0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 66 through *Figure 69* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 106. Quad-SPI characteristics (continued)in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 -1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2+1	
ts(IN)	Data input setup time	-	1	-	-	
th(IN)	Data input hold time		3	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	3	
		1.71 V<V_{DD}<3.6 V	-	1.5	4	
th(OUT)	Data output hold time	-	0	-	-	

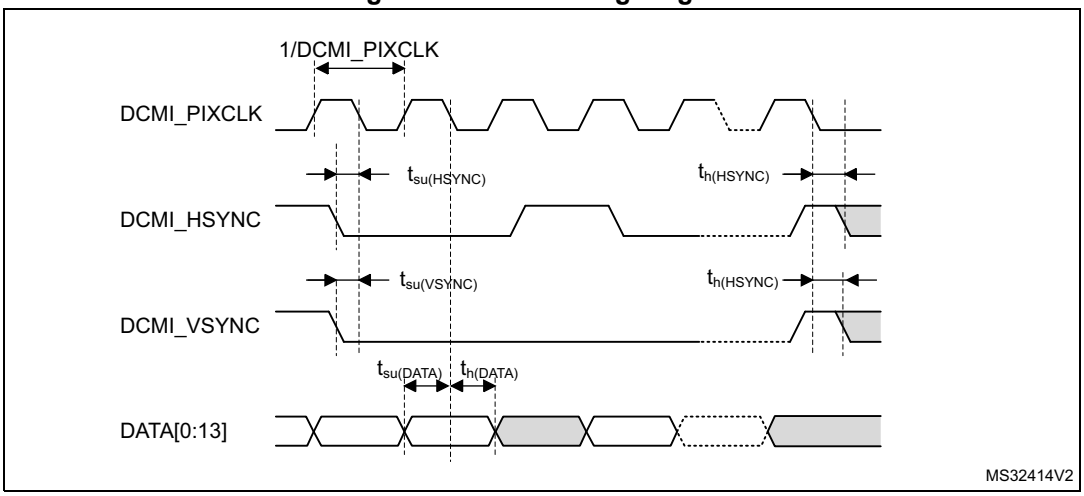
1. Guaranteed by characterization results.

Table 107. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 -1	-	t(CK)/2	ns
tw(CKL)			t(CK)/2	-	t(CK)/2+ 1	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	1.5	-	-	
		1.71 V<V_{DD}<2 V	0.75	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	3.5	-	-	
		1.71 V<V_{DD}<2 V	4.5			
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8	10.5	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	8	14.5	
		DHHC=1 Pres=1, 2...	-	Thclk/2 +1.75	Thclk/2 +2.25	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	7.5	-	-	
		DHHC=1 Pres=1, 2...	Thclk/2 +1.5	-	-	

1. Guaranteed by characterization results.

Figure 74. DCMI timing diagram



5.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 109* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity : low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

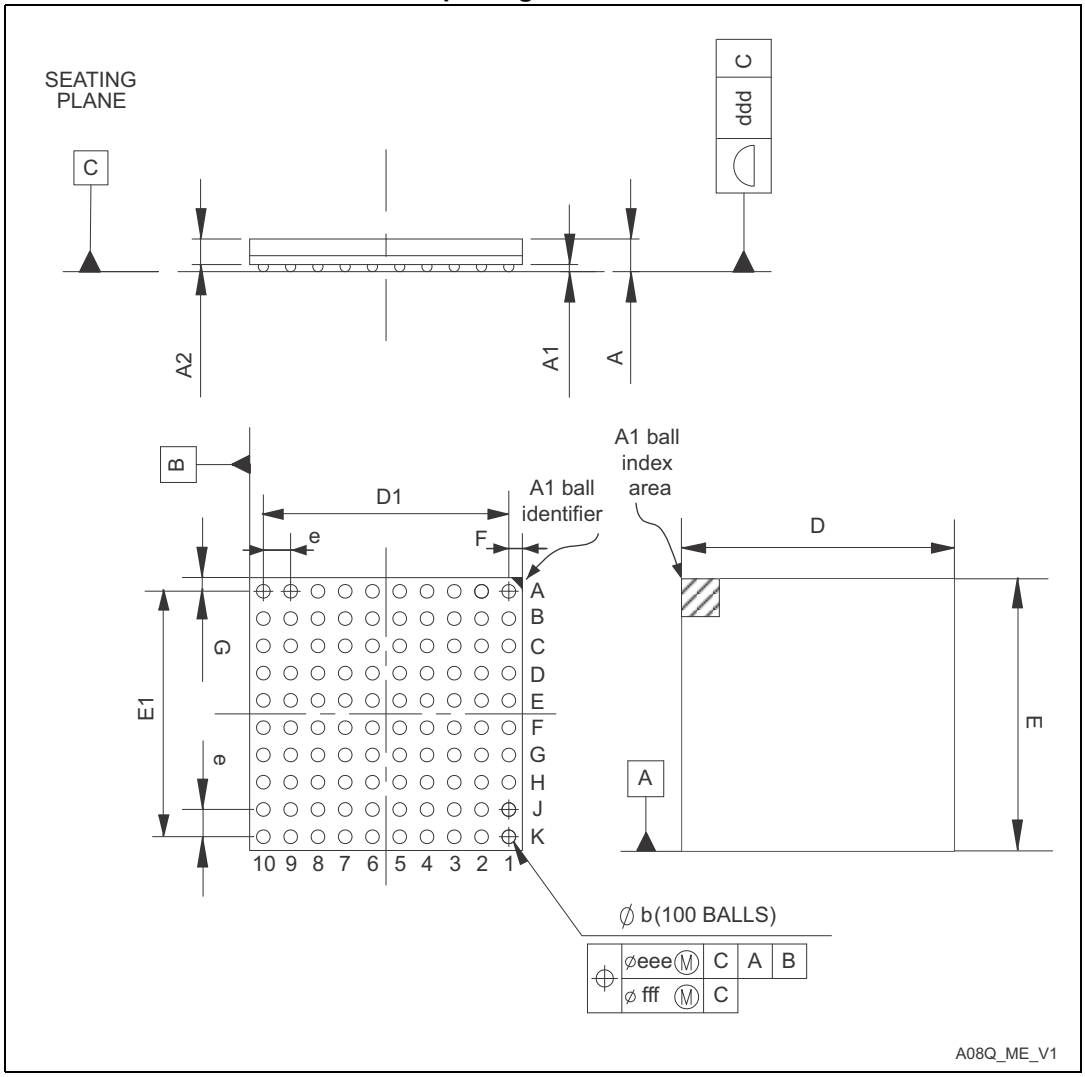
Table 109. LTDC characteristics (1)

Symbol	Parameter	Min	Max	Unit
f_{CLK}	LTDC clock output frequency	-	45	MHz
D_{CLK}	LTDC clock output duty cycle	45	55	%
$t_{w(CLKH)}$ $t_{w(CLKL)}$	Clock High time, low time	tw(CLK)/2 − 0.5	tw(CLK)/2+0.5	ns
$t_{v(DATA)}$	Data output valid time	-	6	
$t_{h(DATA)}$	Data output hold time	2	-	
$t_{v(HSYNC)}$	HSYNC/VSYNC/DE output valid time	-	3	
$t_{v(VSYNC)}$				
$t_{v(DE)}$				
$t_{h(HSYNC)}$	HSYNC/VSYNC/DE output hold time	0.5	-	
$t_{h(VSYNC)}$				
th(DE)				

1. Guaranteed by characterization results.

6.2 TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information

Figure 82. TFBGA100, 8 × 8 × 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 113. TFBGA100, 8 x 8 × 0.8 mm thin fine-pitch ball grid array package mechanical data

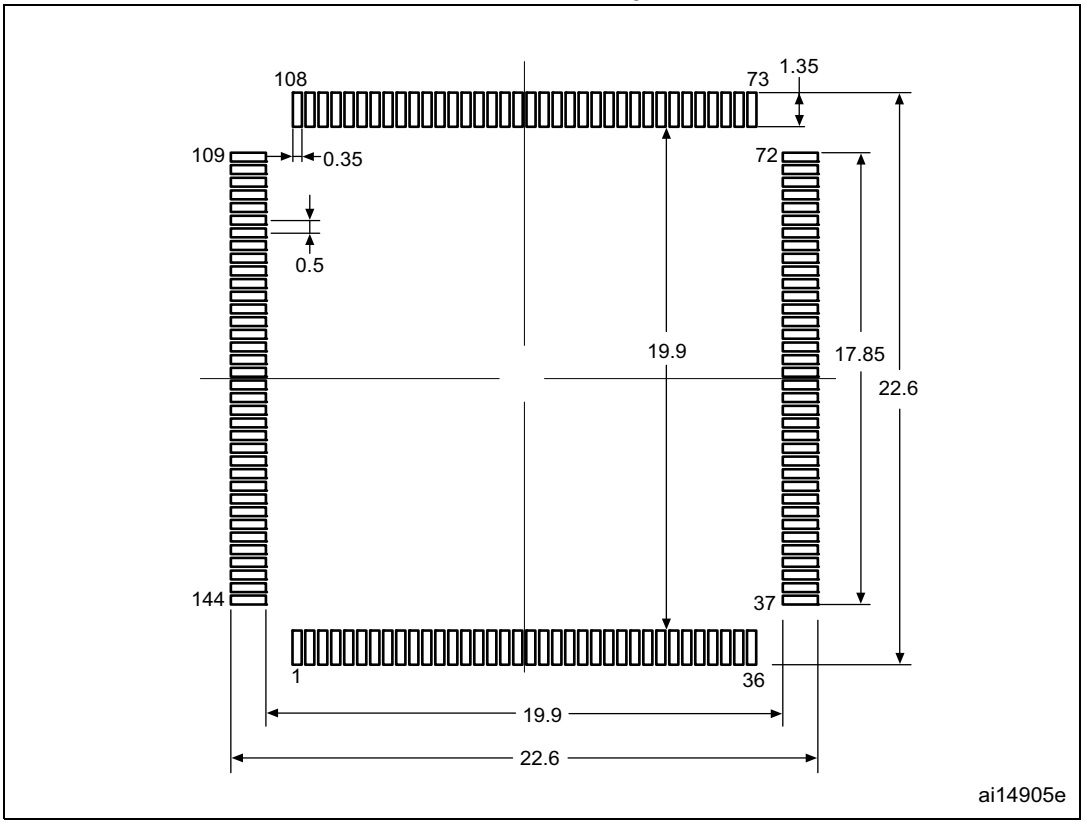
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177

Table 117. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

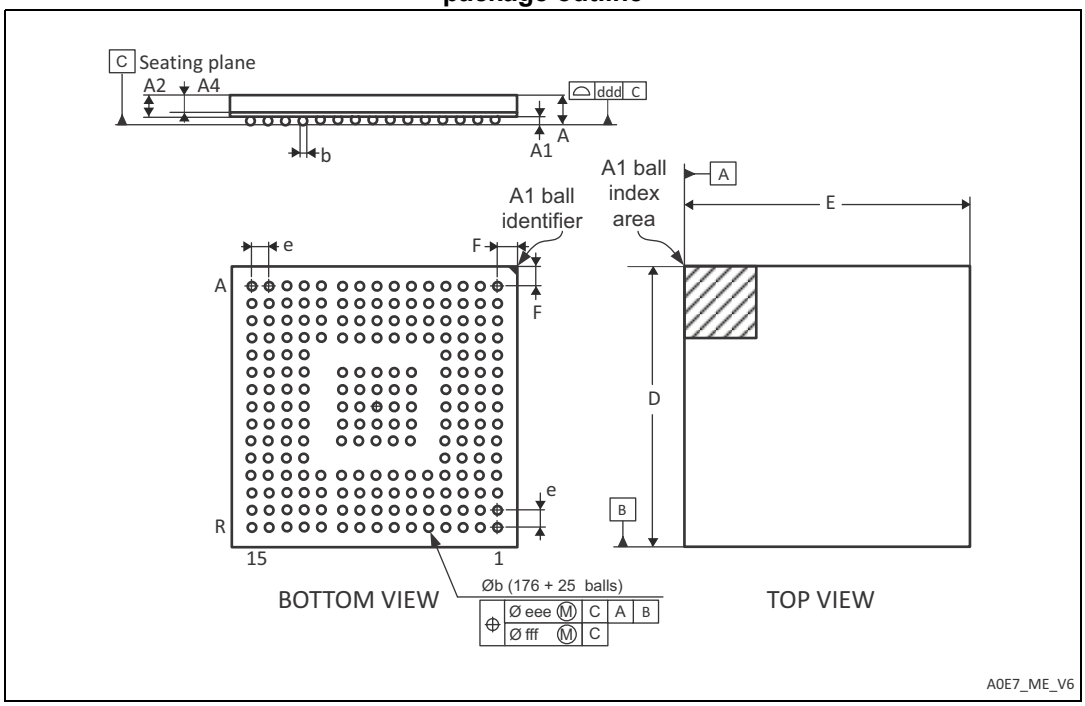
Figure 89. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.7 UFBGA 176+25, 10 x 10 x 0.65 mm ultra thin-pitch ball grid array package information

Figure 97. UFBGA 176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

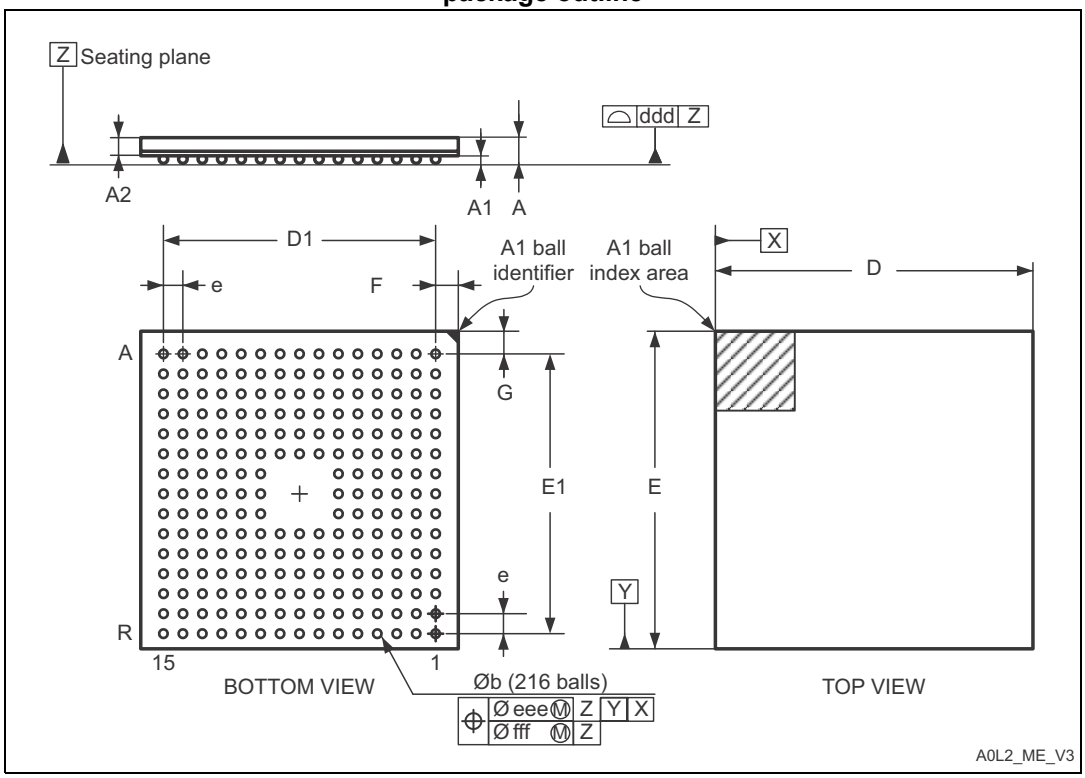
Table 120. UFBGA 176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.8 TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package information

Figure 100. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 122. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-