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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f745vgt6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V₁₂ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V₁₂ minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V₁₂ minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V₁₂ minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

2.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F74xxx devices (see *Table 6* for differences).

• TIM2, TIM3, TIM4, TIM5

The STM32F74xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

• TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

2.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.30 SD/SDIO/MMC card host interface (SDMMC)

An SDMMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory card specification version 2.0.

The SDMMC card specification version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Support of 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Support of the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.35 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.36 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.37 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

		F	Pin Nu	umber									
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
31	КЗ	L8	43	R3	53	56	R3	PA7	I/O	FT	(4)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, ETH_MII_RX_DV/ETH_R MII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_IN7
32	G4	M8	44	N5	54	57	N5	PC4	I/O	FT	(4)	I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RM II_RXD0, FMC_SDNE0, EVENTOUT	ADC12_IN14
33	H4	N9	45	P5	55	58	P5	PC5	I/O	FT	(4)	SPDIFRX_IN3, ETH_MII_RXD1/ETH_RM II_RXD1, FMC_SDCKE0, EVENTOUT	ADC12_IN15
-	-	J7	-	-	-	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-
34	J4	N8	46	R5	56	61	R5	PB0	I/O	FT	(4)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_IN8
35	K4	K7	47	R4	57	62	R4	PB1	I/O	FT	(4)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_IN9
36	G5	L7	48	M6	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

		F	Pin Nu	umbei	r								
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
95	B4	A9	139	A5	167	198	A7	PB8	I/O	FT	_	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
96	A4	В9	140	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	D4	B10	141	A4	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_Rx, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	C4	A10	142	A3	170	201	A5	PE1	I/O	FT	_	LPTIM1_IN2, UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	E4	-	-	D5	-	202	F6	VSS	S	-	-	-	-
-	F7	A11	143	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	F4	D7	144	C5	172	204	E7	VDD	S	-	-	-	-
-	-	-	-	D4	173	205	C3	Pl4	I/O	FT	-	TIM8_BKIN, SAI2_MCK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-

Table 10.	STM32F745xx and	STM32F746xx p	in and ball	definition	(continued)
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		F	Pin Nu	umbei	r			-					
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	Pin name (function after reset) ⁽¹⁾	Pin type	Pin type I/O structure		Alternate functions	Additional functions
-	-	-	-	C3	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	-	-	C2	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

1. Function availability depends on the chosen device.

 PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:

- The speed should not exceed 2 MHz with a maximum load of 30 pF.

- These I/Os must not be used as a current source (e.g. to drive an LED).

3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F75xxx and STM32F74xxx reference manual.

4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

 If the device is delivered in an WLCSP143, UFBGA176, LQFP176, TFBGA100 or TFBGA216 package, and the BYPASS_REG pin is set to VDD (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).

Pinouts and pin description

			(
Pin name	NOR/PSRAM/SR AM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	DA8	D8	D8
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-
PB7	NADV	NADV	-	-

Table 11. FMC pin definition (continued)

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M7	0xE000 0000 - 0xE00F FFFF	Cortex-M7 internal peripherals
	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	Quad-SPI control register
AHB3	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
	0x5006 0800 - 0x5006 0BFF	RNG
	0x5005 0400 - 0x5006 07FF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
AHB2	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Table	13.	STM32F7	45xx ar	nd STM	32F746xx	register	boundary	addresses
IUDIC			TOAN UI			register	Soundary	uuui 00000

Figure 31. Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R _F	Feedback resistor	-	-	200	-	kΩ
I _{DD}	HSE current consumption	V _{DD} =3.3 V, ESR= 30 Ω, C _L =5 pF@25 MHz	-	450	-	110
		V _{DD} =3.3 V, ESR= 30 Ω, C _L =10 pF@25 MHz	-	530	-	μΑ
ACC _{HSE} ⁽²⁾	HSE accuracy	-	- 500	-	500	ppm
G _m _crit_max	Maximum critical crystal g _m	Startup	-	-	1	mA/V
t _{SU(HSE} ⁽³⁾	Startup time	V _{DD} is stabilized	-	2	-	ms

Table	39	HSF	4-26	MH7	oscillator	characteris	stics ⁽¹	
Ianie	JJ.	IIOL	4-20		USCINALUI	Characteris	ະບົວ	1

1. Guaranteed by design.

2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.

 t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is based on characterization results. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

5.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD S5.3.1-2009, LQFP100, LQFP144, LQFP176, LQFP208, WLCSP143, UFBGA176, TFBGA100 and TFBGA216 packages	C3	250	V

Table 53. ESD absolute maximum ratings

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 54. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105 \text{ °C conforming to JESD78A}$	II level A

5.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 78* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5V_{DD}

Refer to Section 5.3.17: I/O port characteristics for more details on the input/output alternate function characteristics (SCK,SD,WS).

Symbol	Parameter	Conditions	Min	Мах	Unit	
f _{MCKL}	SAI Main clock output	-	256 x 8K	256xFs ⁽²⁾	MHz	
F	SAL clock frequency	Master data: 32 bits	-	128xFs	N411-	
FSCK	SAI Clock frequency	Slave data: 32 bits	-	128xFs		
D _{SCK}	SAI clock frequency duty cycle	Slave receiver	30	70	%	
t _{v(FS)}	FS valid time	Master mode	8	22		
t _{su(FS)}	FS setup time	Slave mode	2	-		
4	ES hold time	Master mode	8	-		
^t h(FS)	FS hold lime	Slave mode	0	-		
t _{su(SD_MR)}	Data innut actus tima	Master receiver	5	-		
t _{su(SD_SR)}	Data input setup time	Slave receiver	3	-		
t _{h(SD_MR)}	Data input hold time	Master receiver	0	-	ns	
t _{h(SD_SR)}		Slave receiver	6	-		
t _{v(SD_ST)}		Slave transmitter (after enable	_	15		
t _{h(SD_ST)}	Data output valid time	edge)	_	10		
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	20		
t _{h(SD_MT)}	Data output hold time	Master transmitter (after enable edge)	7	-		

Table 78	. SAI	characteristics ⁽¹⁾
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1. Guaranteed by characterization results.

2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)

Symbol	Parameter	Min	Тур	Max	Unit	
-	f _{HCLK} value to guarantee proper operation of USB HS interface		30	-	-	MHz
F _{START_8BIT}	Frequency (first transition)	8-bit ±10%	54	60	66	MHz
F _{STEADY}	Frequency (steady state) ±500 ppm		59.97	60	60.03	MHz
D _{START_8BIT}	Duty cycle (first transition)	8-bit ±10%	40	50	60	%
D _{STEADY}	Duty cycle (steady state) ±500 ppm		49.975	50	50.025	%
t _{STEADY}	Time to reach the steady state frequency and duty cycle after the first transition		-	-	1.4	ms
t _{START_DEV}	Clock startup time after the	Peripheral	-	-	5.6	me
t _{START_HOST}	de-assertion of SuspendM	Host	-	-	-	1115
t _{PREP}	PHY preparation time after the of the input clock	first transition	_	_	-	μs

Table 83. U	JSB HS clock	timina r	parameters ⁽¹⁾
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1. Guaranteed by design.

Figure 54. ULPI timing diagram

Figure 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table OO As			
Table 90. As	vnchronous non-multiplexe	a Skawi/PSkawi/NUK	write timinas ''

Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FMC_NE low time	3T _{HCLK} -0.5	3T _{HCLK} +1.5	
t _{v(NWE_NE)}	FMC_NEx low to FMC_NWE low	T _{HCLK} -0.5	T _{HCLK} + 1	
t _{w(NWE)}	FMC_NWE low time	T _{HCLK} -0.5	T _{HCLK} + 1	
t _{h(NE_NWE)}	FMC_NWE high to FMC_NE high hold time	T _{HCLK} -0.5	-	
t _{v(A_NE)}	FMC_NEx low to FMC_A valid	-	0	
t _{h(A_NWE)}	Address hold time after FMC_NWE high T _{HC}		-	20
t _{v(BL_NE)}	FMC_NEx low to FMC_BL valid	-	0	115
t _{h(BL_NWE)}	FMC_BL hold time after FMC_NWE high	T _{HCLK} -0.5	-	
t _{v(Data_NE)}	Data to FMC_NEx low to Data valid	-	T _{HCLK} + 3	
t _{h(Data_NWE)}	Data hold time after FMC_NWE high	T _{HCLK} +0.5	-	
t _{v(NADV_NE)}	FMC_NEx low to FMC_NADV low	-	0	
t _{w(NADV)}	FMC_NADV low time	-	T _{HCLK} + 0.5	

1. Guaranteed by characterization results.

SDRAM waveforms and timings

 CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the $T_{\mbox{HCLK}}$ is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V \leq V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 70. SDRAM read access waveforms (CL = 1)

Dimension	Recommended values				
Pitch	0.8				
Dpad	0.400 mm				
Dsm	0.470 mm typ (depends on the soldermask registration tolerance)				
Stencil opening	0.400 mm				
Stencil thickness	Between 0.100 mm and 0.125 mm				
Pad trace width	0.120 mm				

 Table 114. TFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Мах
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
CCC	-	-	0.080	-	-	0.0031

Table 117. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat packagemechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.

1. Dimensions are expressed in millimeters.

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6.5 LQFP176, 24 x 24 mm low-profile quad flat package information

C Seating plane 0.25 mm gauge plane A1 HD 11 PIN 1 D **IDENTIFICATION** b ZE Е HE е ZD b 1T_ME_V2

Figure 91. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline

1. Drawing is not to scale.

Table 118. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat packagemechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Figure 92. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.
- The over-drive mode is not supported.

A.1 Operating conditions

Table 126. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states (f _{Flashmax})	Maximum Flash memory access frequency with wait states ⁽¹⁾⁽²⁾	I/O operation	Possible Flash memory operations
V _{DD} =1.7 to 2.1 V ⁽³⁾	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	 No I/O compensation 	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.

2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.

 V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to Section 2.17.1: Internal reset ON).

